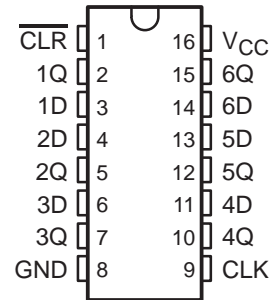


# SN54HC174, SN74HC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

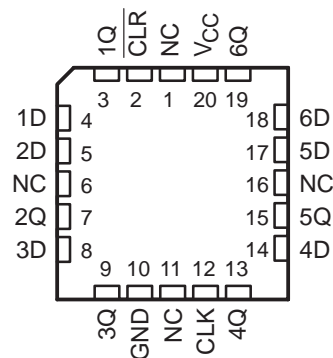
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Contain Six Flip-Flops With Single-Rail Outputs
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

SN54HC174 . . . J OR W PACKAGE  
SN74HC174 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC174 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These positive-edge-triggered D-type flip-flops have a direct clear (CLR) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

## ORDERING INFORMATION

$T_A$	PACKAGE†	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC174N	SN74HC174N
	SOIC – D	Tube of 40	SN74HC174D	HC174
		Reel of 2500	SN74HC174DR	
		Reel of 250	SN74HC174DT	
	SOP – NS	Reel of 2000	SN74HC174NSR	HC174
	SSOP – DB	Reel of 2000	SN74HC174DBR	HC174
	TSSOP – PW	Tube of 90	SN74HC174PW	HC174
Reel of 2000		SN74HC174PWR		
Reel of 250		SN74HC174PWT		
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC174J	SNJ54HC174J
	CFP – W	Tube of 150	SNJ54HC174W	SNJ54HC174W
	LCCC – FK	Tube of 55	SNJ54HC174FK	SNJ54HC174FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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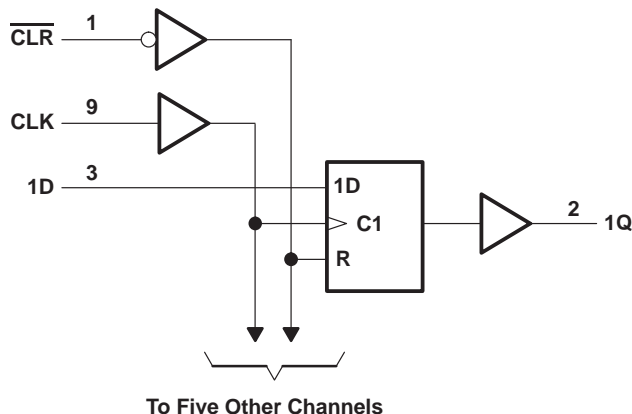
# SN54HC174, SN74HC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

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**FUNCTION TABLE**  
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$Q_0$

## logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	73°C/W
DB package	82°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54HC174, SN74HC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

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## recommended operating conditions (see Note 3)

		SN54HC174			SN74HC174			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5	1.5		V	
		V <sub>CC</sub> = 4.5 V		3.15	3.15			
		V <sub>CC</sub> = 6 V		4.2	4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V			0.5		0.5	V
		V <sub>CC</sub> = 4.5 V			1.35		1.35	
		V <sub>CC</sub> = 6 V			1.8		1.8	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
Δt/Δv	Input transition rise/fall time	V <sub>CC</sub> = 2 V			1000		1000	ns
		V <sub>CC</sub> = 4.5 V			500		500	
		V <sub>CC</sub> = 6 V			400		400	
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC174		SN74HC174		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V		
			4.5 V	4.4	4.499		4.4		4.4			
			6 V	5.9	5.999		5.9		5.9			
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		3.84			
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		5.34			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V	
			4.5 V		0.001	0.1		0.1		0.1		
			6 V		0.001	0.1		0.1		0.1		
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33		
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V				8		160		80	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10		pF



# SN54HC174, SN74HC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC174		SN74HC174		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	6		4.2		5		MHz
		4.5 V	31		21		25		
		6 V	36		25		29		
t <sub>w</sub>	Pulse duration	CLR low	2 V	80	120	100			ns
			4.5 V	16	24	20			
			6 V	14	20	17			
	CLK high or low	2 V	80	120	100				
		4.5 V	16	24	20				
		6 V	14	20	17				
t <sub>su</sub>	Setup time before CLK↑	Data	2 V	100	150	125			ns
			4.5 V	20	30	25			
			6 V	17	25	21			
	CLR inactive	2 V	100	150	125				
		4.5 V	20	30	25				
		6 V	17	25	21				
t <sub>h</sub>	Hold time, data after CLK↑	2 V	0	0	0			ns	
		4.5 V	0	0	0				
		6 V	0	0	0				

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

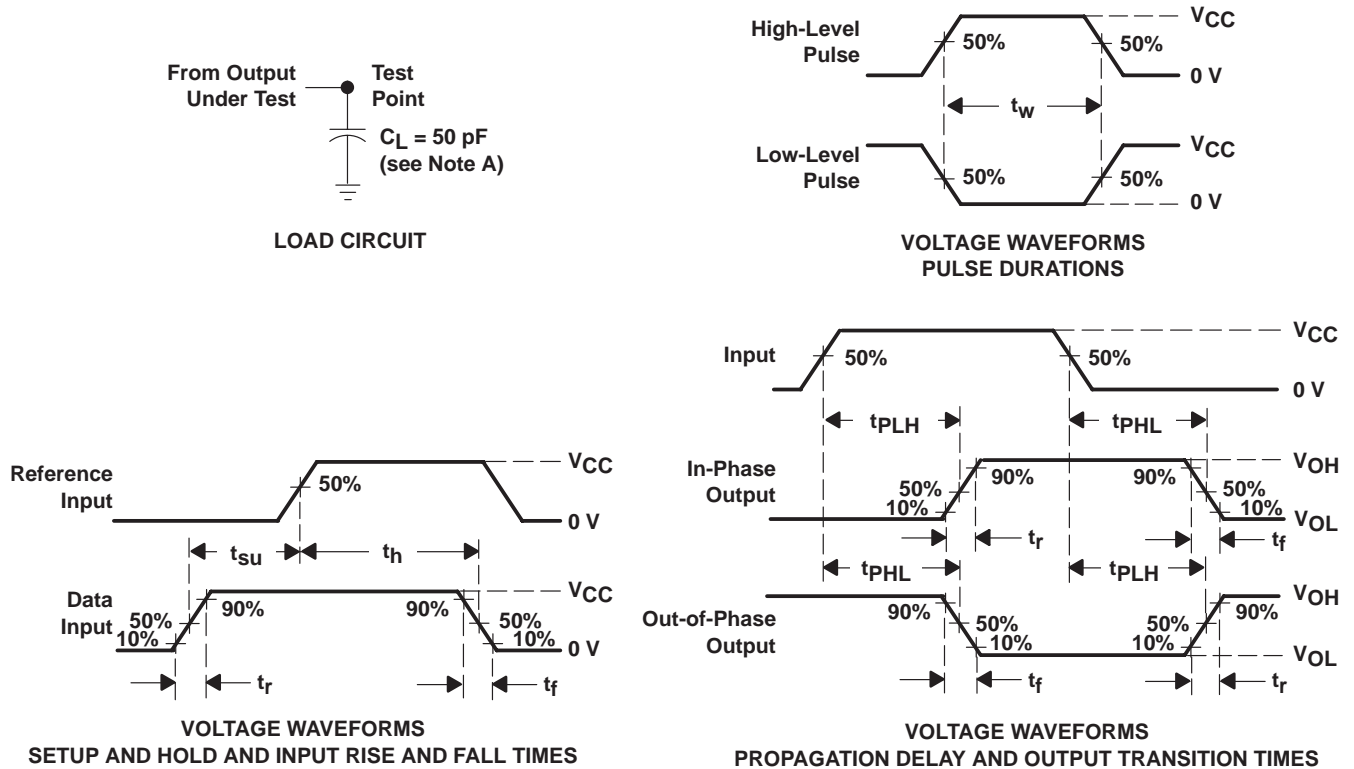
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC174		SN74HC174		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f <sub>max</sub>			2 V	6	9		4.2	5			MHz	
			4.5 V	31	44		21	25				
			6 V	36	50		25	29				
t <sub>pd</sub>	CLR	Any	2 V		58	160		240	200			ns
			4.5 V		17	32		48	40			
			6 V		14	27		41	34			
	CLK	Any	2 V		58	160		240	200			
			4.5 V		17	32		48	40			
			6 V		14	27		41	34			
t <sub>t</sub>		Any	2 V		38	75		110	90			ns
			4.5 V		8	15		22	19			
			6 V		6	13		19	16			

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per flip-flop	No load	27	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .  
 C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
84073012A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8407301EA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
8407301FA	ACTIVE	CFP	W	16	1	None	Call TI	Level-NC-NC-NC
JM38510/65307BEA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
SN54HC174J	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
SN74HC174D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC174DBR	ACTIVE	SSOP	DB	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC174DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
SN74HC174DT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC174N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74HC174NSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC174PW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74HC174PWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74HC174PWT	ACTIVE	TSSOP	PW	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SNJ54HC174FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54HC174J	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
SNJ54HC174W	ACTIVE	CFP	W	16	1	None	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

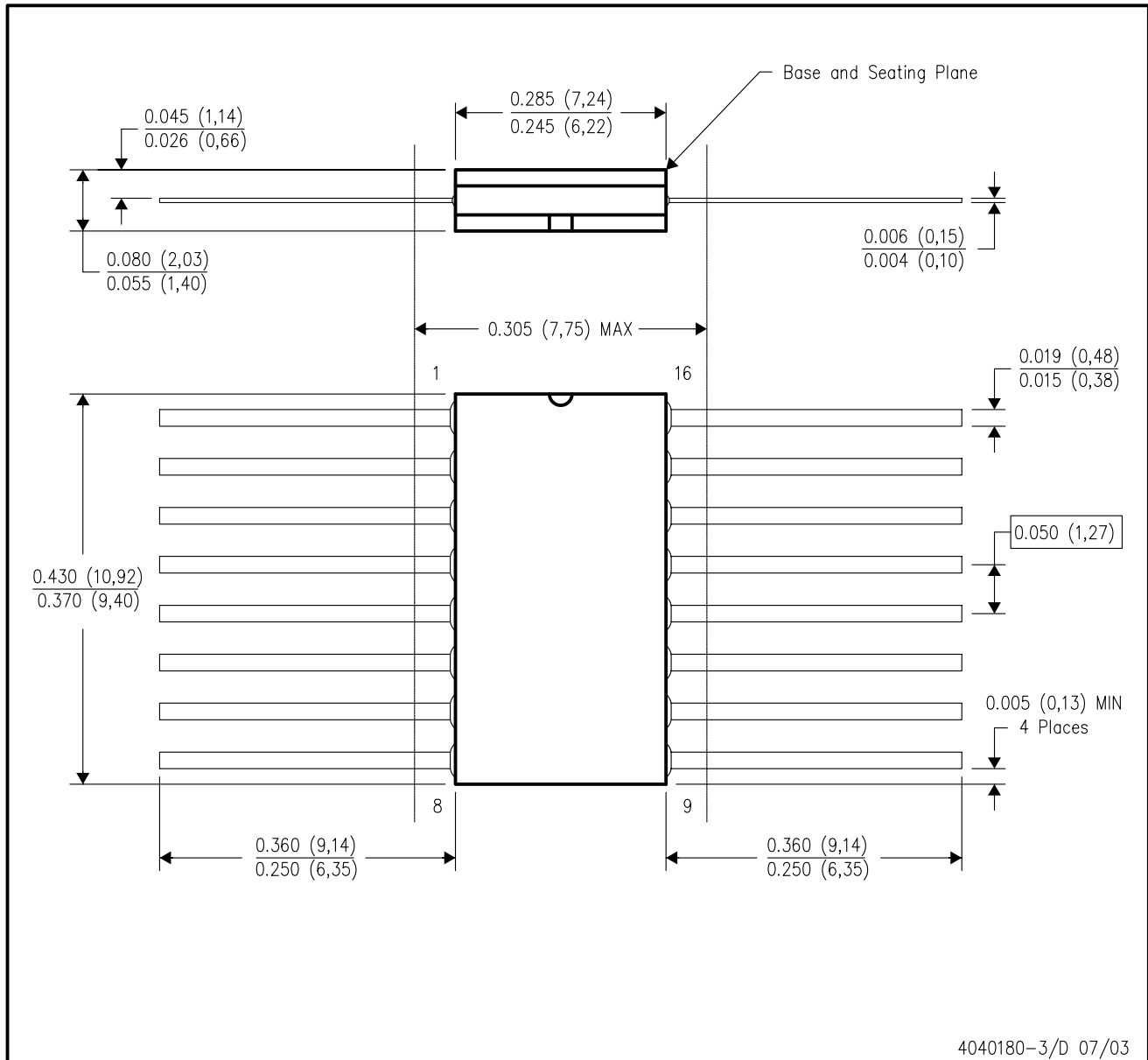


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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