

SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

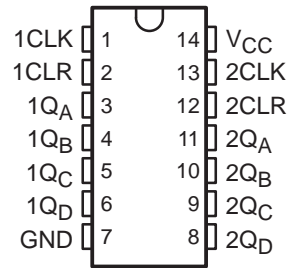
SCLS143D – DECEMBER 1982 – REVISED JULY 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 13$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Dual 4-Bit Binary Counters With Individual Clocks
- Direct Clear for Each 4-Bit Counter
- Can Significantly Improve System Densities by Reducing Counter Package Count by 50 Percent

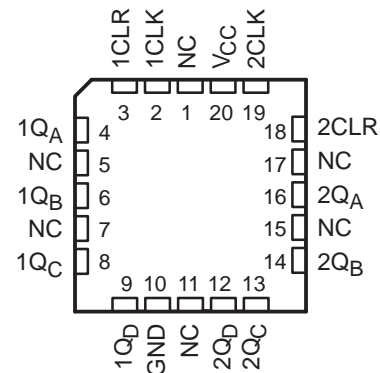
description/ordering information

The 'HC393 devices contain eight flip-flops and additional gating to implement two individual 4-bit counters in a single package. These devices comprise two independent 4-bit binary counters, each having a clear (CLR) and a clock (CLK) input. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The 'HC393 devices have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

SN54HC393 . . . J OR W PACKAGE
SN74HC393 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC393 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC393N | SN74HC393N |
| | SOIC – D | Tube of 50 | SN74HC393D | HC393 |
| | | Reel of 2500 | SN74HC393DR | |
| | | Reel of 250 | SN74HC393DT | |
| | SOP – NS | Reel of 2000 | SN74HC393NSR | HC393 |
| | SSOP – DB | Reel of 2000 | SN74HC393DBR | HC393 |
| -55°C to 125°C | TSSOP – PW | Tube of 90 | SN74HC393PW | HC393 |
| | | Reel of 2000 | SN74HC393PWR | |
| | | Reel of 250 | SN74HC393PWT | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC393J | SNJ54HC393J |
| | CFP – W | Tube of 150 | SNJ54HC393W | SNJ54HC393W |
| | LCCC – FK | Tube of 55 | SNJ54HC393FK | SNJ54HC393FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

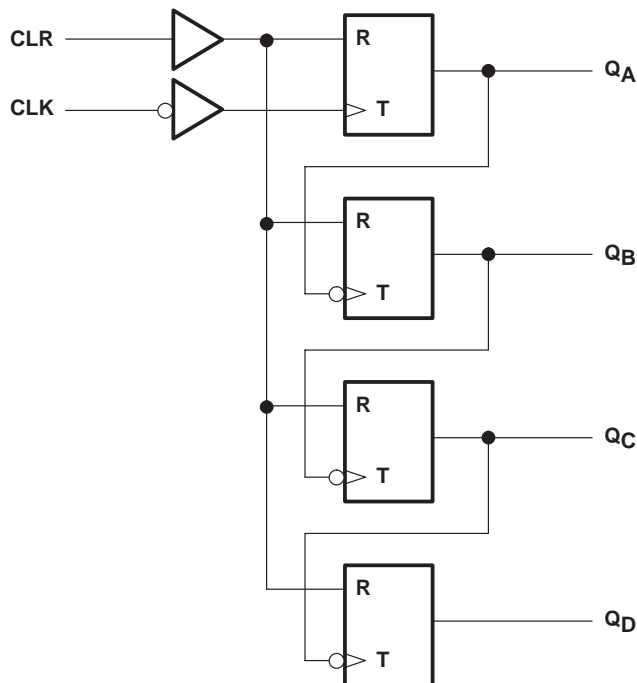
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FUNCTION TABLE COUNT SEQUENCE
(each counter)

| COUNT | OUTPUTS | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q _D | Q _C | Q _B | Q _A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

logic diagram, each counter (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| DB package | 96°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | SN54HC393 | | | SN74HC393 | | | UNIT |
|------------------------------|---------------------------------|------------------|-----|----------|------------------|-----|----------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | | 1.5 | $V_{CC} = 2$ V | | 1.5 | V |
| | | $V_{CC} = 4.5$ V | | 3.15 | $V_{CC} = 4.5$ V | | 3.15 | |
| | | $V_{CC} = 6$ V | | 4.2 | $V_{CC} = 6$ V | | 4.2 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | | $V_{CC} = 2$ V | | 0.5 | V |
| | | $V_{CC} = 4.5$ V | | | $V_{CC} = 4.5$ V | | 1.35 | |
| | | $V_{CC} = 6$ V | | | $V_{CC} = 6$ V | | 1.8 | |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| $\Delta t/\Delta v^\ddagger$ | Input transition rise/fall time | $V_{CC} = 2$ V | | | $V_{CC} = 2$ V | | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | | $V_{CC} = 4.5$ V | | 500 | |
| | | $V_{CC} = 6$ V | | | $V_{CC} = 6$ V | | 400 | |
| T_A | Operating free-air temperature | –55 | | 125 | –40 | | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

‡ If this device is used in the threshold region (from $V_{IL,max} = 0.5$ V to $V_{IH,min} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_f = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HC393 | | SN74HC393 | | UNIT | | |
|-----------------|---|---------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|----|----|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | | | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | | | |
| | | I _{OH} = -5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V | | |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | | | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | | | |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | | | |
| | | I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | | | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA | | |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | | | 8 | | 160 | 80 | μA | |
| C _i | | | 2 V to 6 V | | | | | | | 3 | 10 | 10 | pF |

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC393 | | SN74HC393 | | UNIT | |
|--------------------|--------------------------|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|----|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| f _{clock} | Clock frequency | 2 V | | 6 | | 4.2 | | 5 | MHz | |
| | | 4.5 V | | 31 | | 21 | | 25 | | |
| | | 6 V | | 36 | | 25 | | 28 | | |
| t _w | Pulse duration | CLK high or low | 2 V | | 80 | | 120 | | 100 | ns |
| | | | 4.5 V | | 16 | | 24 | | 20 | |
| | | | 6 V | | 14 | | 20 | | 18 | |
| | | CLR high | 2 V | | 80 | | 120 | | 100 | |
| | | | 4.5 V | | 16 | | 24 | | 20 | |
| | | | 6 V | | 14 | | 20 | | 18 | |
| t _{su} | Setup time, CLR inactive | 2 V | | 25 | | 25 | | 25 | ns | |
| | | 4.5 V | | 5 | | 5 | | 5 | | |
| | | 6 V | | 5 | | 5 | | 5 | | |



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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HC393 | | SN74HC393 | | UNIT |
|------------------|--------------|----------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | CLK | Q _A | 2 V | 6 | 10 | | 4.2 | | 5 | MHz | |
| | | | 4.5 V | 31 | 50 | | 21 | | 25 | | |
| | | | 6 V | 36 | 60 | | 25 | | 28 | | |
| t _{pd} | CLK | Q _A | 2 V | | 50 | 120 | | 180 | | 150 | ns |
| | | | 4.5 V | | 15 | 24 | | 36 | | 30 | |
| | | | 6 V | | 13 | 20 | | 31 | | 26 | |
| | | Q _B | 2 V | | 72 | 190 | | 285 | | 240 | |
| | | | 4.5 V | | 22 | 38 | | 57 | | 47 | |
| | | | 6 V | | 18 | 32 | | 48 | | 40 | |
| | | Q _C | 2 V | | 91 | 240 | | 360 | | 300 | |
| | | | 4.5 V | | 28 | 48 | | 72 | | 60 | |
| | | | 6 V | | 22 | 41 | | 61 | | 51 | |
| | | Q _D | 2 V | | 100 | 290 | | 430 | | 360 | |
| | | | 4.5 V | | 32 | 58 | | 87 | | 72 | |
| | | | 6 V | | 24 | 50 | | 74 | | 62 | |
| t _{PHL} | CLR | Any | 2 V | | 45 | 165 | | 250 | | 205 | ns |
| | | | 4.5 V | | 17 | 33 | | 49 | | 41 | |
| | | | 6 V | | 14 | 28 | | 42 | | 35 | |
| t _t | | Any | 2 V | | 28 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

operating characteristics, T_A = 25°C

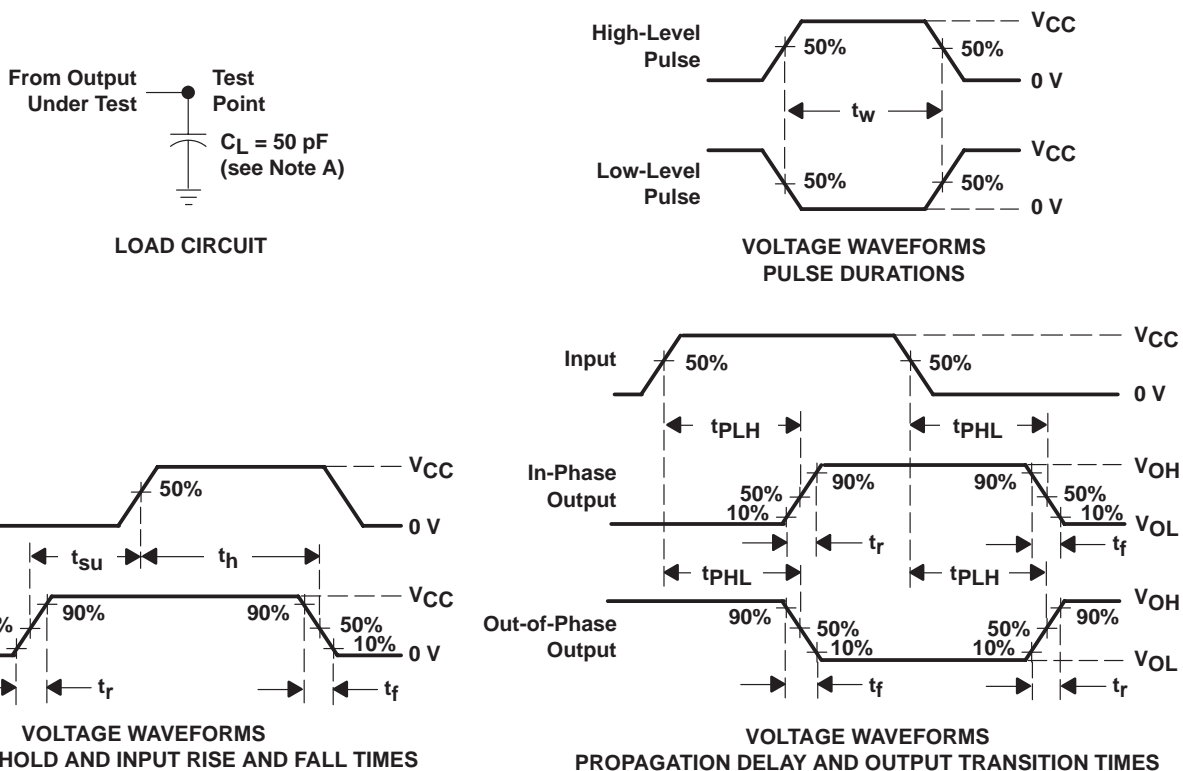
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------|-----|------|
| C _{pd} Power dissipation capacitance per counter | No load | 40 | pF |



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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| 84100012A | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| 8410001CA | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| 8410001DA | ACTIVE | CFP | W | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/66309BCA | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SN54HC393J | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SN74HC393D | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC393DBR | ACTIVE | SSOP | DB | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC393DR | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC393DT | ACTIVE | SOIC | D | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC393N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74HC393N3 | OBSOLETE | PDIP | N | 14 | | None | Call TI | Call TI |
| SN74HC393NSR | ACTIVE | SO | NS | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74HC393PW | ACTIVE | TSSOP | PW | 14 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HC393PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74HC393PWT | ACTIVE | TSSOP | PW | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SNJ54HC393FK | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54HC393J | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54HC393W | ACTIVE | CFP | W | 14 | 1 | None | Call TI | Level-NC-NC-NC |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

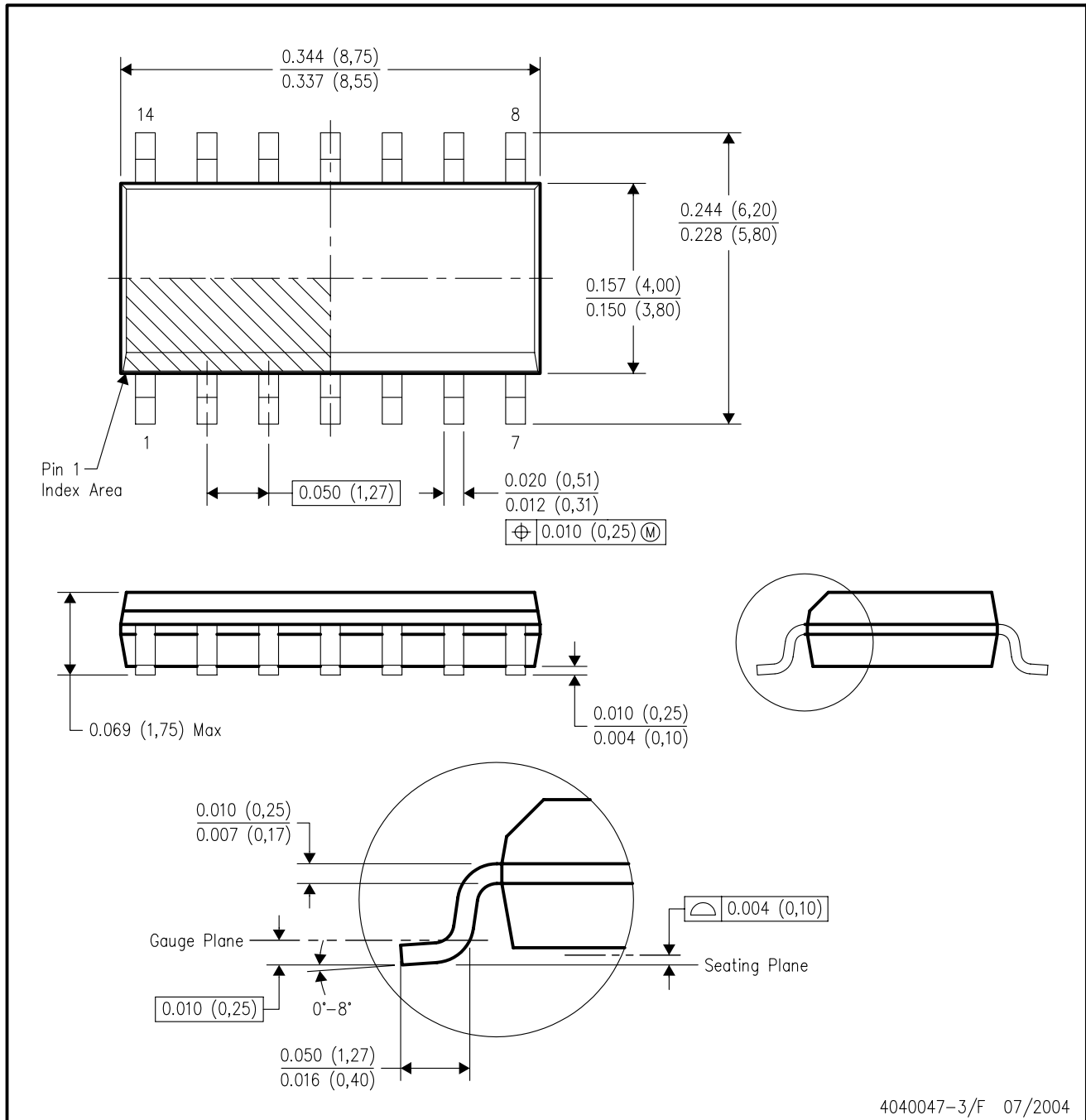
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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