

CD40109B Types

CMOS Quad Low-to-High Voltage Level Shifter

High-Voltage Types (20-Volt Rating)

■ CD40109B contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a higher-voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS} .

The CD40109, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD} , V_{CC} , or the input signals. In addition, with one exception there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings, provided that the input signal swings between V_{SS} and at least 0.7 V_{CC} ; V_{CC} may exceed V_{DD} , and input signals may exceed V_{CC} and V_{DD} . When operated in the mode $V_{CC} > V_{DD}$, the CD40109 will operate as a high-to-low level-shifter.

The CD40109 also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

The CD40109B-Series types are supplied in 16-lead ceramic dual-in-line packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Applications:

- High-or-low level-shifting with three-state outputs for unidirectional or bidirectional bussing
- Isolation of logic subsystems using separate power supplies from supply sequencing, supply loss and supply regulation considerations

Features:

- Independence of power supply sequence considerations— V_{CC} can exceed V_{DD} , input signals can exceed both V_{CC} and V_{DD}
- Up and down level-shifting capability
- Three-state outputs with separate enable controls
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range)
 - 1 V at $V_{CC} = 5 V$, $V_{DD} = 10 V$
 - 2 V at $V_{CC} = 10 V$, $V_{DD} = 15 V$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	Voltages referenced to V_{SS} Terminal)	–0.5V to +20V
OUTPUT VOLTAGE RANGE, ALL OUTPUTS		–0.5 V to $V_{DD} + 0.5 V$
DC INPUT CURRENT, ANY ONE INPUT		$\pm 10mA$
POWER DISSIPATION PER PACKAGE (P_D):		
For $T_A = -55^\circ C$ to $+100^\circ C$		500mW
For $T_A = +100^\circ C$ to $+125^\circ C$		Derate Linearly at 12mW/ $^\circ C$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)		100mW
OPERATING-TEMPERATURE RANGE (T_A)		–55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})		–65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max		+265°C

TRUTH TABLE		
INPUTS		OUTPUTS
A, B, C, D	ENABLE A, B, C, D	E, F, G, H
0	1	0
1	1	1
X	0	Z

LOGIC 0 = LOW(V_{SS}) X = DON'T CARE Z = HIGH IMPEDANCE
LOGIC 1 = V_{CC} at INPUTS and V_{DD} at OUTPUTS

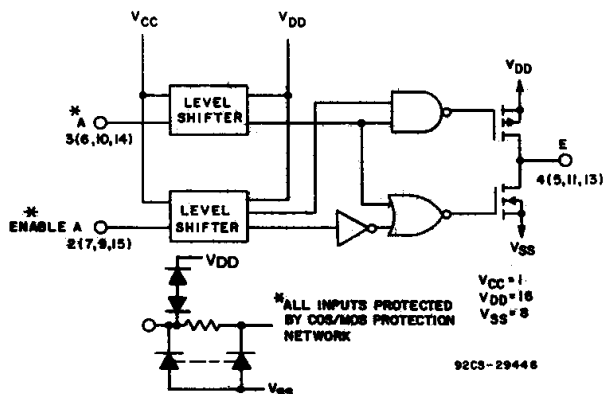
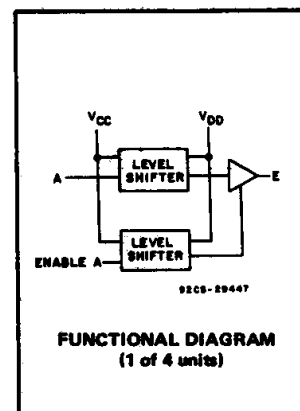


Fig. 1 – CD40109B logic diagram (1 of 4 units).

CD40109B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Current I _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA
3-State Output Leakage Current I _{OUT} Max.		0,18	18	±0.4	±0.4	±12	±12	—	±10 ⁻⁴	±0.4	μA
	V _O (V)	V _{CC} (V)	V _{DD} (V)								
Input Low Voltage, V _{IL} Max.	1,9	5	10	1.5				—	—	1.5	V
	1.5, 13.5	10	15	3				—	—	3	
Input High Voltage, V _{IH} Min.	1,9	5	10	3.5				3.5	—	—	V
	1.5, 13.5	10	15	7				7	—	—	

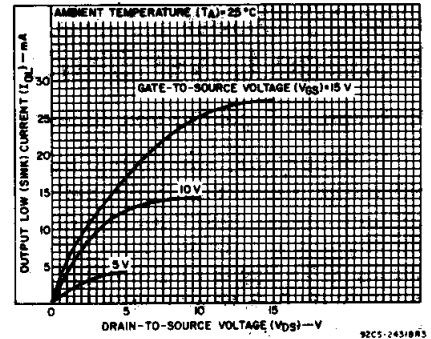


Fig.2 - Typical output low (sink) current characteristics.

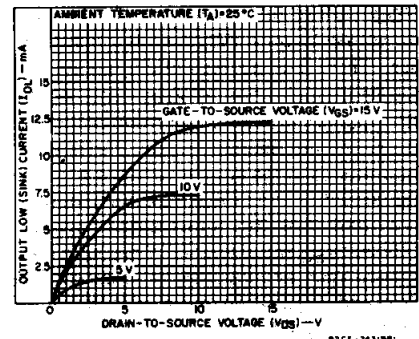


Fig.3 - Minimum output low (sink) current characteristics.

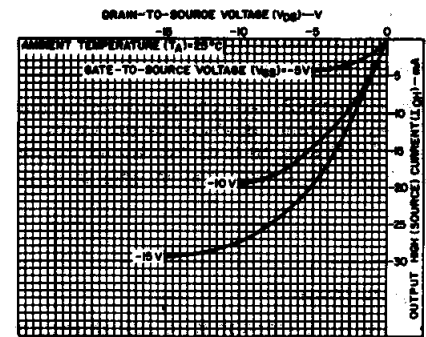


Fig.4 - Typical output high (source) current characteristics.

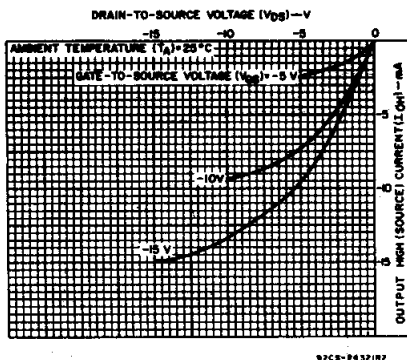


Fig.5 - Minimum output high (source) current characteristics.

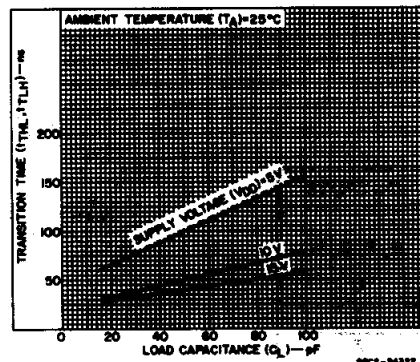


Fig.6 - Typical transition time as a function of load capacitance.

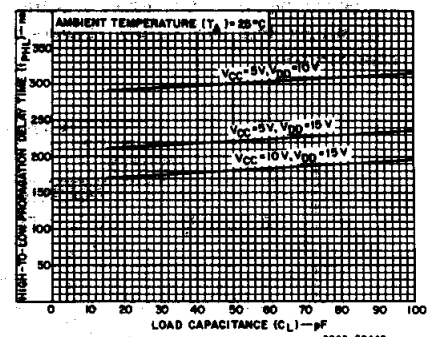


Fig.7 - Typical high-to-low propagation delay time as a function of load capacitance.

CD40109B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$ unless otherwise specified

CHARACTERISTIC	SHIFTING MODE	VCC (V)	VDD (V)	LIMITS		UNITS
				Typ.	Max.	
Propagation Delay — Data Input to Output: High-to-Low Level, t_{PHL}	L—H	5	10	300	600	ns
		5	15	220	440	
		10	15	180	360	
	H—L	10	5	250	500	ns
		15	5	250	500	
		15	10	120	240	
Low-to-High Level, t_{PLH}	L—H	5	10	130	260	ns
		5	15	120	240	
		10	15	70	140	
	H—L	10	5	230	460	ns
		15	5	230	460	
		15	10	80	160	
3-State Disable Delay: $R_L = 1 \text{ k}\Omega$ Output High to High Impedance, t_{PHZ}	L—H	5	10	60	120	ns
		5	15	75	150	
		10	15	35	70	
	H—L	10	5	200	400	ns
		15	5	200	400	
		15	10	40	80	
Output Low to High Impedance, t_{PLZ}	L—H	5	10	370	740	ns
		5	15	300	600	
		10	15	250	500	
	H—L	10	5	250	500	ns
		15	5	250	500	
		15	10	130	260	
High Impedance to Output High, t_{pZH}	L—H	5	10	320	640	ns
		5	15	230	460	
		10	15	180	360	
	H—L	10	5	300	600	ns
		15	5	300	600	
		15	10	130	260	
High Impedance to Output Low, t_{pZL}	L—H	5	10	100	200	ns
		5	15	80	160	
		10	15	40	80	
	H—L	10	5	200	400	ns
		15	5	200	400	
		15	10	40	80	
Transition Time, t_{THL}, t_{TLH}	L—H	5	10	50	100	ns
		5	15	40	80	
		10	15	40	80	
	H—L	10	5	100	200	ns
		15	5	100	200	
		15	10	50	100	
Input Capacitance, C_i			Any Input	5	7.5	pF

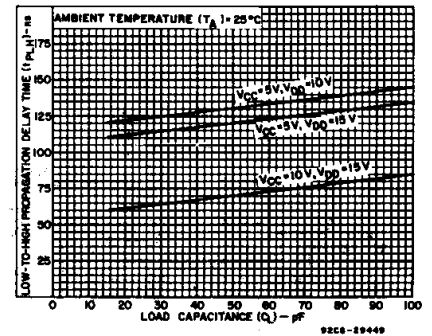


Fig. 8 — Typical low-to-high propagation delay time as a function of load capacitance.

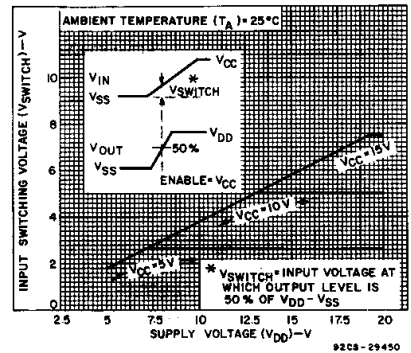


Fig. 9 — Typical input switching as a function of high-level supply voltage.

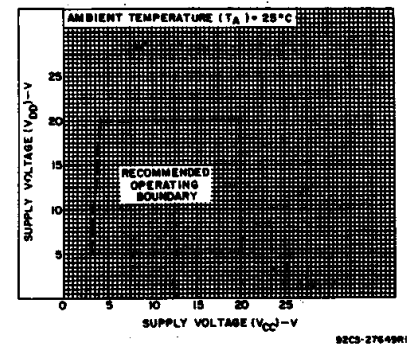


Fig. 10 — High-level supply voltage vs. low-level supply voltage.

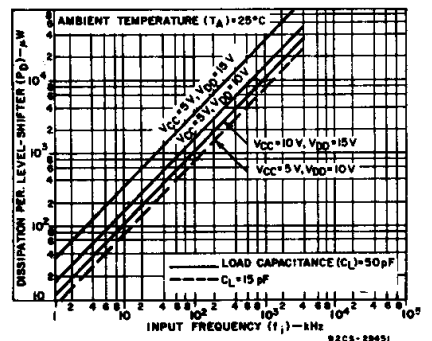


Fig. 11 — Typical dynamic power dissipation as a function of input frequency.

CD40109B Types

TEST CIRCUITS

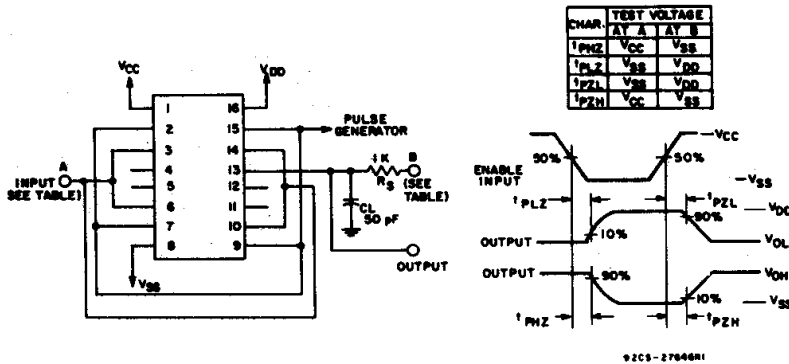


Fig. 12 - Output enable delay times test circuit and waveforms.

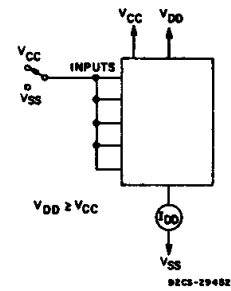


Fig. 13 - Quiescent device current.

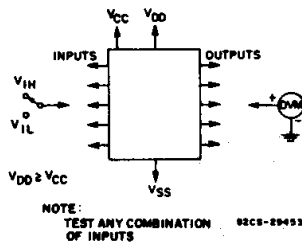


Fig. 14 - Input voltage.

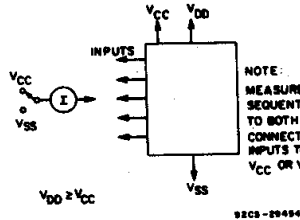


Fig. 15 - Input current.

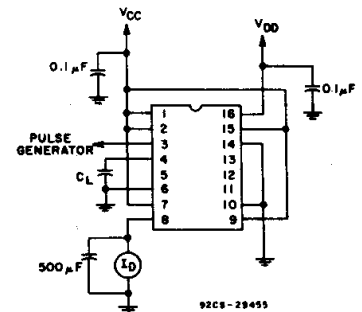
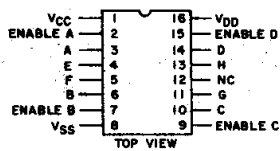
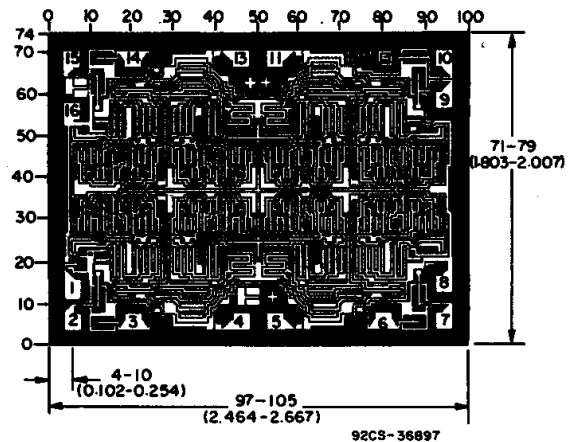


Fig. 16 - Dynamic power dissipation test circuit.



CD40109B TERMINAL ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Dimensions and pad layout for CD40109BH.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD40109BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40109BE	Samples
CD40109BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD40109BE	Samples
CD40109BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40109BF	Samples
CD40109BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD40109BF3A	Samples
CD40109BK3	OBSOLETE	CFP	WR	16		TBD	Call TI	Call TI	-55 to 125		
CD40109BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40109B	Samples
CD40109BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40109B	Samples
CD40109BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40109B	Samples
CD40109BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples
CD40109BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples
CD40109BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples
CD40109BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples
CD40109BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples
CD40109BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0109B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

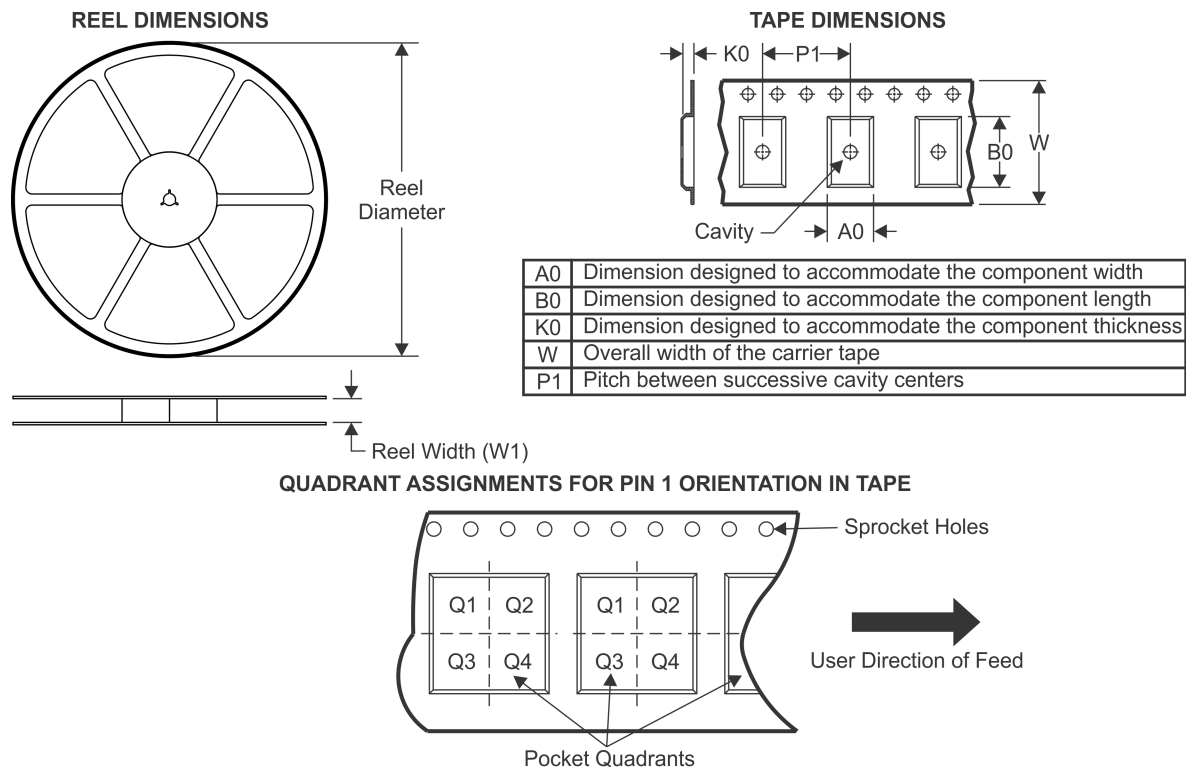
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD40109B, CD40109B-MIL :

- Catalog: [CD40109B](#)
- Automotive: [CD40109B-Q1](#), [CD40109B-Q1](#)
- Military: [CD40109B-MIL](#)

NOTE: Qualified Version Definitions:

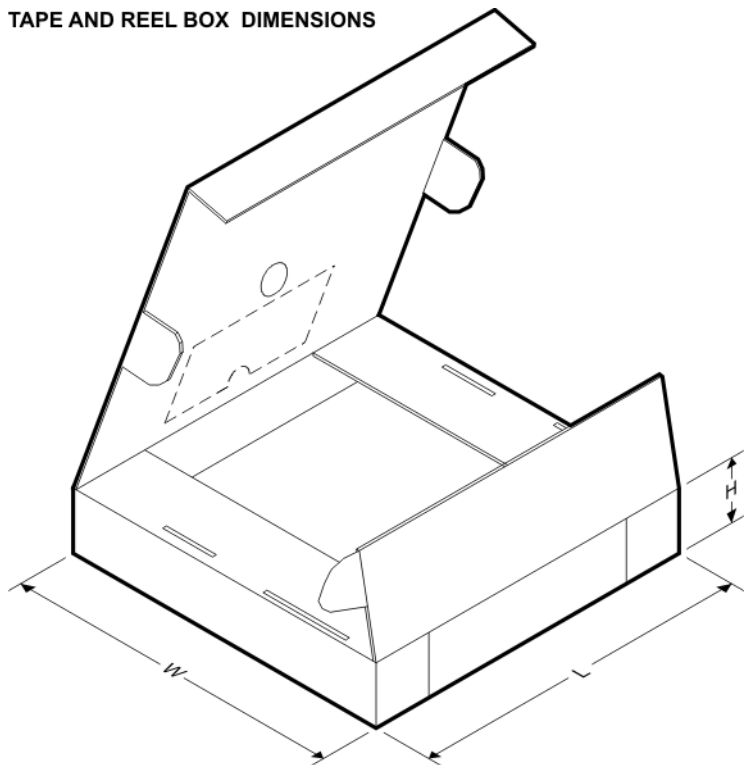
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40109BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



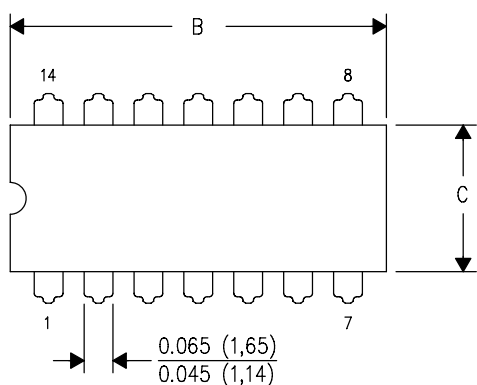
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40109BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

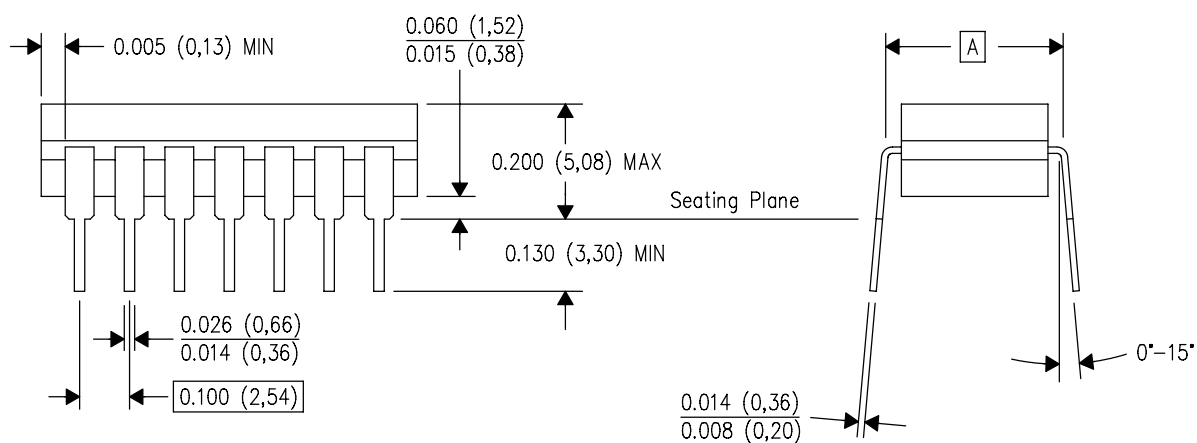
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



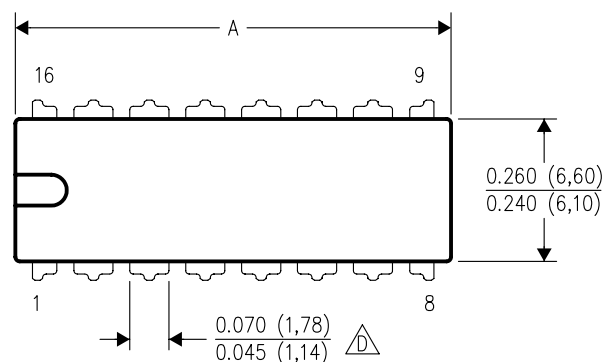
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

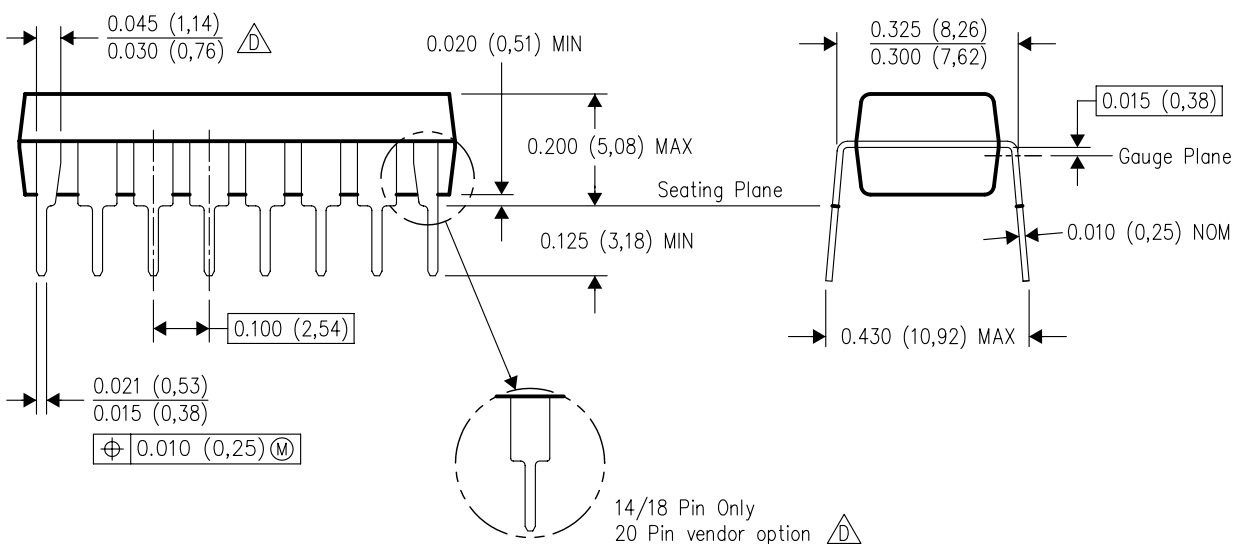
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

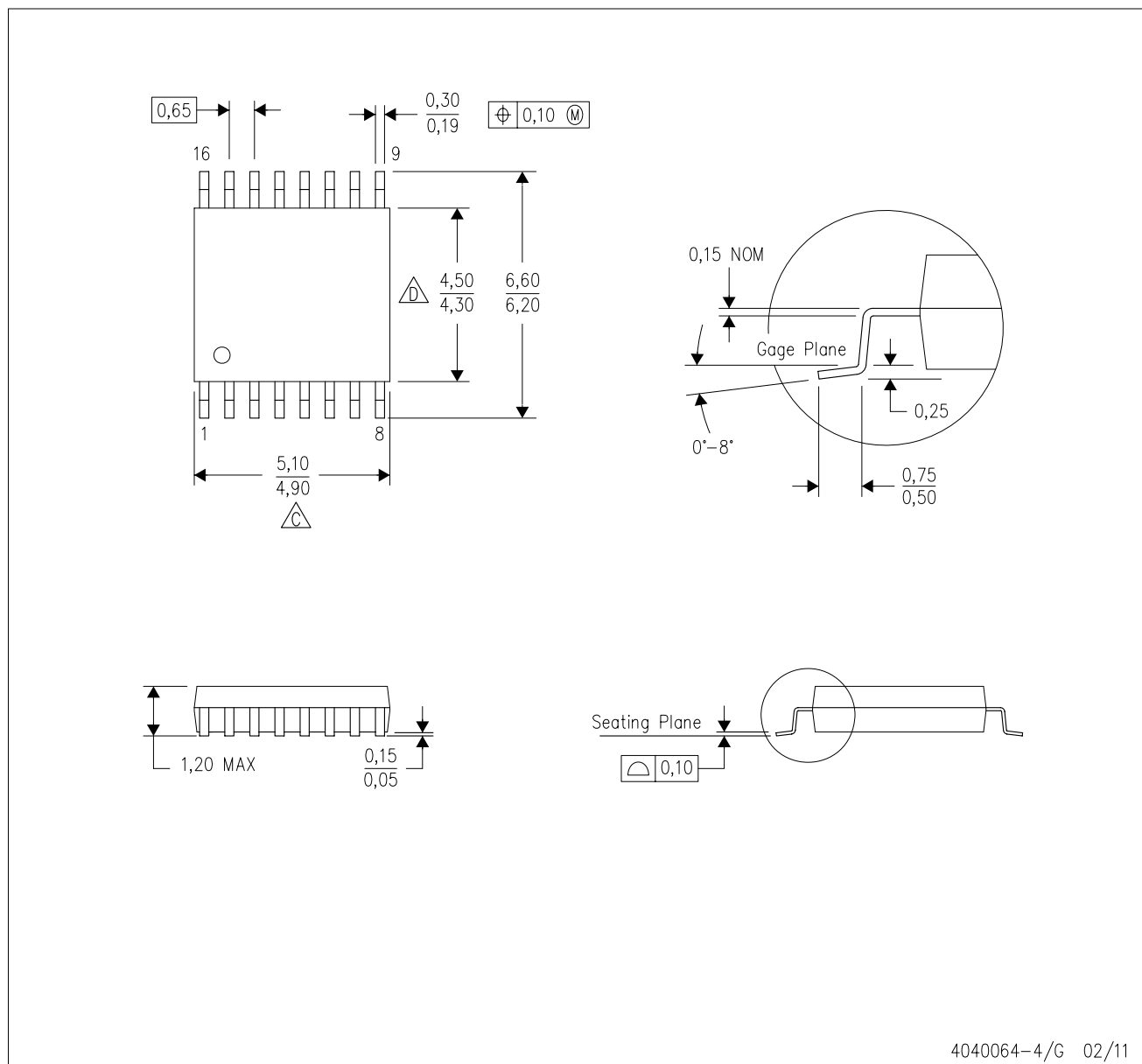


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G16)

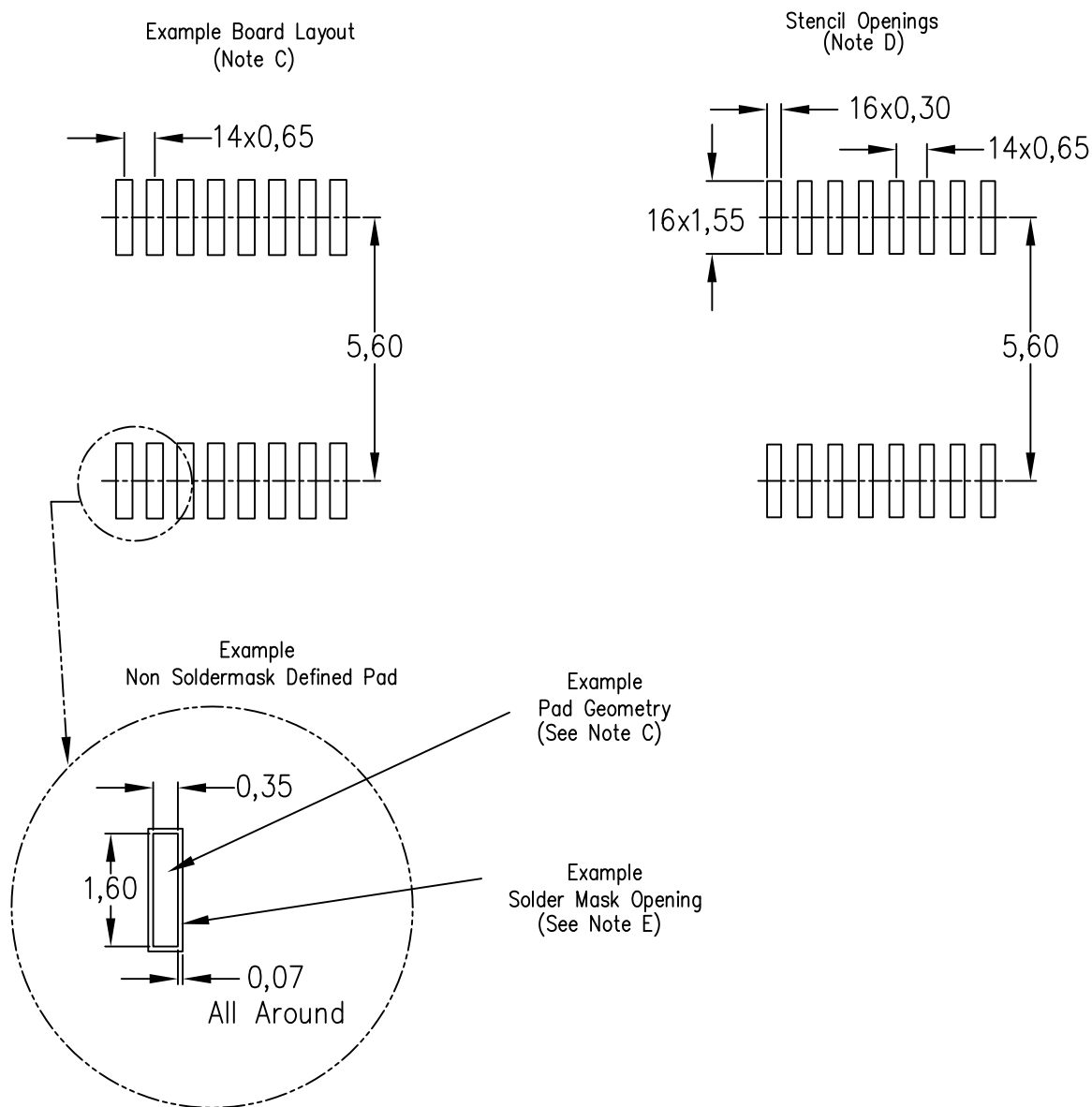
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

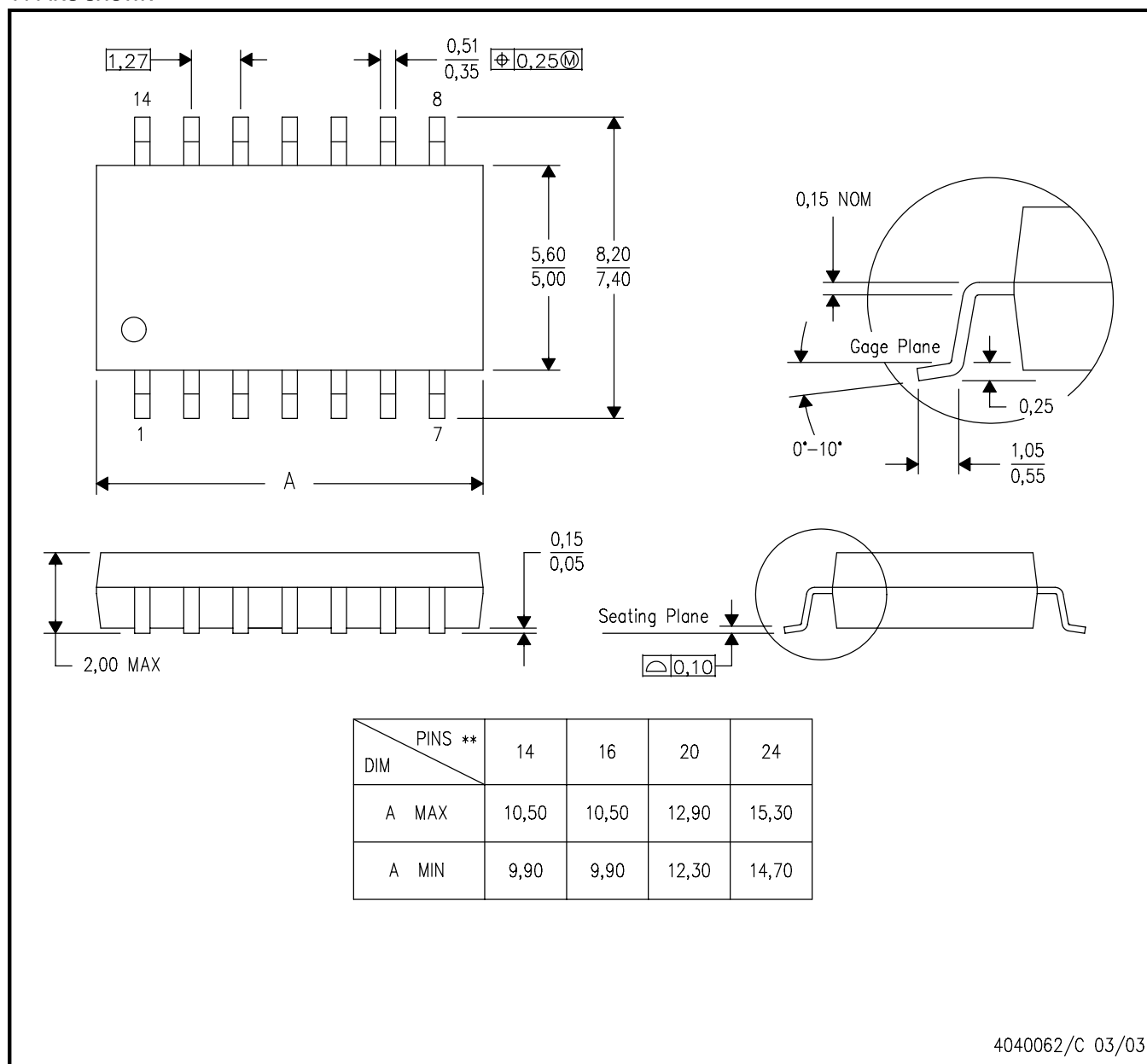
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com