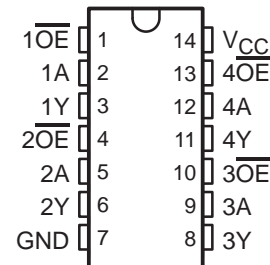


# CD74HC125-Q1 HIGH-SPEED CMOS LOGIC QUAD BUFFER WITH 3-STATE OUTPUTS

SCLS579 – APRIL 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- 3-State Outputs
- Separate Output Enable Inputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . 15 LSTTL Loads
- Extended Temperature Performance of –40°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction, Compared to LSTTL Logic ICs
- 2-V to 6-V  $V_{CC}$  Operation
- High Noise Immunity  $N_{IL}$  or  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$

M OR PW PACKAGE  
(TOP VIEW)



† Contact factory for details. Q100 qualification data available on request.

## description/ordering information

The CD74HC125 contains four independent 3-state buffers, each having its own output enable input which, when HIGH, puts the output in the high-impedance state.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Reel of 2500	CD74HC125QM96Q1	HC125Q
	TSSOP – PW	Reel of 2000	CD74HC125QPWRQ1	HC125Q

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	$\overline{\text{OE}}$	Y
H	L	H
L	L	L
X	H	Z



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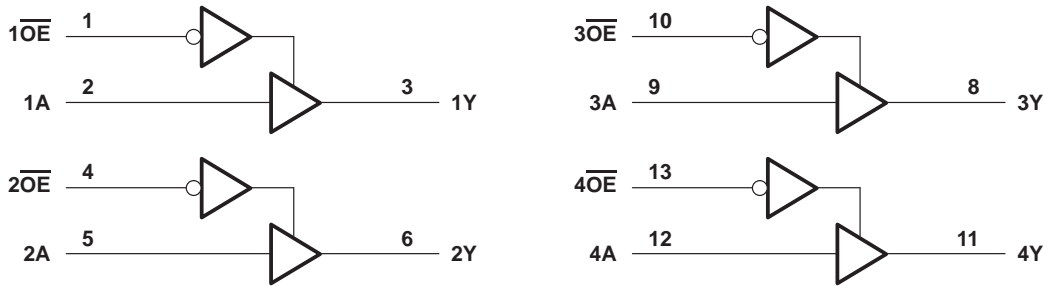
# CD74HC125-Q1

## HIGH-SPEED CMOS LOGIC

### QUAD BUFFER WITH 3-STATE OUTPUTS

SCLS579 – APRIL 2004

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O > -0.5$ or $V_O < V_{CC} + 0.5$ V)	±35 mA
Output source or sink current per output pin, $I_O$ ( $V_O > -0.5$ or $V_O < V_{CC} + 0.5$ V)	±25 mA
Continuous current through $V_{CC}$ or GND	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): M package	86°C/W
PW package	113°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V		1.8	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$t_t$	Input transition rise/fall time	$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		400	
$T_A$	Operating free-air temperature	–40		125	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**CD74HC125-Q1**  
**HIGH-SPEED CMOS LOGIC**  
**QUAD BUFFER WITH 3-STATE OUTPUTS**

SCLS579 – APRIL 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I <sub>O</sub> (mA)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	-0.02	2 V	1.9		1.9	V		
			-0.02	4.5 V	4.4	4.4				
			-0.02	6 V	5.9	5.9				
		TTL loads	-6	4.5 V	3.98	3.7				
			-7.8	6 V	5.48	5.2				
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	0.02	2 V		0.1	0.1			
			0.02	4.5 V		0.1	0.1			
			0.02	6 V		0.1	0.1			
		TTL loads	6	4.5 V		0.26	0.4			
			7.8	6 V		0.26	0.4			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		6 V			±0.1	±1	μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		6 V			8	160	μA		
I <sub>OZ</sub>	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		6 V			±0.5	±10	μA		
C <sub>I</sub>						10	10	pF		
C <sub>O</sub>	3-state					20	20	pF		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF	5 V		8			ns	
				2 V		100	150			
			C <sub>L</sub> = 50 pF	4.5 V		20	30			
				6 V		17	26			
t <sub>en</sub>	$\overline{\text{OE}}$	Y	C <sub>L</sub> = 15 pF	5 V		10		ns		
				2 V		125	190			
			C <sub>L</sub> = 50 pF	4.5 V		25	38			
				6 V		21	32			
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	C <sub>L</sub> = 15 pF	5 V		10		ns		
				2 V		125	190			
			C <sub>L</sub> = 50 pF	4.5 V		25	38			
				6 V		21	32			
t <sub>t</sub>		Y	C <sub>L</sub> = 50 pF	2 V			60	90	ns	
				4.5 V			12	18		
				6 V			10	15		



# CD74HC125-Q1

## HIGH-SPEED CMOS LOGIC

### QUAD BUFFER WITH 3-STATE OUTPUTS

SCLS579 – APRIL 2004

operating characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per gate (see Note 4)	No load	29	pF

NOTE 4:  $C_{pd}$  is used to determine the dynamic power consumption, per channel.

$$P_D = V_{CC}^2 f_I (C_{pd} + C_L)$$

$f_I$  = input frequency

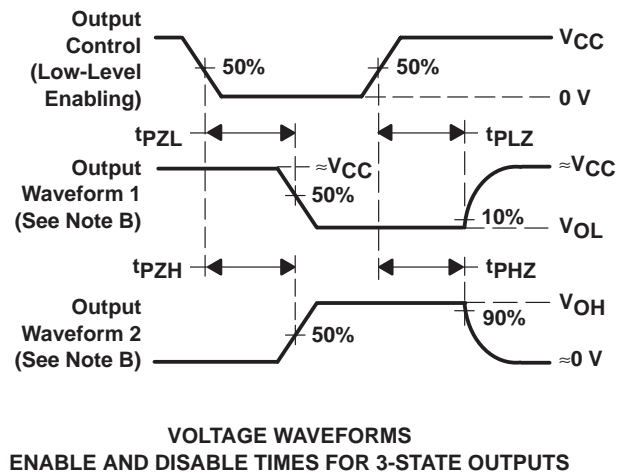
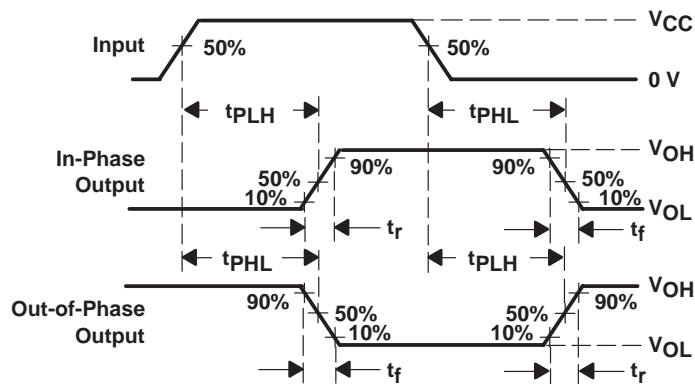
$C_L$  = output load capacitance

$V_{CC}$  = supply voltage

**PARAMETER MEASUREMENT INFORMATION**



PARAMETER	$R_L$	$C_L$	S1	S2	
$t_{en}$	$t_{PZH}$	1 k $\Omega$	50 pF	Open	Closed
	$t_{PZL}$			Closed	Open
$t_{dis}$	$t_{PHZ}$	1 k $\Omega$	50 pF	Open	Closed
	$t_{PLZ}$			Closed	Open
$t_{pd}$ or $t_t$	--	50 pF	Open	Open	

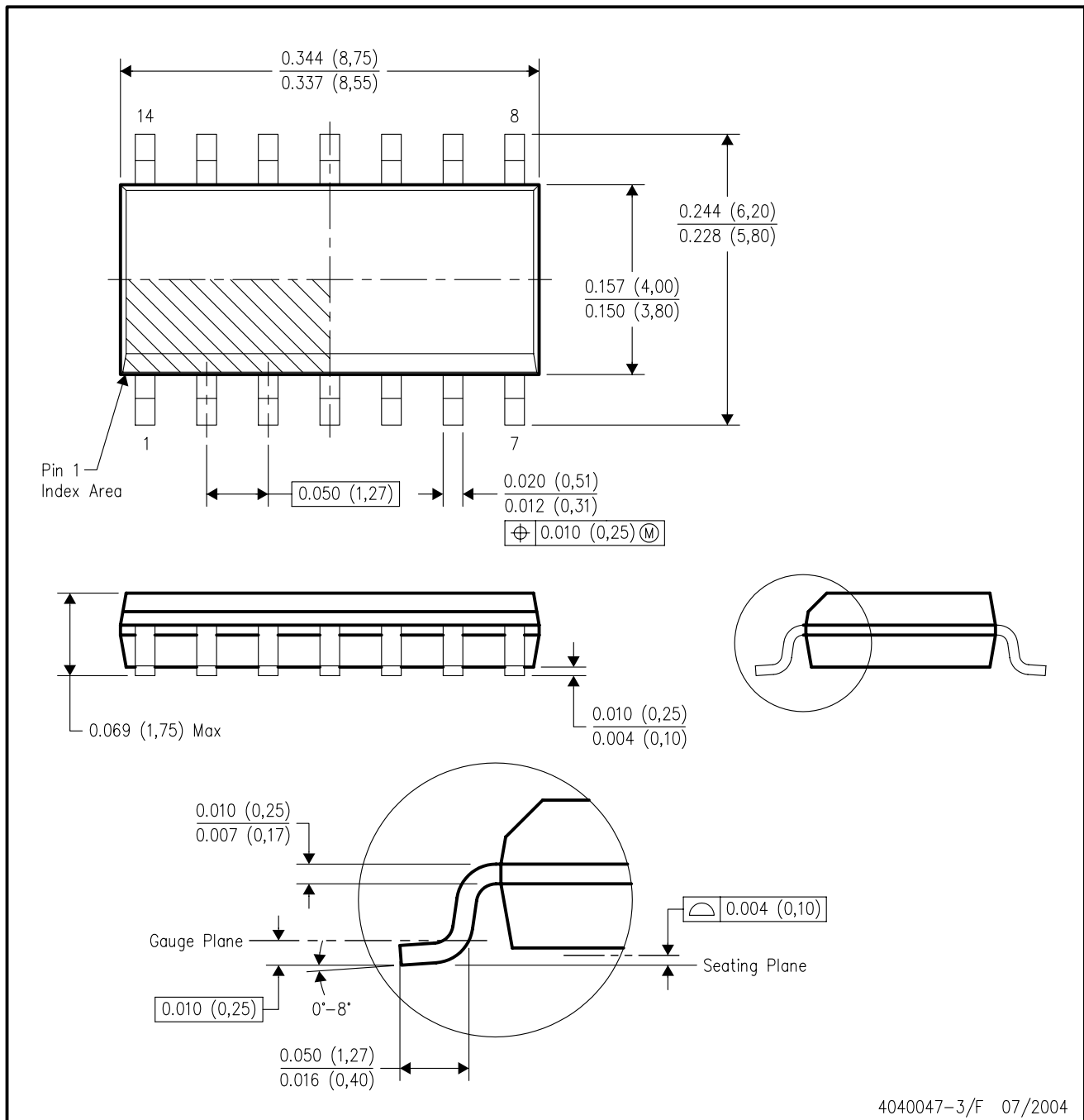


- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

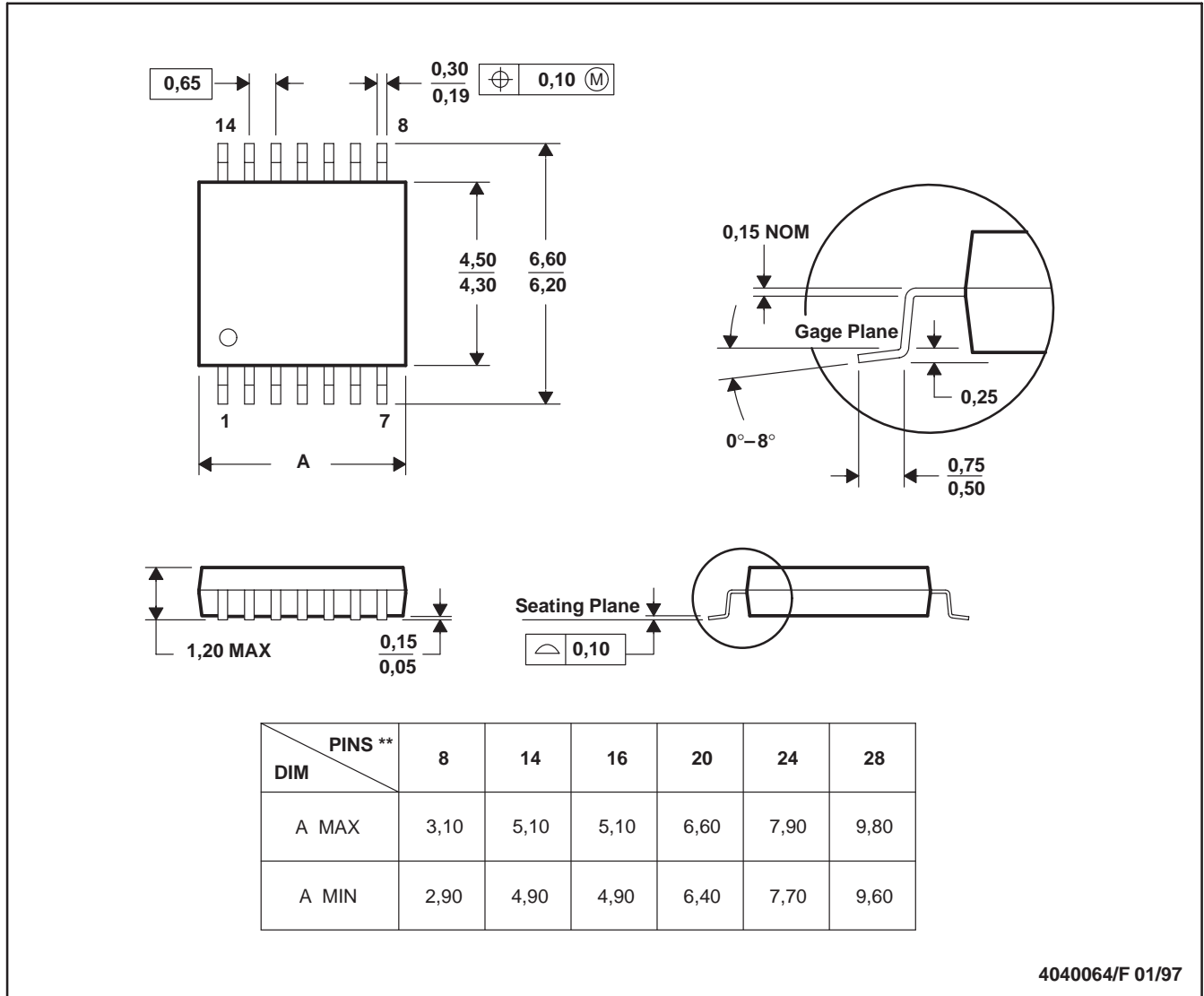


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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