LF444QML Quad Low Power JFET Input Operational Amplifier

Check for Samples: LF444QML

FEATURES

- **1/4 Supply Current of a LM148: 250 µA/Amplifier (Max)**
- **Low Input Bias Current: 100 pA (max)**
- **High Gain Bandwidth: 1 MHz**
- **High Slew Rate: 1 V/µs**
- **Low Noise Voltage for Low Power 35 nV/$\sqrt{Hz}$**
- **Low Input Noise Current 0.01 pA/$\sqrt{Hz}$**
- **High Input Impedance: $10^{12}\Omega$**
- **High Gain, V_O = ±10V, R_L = 10kΩ: 25K (Min)**

DESCRIPTION

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Connection Diagram

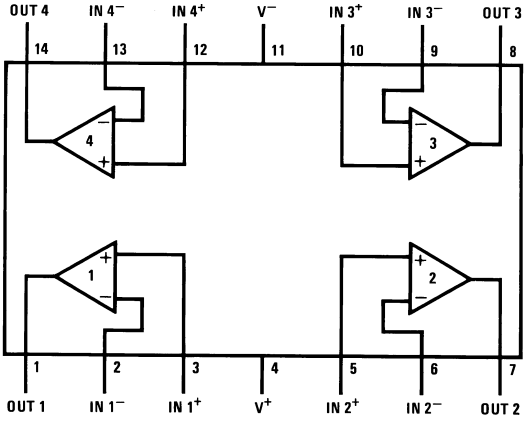


Figure 1. CDIP - Top View
See Package Number NAK0014D

Simplified Schematic

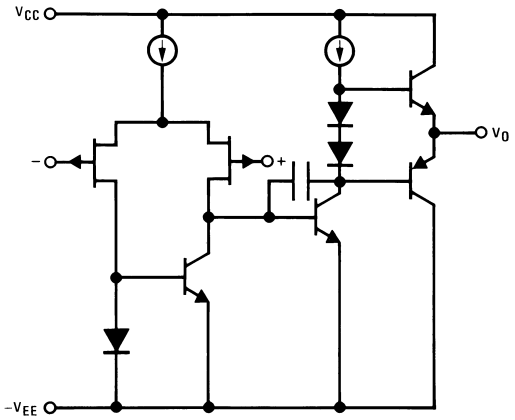


Figure 2. 1/4 Quad

Detailed Schematic

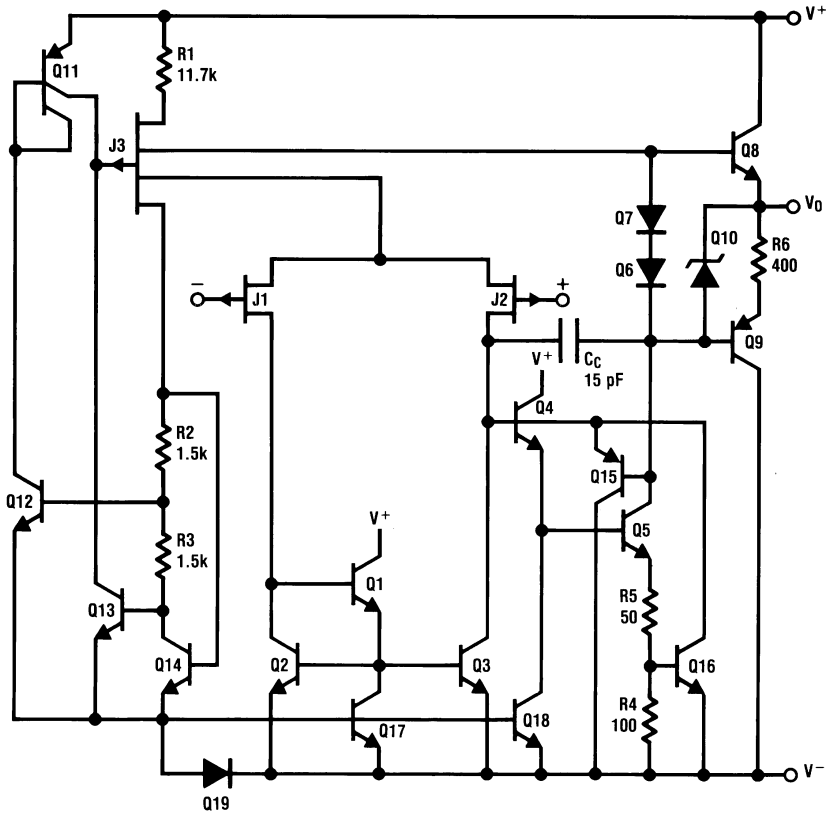


Figure 3. 1/4 Quad

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range(2)	±15V
Output Short Circuit Duration(3)	Continuous
Power Dissipation(4)(5)	900 mW
T_{Jmax}	150°C
θ_{JA} (Typical)	100°C/W
Operating Temperature Range	$-55°C \le T_A \le 125°C$
Storage Temperature Range	$-65°C \le T_A \le 150°C$
ESD Tolerance(6)	Rating to be determined

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(5) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside specified limits.
(6) Human body model, 1.5 kΩ in series with 100 pF.

Table 1. QUALITY CONFORMANCE INSPECTION

Mil-Std-883, Method 5005 - Group A		
Subgroup	**Description**	**Temp (°C)**
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LF444 ELECTRICAL CHARACTERISTICS DC PARAMETERS

The following conditions apply, unless otherwise specified. V_S = ±15V, V_{CM} = 0V, R_S = 0Ω, R_L = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	R_S = 10KΩ		-10	10	mV	1
				-14	14	mV	2, 3
I_{IO}	Input Offset Current	R_L = 10KΩ		-0.05	0.05	nA	1
				-10	10	nA	2
$+I_{IB}$	Input Bias Current	R_L = 10KΩ		-0.10	0.10	nA	1
				-20	20	nA	2
$-I_{IB}$	Input Bias Current	R_L = 10KΩ		-0.10	0.10	nA	1
				-20	20	nA	2
$+A_{VS}$	Large Signal Voltage Gain	V_O = 0 to +10V, R_L = 10KΩ, R_S = 10KΩ	See (1)	25		V/mV	1
				15		V/mV	2, 3
$-A_{VS}$	Large Signal Voltage Gain	V_O = 0 to -10V, R_L = 10KΩ, R_S = 10KΩ	See (1)	25		V/mV	1
				15		V/mV	2, 3
$+V_O$	Output Voltage Swing	R_L = 10KΩ, V_I = +1V		12		V	1, 2, 3
$-V_O$	Output Voltage Swing	R_L = 10KΩ, V_I = -1V			-12	V	1, 2, 3
V_{CM}	Input Common Mode Voltage Range		See (2)	9	-9	V	1, 2, 3
CMRR	Common Mode Rejection Ratio	R_S = 10KΩ, V_{CM} = ±9V		70		dB	1, 2, 3
PSRR+	Power Supply Rejection Ratio	V_S = ±15V to V_S = ±6V		70		dB	1, 2, 3
PSRR-	Power Supply Rejection Ratio	V_S = ±15V to V_S = ±6V		70		dB	1, 2, 3
I_S	Supply Current				1.0	mA	1, 2, 3
$+I_{OS}$	Output Short Circuit Current	V_I = 1V		-3.0	-20	mA	1
				-3.0	-40	mA	2, 3
$-I_{OS}$	Output Short Circuit Current	V_I = -1V		3.0	20	mA	1
				3.0	40	mA	2, 3

(1) Datalog in K = V/mV.
(2) Parameter tested go-no-go only. Specified by the CMRR test.

TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current

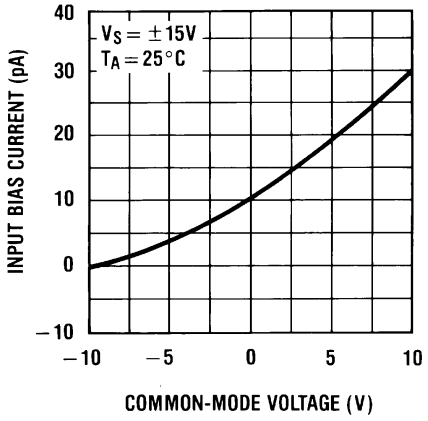


Figure 4.

Input Bias Current

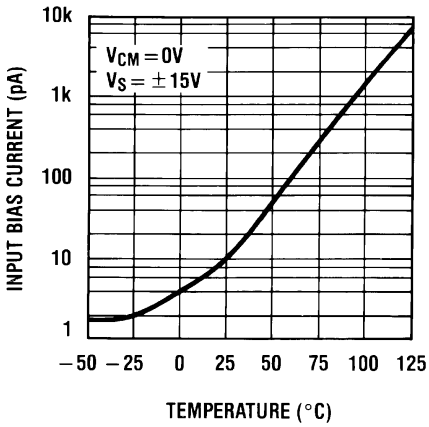


Figure 5.

Supply Current

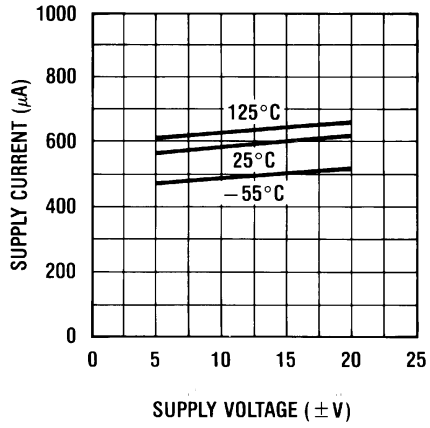


Figure 6.

Positive Common-Mode Input Voltage Limit

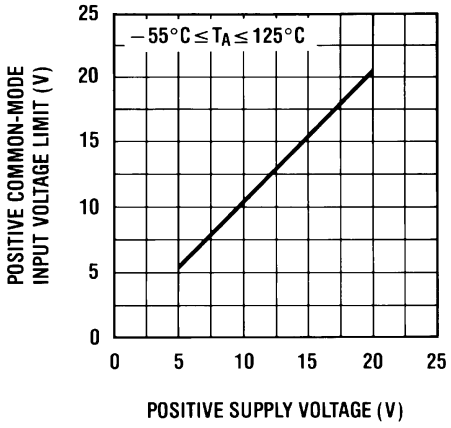


Figure 7.

Negative Common-Mode Input Voltage Limit

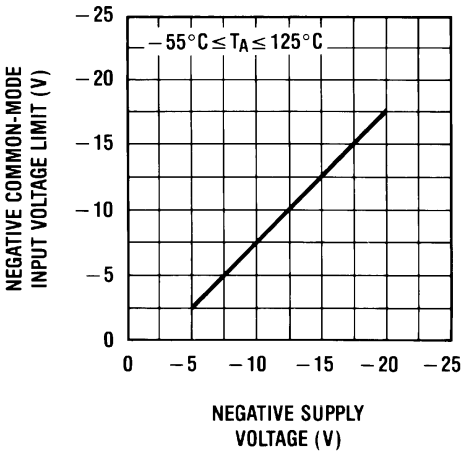


Figure 8.

Positive Current Limit

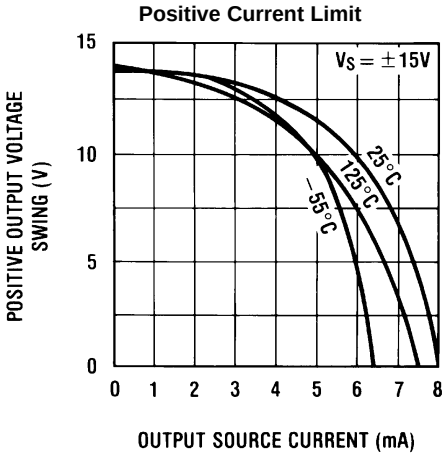


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Negative Current Limit

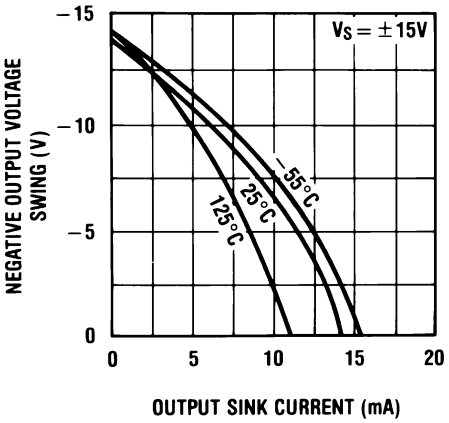


Figure 10.

Output Voltage Swing

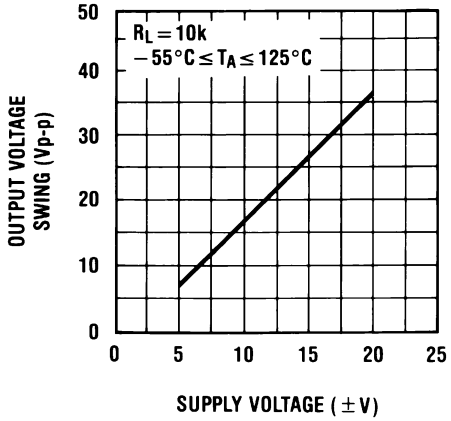


Figure 11.

Output Voltage Swing

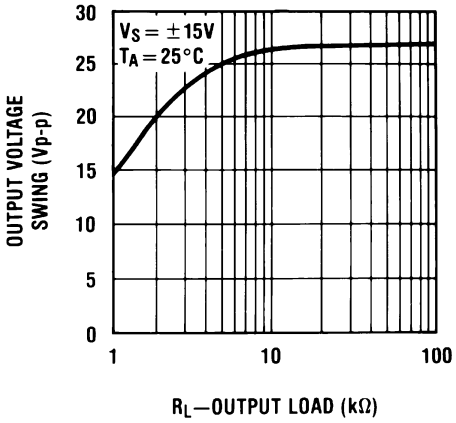


Figure 12.

Gain Bandwidth

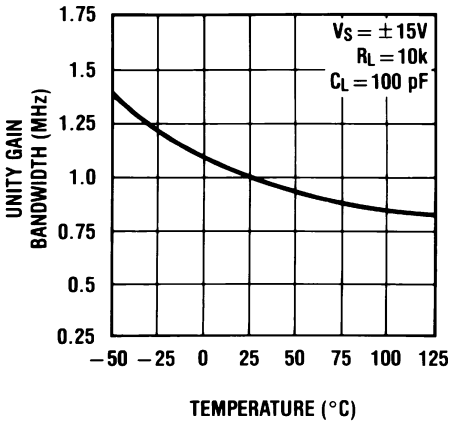


Figure 13.

Bode Plot

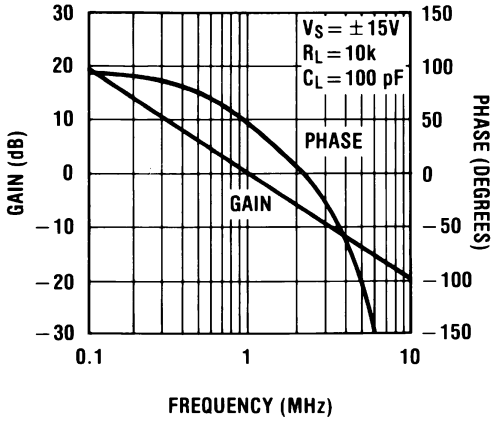


Figure 14.

Slew Rate

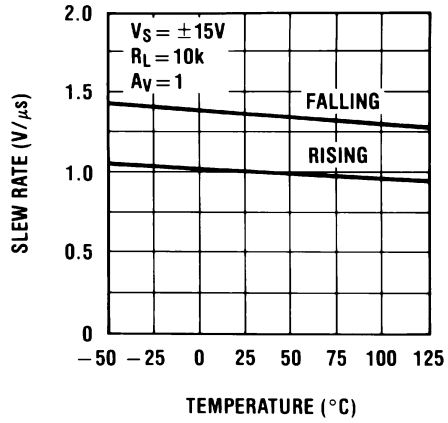


Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Distortion vs Frequency

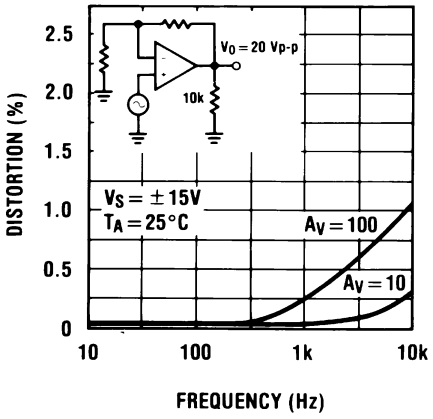


Figure 16.

Undistorted Output Voltage Swing

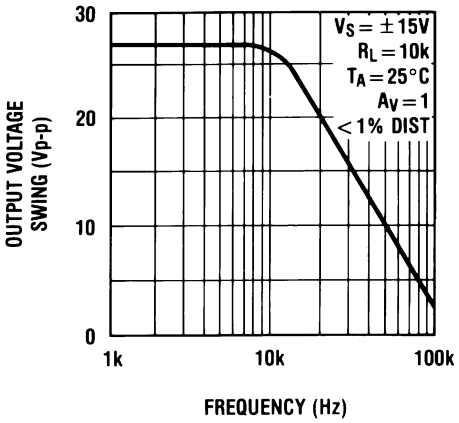


Figure 17.

Open Loop Frequency Response

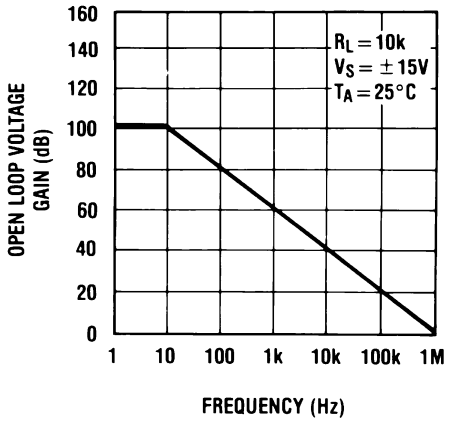


Figure 18.

Common-Mode Rejection Ratio

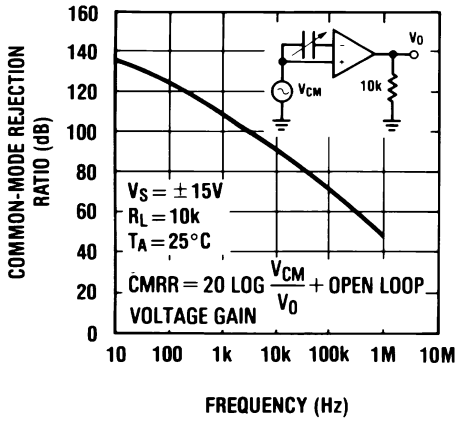


Figure 19.

Power Supply Rejection Ratio

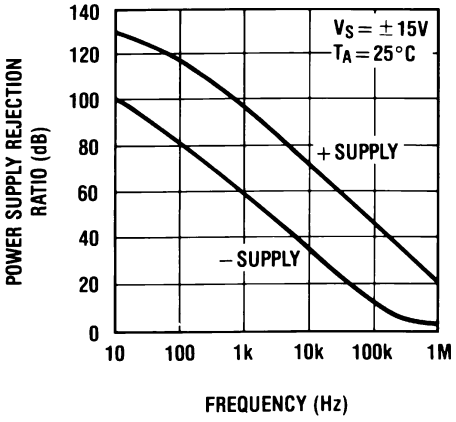


Figure 20.

Equivalent Input Noise Voltage

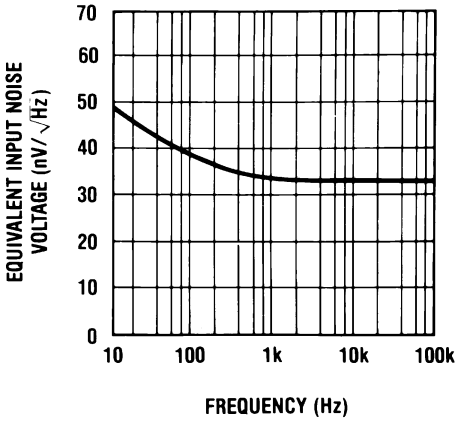


Figure 21.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Open Loop Voltage Gain

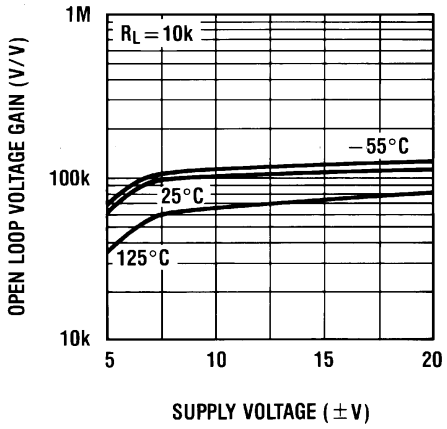


Figure 22.

Output Impedance

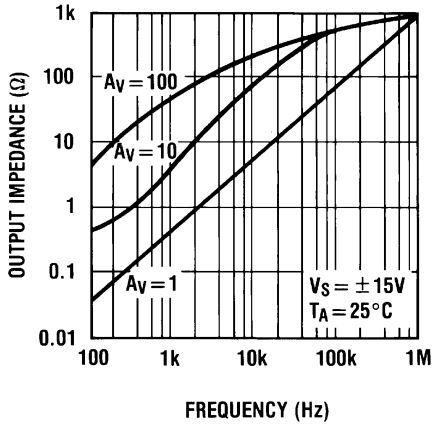


Figure 23.

Inverter Settling Time

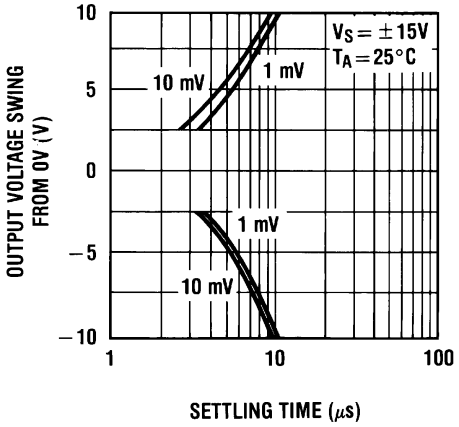


Figure 24.

PULSE RESPONSE

R_L = 10 kΩ, C_L = 10 pF

Small Signal Inverting

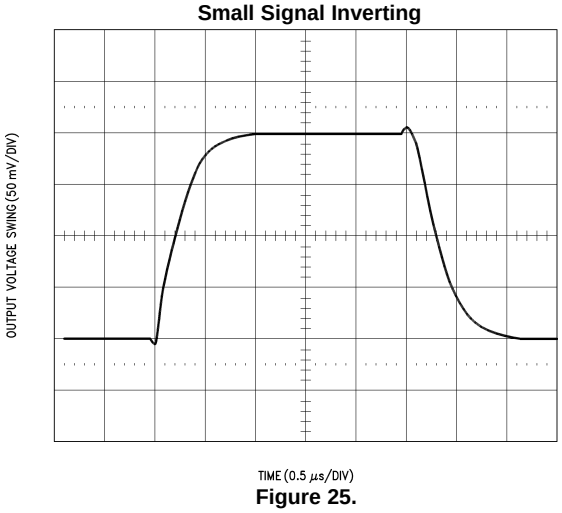


Figure 25.

Small Signal Non-Inverting

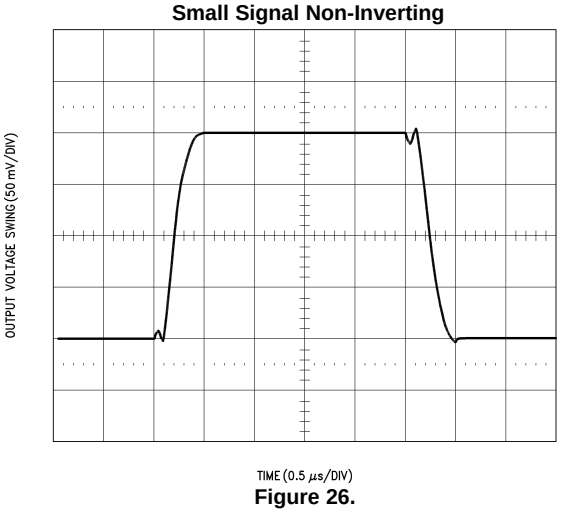


Figure 26.

Large Signal Inverting

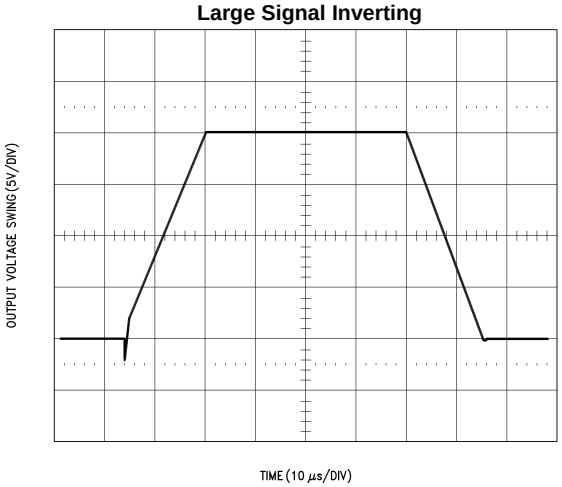


Figure 27.

Large Signal Non-Inverting

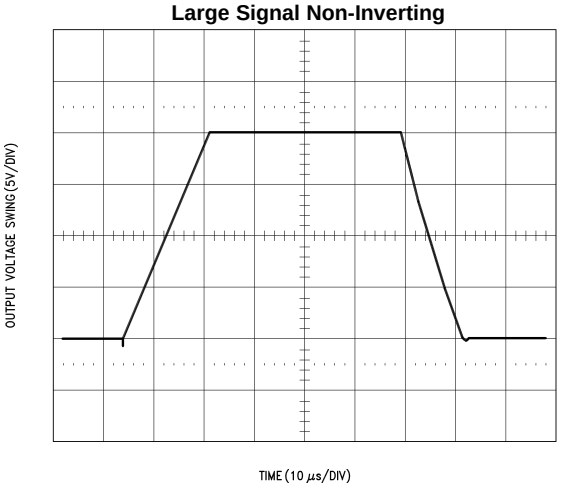


Figure 28.

APPLICATION HINTS

This device is a quad low power op amp with JFET input devices (BI-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

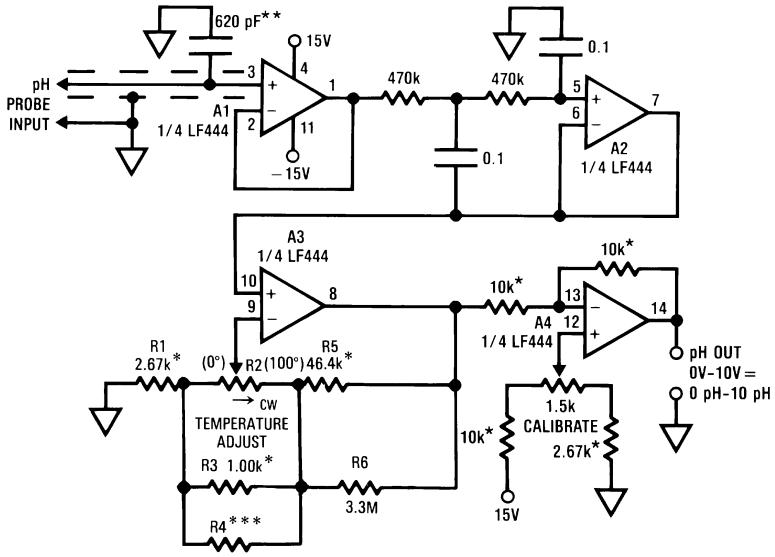
The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application



***For R2 = 50kΩ, R4 = 330k ±1%
For R2 = 100k, R4 = 75k ±1%
For R2 = 200k, R4 = 56k ±1%
**Polystyrene
*Film resistor type RN60C
To calibrate, insert probe in pH =7 solution. Set the “TEMPERATURE ADJUST” pot, R2, to correspond to the solution temperature: full clockwise for 0°C, and proportionately for intermediate temperatures, using a turns-counting dial. Then set “CALIBRATE” pot so output reads 7V.
Typical probe = Ingold Electrodes #465-35

Figure 29. pH Probe Amplifier/Temperature Compensator

REVISION HISTORY

Date Released	Revision	Section	Changes
12/16/2010	A	New release to corporate format	1 MDS datasheet converted to standard corporate format. MDS MNLF444M-X Rev 0AL will be archived.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LF444MD/883	ACTIVE	CDIP SB	NAK	14	25	TBD	Call TI	Call TI	-55 to 125	LF444MD/ 883 Q YQ ACO 883 Q >Y >T	Samples

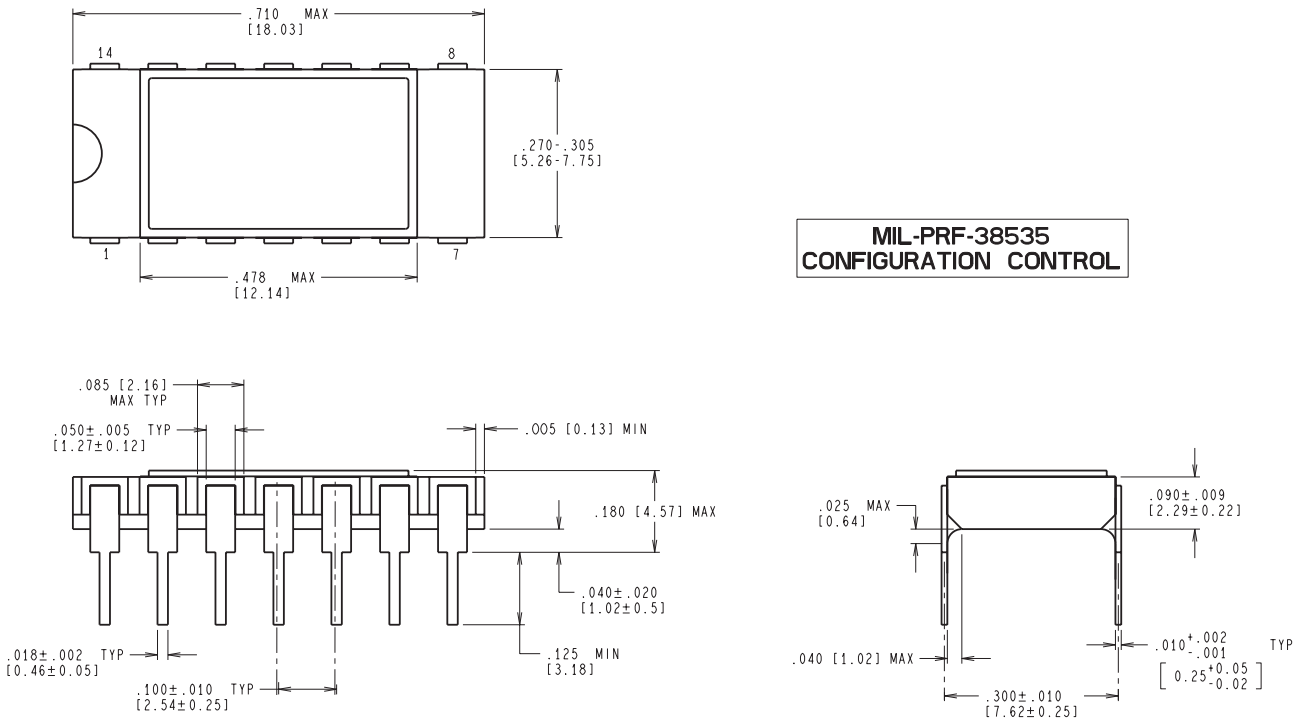
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

NAK0014D



MIL-PRF-38535
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

D14D (REV J)

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