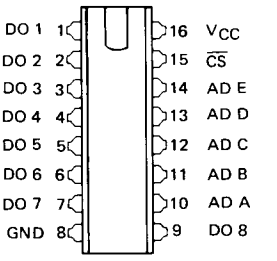
SERIES 54/74, 54S/74S
READ-ONLY MEMORIES

BULLETIN NO. DL-S 7512259, MAY 1975

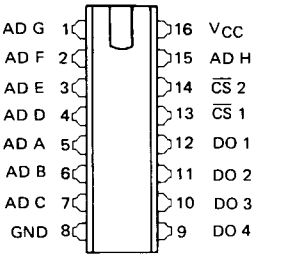
- Mask-Programmed Memories That Can Replace PROMs
- Full On-Chip Decoding and Fast Chip Select(s) Simplify System Decoding
- All Schottky-Clamped ROMs Offer
  - —Choice of 3-State or Open-Collector Outputs
  - —P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Applications Include:
  - —Microprogramming Firmware/Firmware Loaders
  - —Code Converters/Character Generators
  - —Translators/Emulators
  - —Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		TYPE OF	BIT SIZE	TYPICAL ACCESS TIMES	
−55°C to 125°C	0°C to 70°C	OUTPUT(S)	(ORGANIZATION)	CHIP-SELECT	ADDRESS
SN5488A(J, W)	SN7488A(J, N)	Open-Collector	256 Bits (32 W x 8 B)	22 ns	26 ns
SN54187(J, W)	SN74187(J, N)	Open-Collector	1024 Bits (256 W x 4 B)	20 ns	40 ns
SN54S270(J)	SN74S270(J, N)	Open-Collector	2048 Bits (512 W x 4 B)	15 ns	45 ns
SN54S370(J)	SN74S370(J, N)	3-State			
SN54S271(J)	SN74S271(J, N)	Open-Collector	2048 Bits (256 W x 8 B)	15 ns	45 ns
SN54S371(J)	SN74S371(J, N)	3-State			

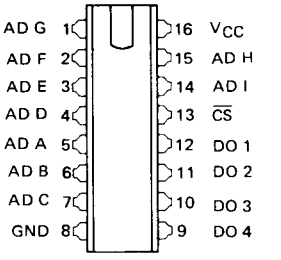
256 BITS (32 WORDS BY 8 BITS)
'88A



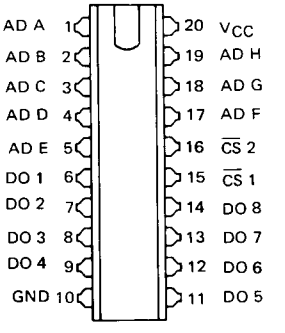
1024 BITS (256 WORDS BY 4 BITS)
'187



2048 BITS (512 WORDS BY 4 BITS)
'S270, 'S370



2048 BITS (256 WORDS BY 8 BITS)
'S271, 'S371



Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL custom-programmed read-only memories (ROMs) are particularly attractive for applications requiring medium to large quantities of the same bit pattern. Plug-in replacements can be obtained for most of the popular TTL PROMs.

The high-complexity 2048-bit ROMs can be used to significantly improve system bit density for fixed memory as all are offered in compact 16- or 20-pin dual-in-line packages having pin-row spacings of 0.300-inch.

The Schottky-clamped versions offer considerable flexibility for upgrading existing designs or improving new designs as they feature improved performance; plus, they offer low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

Data from a sequenced deck of data cards punched according to the specified format are permanently programmed by the factory into the monolithic structure for all bit locations. Upon receipt of the order, Texas Instruments will assign a special identifying number for each pattern programmed according to the order. The completed devices will be marked with the appropriate TI special device number. It is important that the customer specify not only the output levels desired at all bit locations, but also the other information requested under ordering instructions.

The three-state outputs offer the convenience of an open-collector output with the speed of a totem-pole output: they can be bus-connected to other similar outputs yet they retain the fast rise time characteristic of the TTL totem-pole output. The open-collector outputs offer the capability of direct interface with a data line having a passive pull-up.

Word-addressing is accomplished in straight positive-logic binary and the memory may be read when all $\overline{CS}$ inputs are low. A high at any $\overline{CS}$ input causes the outputs to be off.

TEXAS INSTRUMENTS
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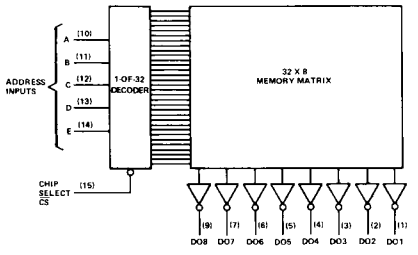
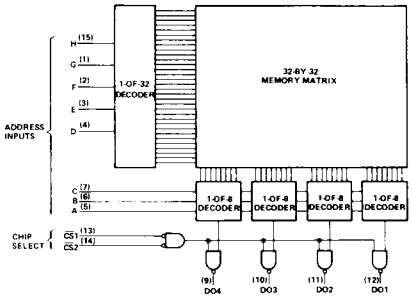
functional block diagrams

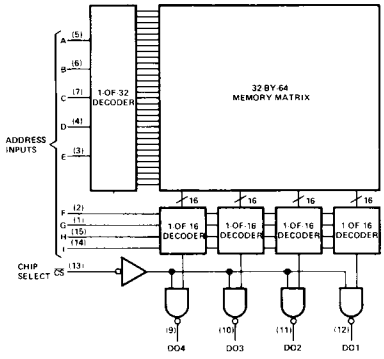
SN5488A, SN7488A



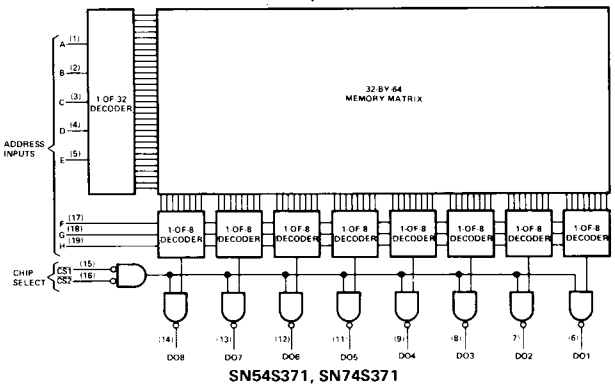
SN54187, SN74187



SN54S270, SN74S270

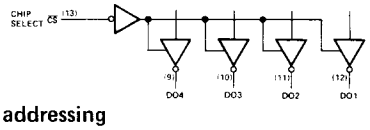


SN54S271, SN74S271



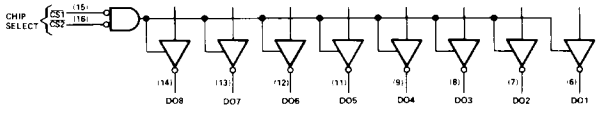
SN54S370, SN74S730

Same as SN54S270, SN74S270 except outputs are as shown below:



SN54S371, SN74S371

Same as SN54S271, SN74S271 except outputs are as shown below:



word addressing

'88A

WORD ADDRESS TABLE

WORD	INPUTS				
	E	D	C	B	A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
	Words 9 thru 26 omitted				
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

'187, 'S271, 'S371

WORD ADDRESS TABLE

WORD	INPUTS							
	H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	H	H
4	L	L	L	L	L	H	L	L
5	L	L	L	L	L	H	L	H
6	L	L	L	L	L	H	H	L
7	L	L	L	L	L	H	H	H
8	L	L	L	L	H	L	L	L
	Words 9 thru 250 omitted							
251	H	H	H	H	H	L	H	H
252	H	H	H	H	H	H	L	L
253	H	H	H	H	H	H	L	H
254	H	H	H	H	H	H	H	L
255	H	H	H	H	H	H	H	H

'S270, 'S370

WORD ADDRESS TABLE

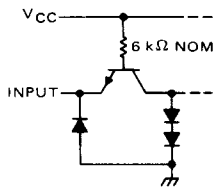
WORD	INPUTS							
	I	H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	L	H	H
4	L	L	L	L	L	L	H	L	L
5	L	L	L	L	L	L	H	L	H
6	L	L	L	L	L	L	H	H	L
7	L	L	L	L	L	L	H	H	H
8	L	L	L	L	L	H	L	L	L
	Words 9 thru 506 omitted								
507	H	H	H	H	H	H	L	H	H
508	H	H	H	H	H	H	H	L	L
509	H	H	H	H	H	H	H	L	H
510	H	H	H	H	H	H	H	H	L
511	H	H	H	H	H	H	H	H	H

Word selection is accomplished in a conventional positive-logic binary code with the A address input being the least-significant bit progressing alphabetically through the address inputs to the most-significant bit.

schematics of inputs and outputs

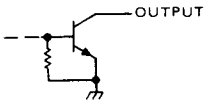
'88A, '187

EQUIVALENT OF EACH INPUT



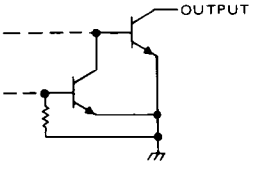
'88A

TYPICAL OF ALL OUTPUTS



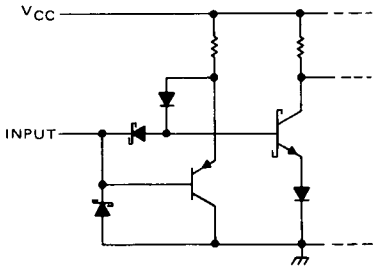
'187

TYPICAL OF ALL OUTPUTS



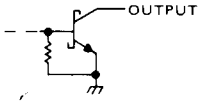
'S270, 'S271, 'S370, 'S371

EQUIVALENT OF EACH INPUT



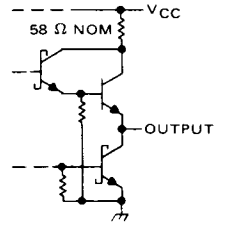
'S270, 'S271

TYPICAL OF ALL OUTPUTS



'S370, 'S371

TYPICAL OF ALL OUTPUTS



4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54', SN54S' Circuits (see Note 2)	−55°C to 125°C
	SN74', SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54187 in the W package operating at free-air temperatures above 111°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 46°C/W.

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recommended operating conditions

	SN5488A			SN7488A			SN54187			SN74187			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}			12			12			16			16	mA
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	−55		125	0		70	°C

NOTE 2: An SN54187 in the W package operating at free-air temperatures above 111°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 46°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'88A			'187			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			40			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA		0.2	0.4			0.4	V
			I_{OL} = 16 mA						0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			25			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1			−1	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		64	80		92	130	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 5 V,		6.5			6.5		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 3: With outputs open and $\overline{CS}$ input(s) grounded, I_{CC} is measured first by selecting a word that contains the maximum number of programmed high-level outputs, then by selecting a word that contains the maximum number of programmed low-level outputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'88A		'187		UNIT
			TYP	MAX	TYP	MAX	
$t_{a(ad)}$	Access time from address	C_L = 30 pF, R_{L1} = 400 Ω ('88A) 300 Ω ('187) R_{L2} = 600 Ω, See Figure 1	26	45	40	60	ns
$t_{a(\overline{CS})}$	Access time from chip select (enable time)		22	35	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select (disable time)		22	35	20	30	ns

recommended operating conditions

	SN54S270 SN54S271			SN74S270 SN74S271			SN54S370 SN54S371			SN74S370 SN74S371			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5							V
High-level output current, I_{OH}									−2			−6.5	mA
Low-level output current, I_{OL}			16			16			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'S270, 'S271			'S370, 'S371			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX				2.4			V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50				μA
			V_{OH} = 5.5 V			100				μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,						50	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,						−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX					−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4		105	155		105	155	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 5 V,		6.5			6.5		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 4: With outputs open and $\overline{CS}$ input(s) grounded, I_{CC} is measured first by selecting a word that contains the maximum number of programmed high-level outputs; then by selecting a word that contains the maximum number of programmed low-level outputs.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54270 SN54271		SN74270 SN74271		SN54370 SN54370		SN74370 SN74370		UNIT
			TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address	R_{L2} = 600 Ω, See Figure 1	45	95	45	70					ns
$t_{a(\overline{CS})}$	Access time from chip select (enable time)		15	45	15	30					ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select (disable time)		15	40	15	25					ns
$t_{a(ad)}$	Access time from address	C_L = 30 pF, See Figure 2					45	95	45	70	ns
$t_{a(\overline{CS})}$	Access time from chip select (enable time)						15	45	15	30	ns
t_{PXZ}	Disable time from high or low level	C_L = 5 pF, See Figure 2					10	40	10	25	ns

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

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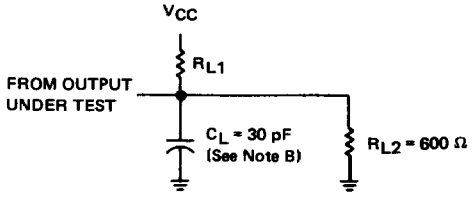
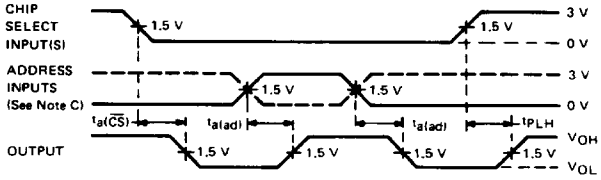
PARAMETER MEASUREMENT INFORMATION



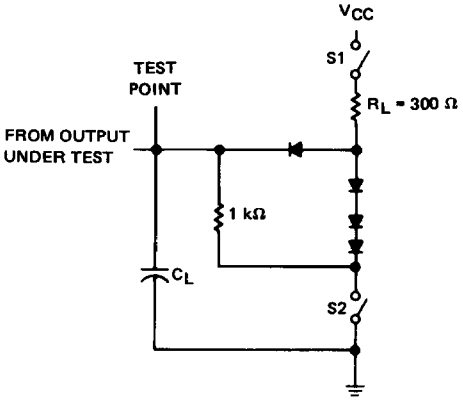
LOAD CIRCUIT



VOLTAGE WAVEFORMS

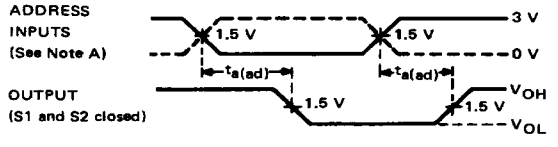
NOTES: A. The input pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$. For Series 54/74, $t_r \leq 7$ ns, $t_f \leq 7$ ns, for Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 1–SWITCHING TIMES OF '88A, '187, 'S270, AND 'S271 (OPEN-COLLECTOR OUTPUTS)

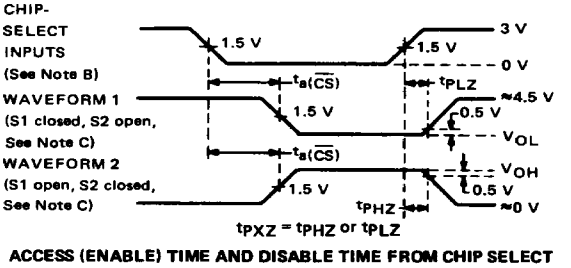


C_L includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP SELECT VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip-select input(s) is(are) low.
B. When measuring access and disable times from chip-select input(s) the address inputs are steady-state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 2–SWITCHING TIMES OF 'S370 AND 'S371 (3-STATE OUTPUTS)

ORDERING INSTRUCTIONS

Programming instructions for these read-only memories are solicited in the form of a sequenced deck of standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table for the requested part. This function table, showing output conditions for each of the words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the words specified and describes the levels at the outputs for each of those words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

The following information will be furnished to the customer by Texas Instruments:

a) TI part number
b) TI sales order number
c) Date received.

'88A DATA CARD FORMAT (32 CARDS)

Column	
1-2	Punch a right-justified integer representing the positive-logic binary input address (00-31) for the word described on the card.
3-4	Blank
5	Punch "H" or "L" for output Y8. H = high-voltage-level output, L = low-voltage-level output
6-9	Blank
10	Punch "H" or "L" for output DO 7.
11-14	Blank
15	Punch "H" or "L" for output DO 6.
16-19	Blank
20	Punch "H" or "L" for output DO 5.
21-24	Blank
25	Punch "H" or "L" for output DO 4.
26-29	Blank
30	Punch "H" or "L" for output DO 3.
31-34	Blank
35	Punch "H" or "L" for output DO 2.
36-39	Blank
40	Punch "H" or "L" for output DO 1.
41-49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

'187 DATA CARD FORMAT (32 CARDS)

Column	
1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8- 9	Blank

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ORDERING INSTRUCTIONS

10-13 Punch "H", "L", or "X" for bits four, three, two, and one (outputs DO 4, DO 3, DO 2 and DO 1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.

14 Blank

15-18 Punch "H", "L", or "X" for the second set of outputs.

19 Blank

20-23 Punch "H", "L", or "X" for the third set of outputs.

24 Blank

25-28 Punch "H" "L", or "X" for the fourth set of outputs.

29 Blank

30-33 Punch "H", "L", or "X" for the fifth set of outputs.

34 Blank

35-38 Punch "H", "L", or "X" for the sixth set of outputs.

39 Blank

40-43 Punch "H", "L", or "X" for the seventh set of outputs.

44 Blank

45-48 Punch "H", "L", or "X" for the eighth set of outputs.

49 Blank

50-51 Punch a right-justified integer representing the current calendar day of the month.

52 Blank

53-55 Punch an alphabetic abbreviation representing the current month.

56 Blank

57-58 Punch the last two digits of the current year.

59 Blank

60-61 Punch "SN"

62-66 Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.

67-68 Blank

69-80 Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

'S270, 'S370 DATA CARD FORMAT (64 CARDS)

Column

1-3 Punch a right-justified integer representing the binary input address (000-504) for the first set of outputs described on the card.

4 Punch a "–" (Minus sign)

5-7 Punch a right-justified integer representing the binary input address (007-511) for the last set of outputs described on the card.

8-80 Same as the '187 data card format.

'S271, 'S371 DATA CARD FORMAT (64 CARDS)

Column

1- 3 Punch a right-justified integer representing the binary input address (000-252) for the first set of outputs described on the card.

4 Punch a "–" (Minus sign)

5- 7 Punch a right-justified integer representing the binary input address (003-255) for the last set of outputs described on the card.

8- 9 Blank

10-17 Punch "H", "L", or "X" for bits eight, seven, six, five, four, three, two, and one (outputs DO 8, DO 7, DO 6, DO 5, DO 4, DO 3, DO 2, and DO 1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.

18 Blank

19-26 Punch "H", "L", or "X" for the second set of outputs.

27 Blank

28-35 Punch "H", "L", or "X" for the third set of outputs.

36 Blank

37-44 Punch "H", "L", or "X" for the fourth set of outputs.

45-49 Blank

50-80 Same as the '187 data card format.

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