- Designed to Reduce Reflection Noise

- Repetitive Peak Forward Current . . . 200 mA

- 16-Bit Array Structure Suited for Bus-Oriented Systems

- ESD Protection Exceeds 10 kV Per MIL-STD-883C, Method 3015

- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

DW OR N PACKAGE
(TOP VIEW)

DO1	1	20	D16
DO2	2	19	D15
DO3	3	18	D14
DO4	4	17	D13
GND	5	16	GND
GND	6	15	GND
DO5	7	14	D12
DO6	8	13	D11
DO7	9	12	D10
DO8	10	11	DO9
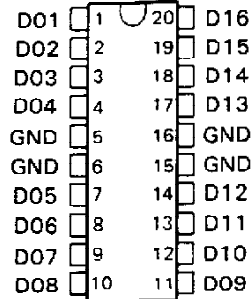
description
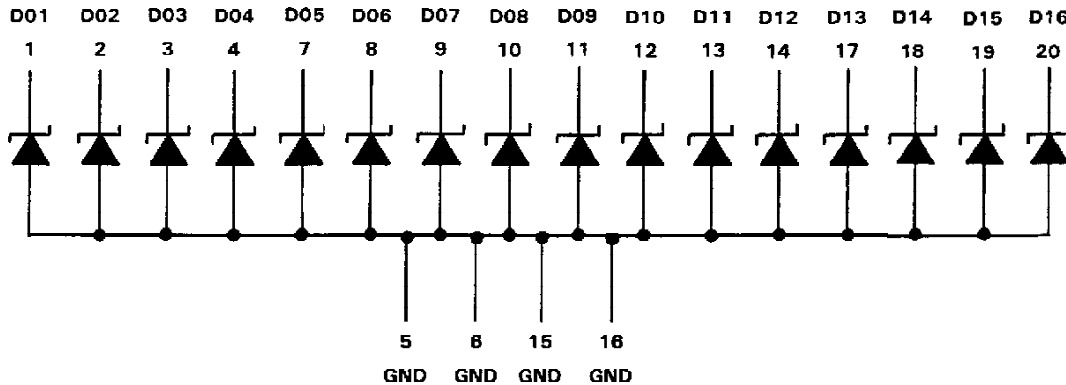
This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 16-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1052 is characterized for operation from 0 °C to 70 °C.

schematic diagram

DO1	DO2	DO3	DO4	DO5	DO6	DO7	DO8	DO9	D10	D11	D12	D13	D14	D15	D16
1	2	3	4	7	8	9	10	11	12	13	14	17	18	19	20

5	6	15	16
GND	GND	GND	GND

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Steady-state reverse voltage, V_R	7 V
Continuous forward current, I_F: any D terminal from GND	50 mA
total through all GND terminals	170 mA
Repetitive peak forward current,[‡] I_{FRM}: any D terminal from GND	200 mA
total through all GND terminals	1 A
Continuous total power dissipation at (or below) 25°C free-air temperature	735 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡]These values apply for $t_W \leq 100$ μs, duty cycle $\leq 20\%$.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP[§]	MAX	UNIT
I_R	Static reverse current	$V_R = 7$ V			5	μA
V_F	Static forward voltage	$I_F = 18$ mA		0.75	0.95	V
		$I_F = 50$ mA		0.95	1.2	
V_{FM}	Peak forward voltage	$I_F = 200$ mA			1.45	V
C_T	Total capacitance	$V_R = 0$, f = 1 MHz		5	10	pF
		$V_R = 2$ V, f = 1 MHz		4	8	

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS	MIN	TYP[§]	MAX	UNIT
I_X	Internal crosstalk current	Total $I_F = 1$ A, See Note 2		0.6	2	mA
		Total $I_F = 270$ mA, See Note 2		0.02	0.2	

[§]All typical values are at $T_A = 25$°C.

NOTE 2. I_X is measured under the following conditions with one diode static and all others switching:
Switching diodes: $t_W = 100$ μs, duty cycle = 20%; static diode: $V_R = 5$ V.
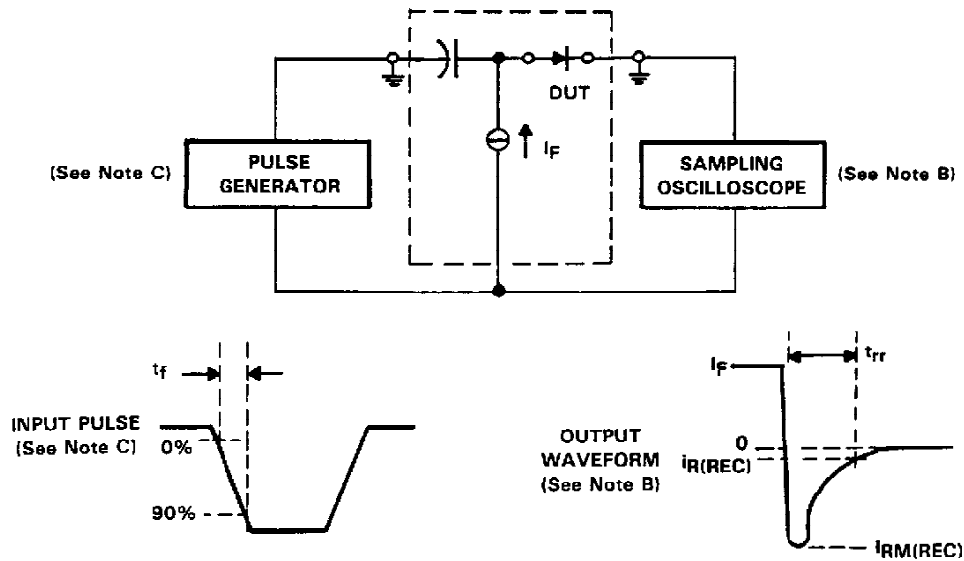The static diode's input current is the internal crosstalk current I_X.

switching characteristics at 25°C free-air temeprature (see Figures 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	$I_F = 10$ mA, $I_{RM(REC)} = 10$ mA, $i_{R(REC)} = 1$ mA, $R_L = 100$ Ω			8	16	ns

PARAMETER MEASUREMENT INFORMATION

FIGURE 1. FORWARD RECOVERY VOLTAGE

FIGURE 2. REVERSE RECOVERY TIME
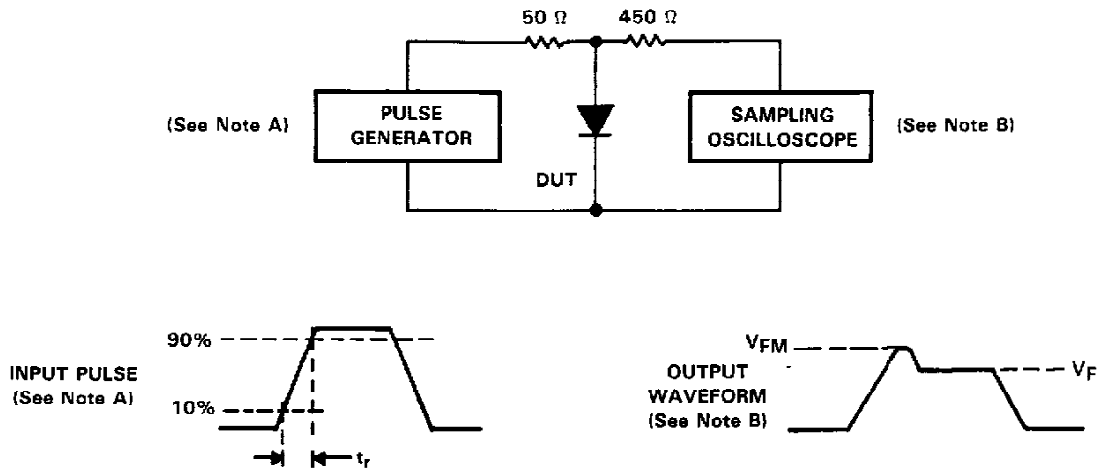
NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: t_r = 20 ns, Z_{out} = 50 Ω, f_{PR} = 500 Hz, duty cycle = 0.01.
      B. The output waveform is monitored by an oscilloscope having the following characteristics: t_r ≤ 350 ps, R_{in} = 50 Ω, C_{in} = ≤ 5 pF.
      C. The input pulse is supplied by a pulse generator having the following characteristics: t_f = 0.5 ns, Z_{out} = 50 Ω, t_w = ≤ 50 ns, duty cycle ≥ 0.01.

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APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.), or on the CLOCK lines of many clocked devices can result in improper operation of the device. The SN74S1050 and SN74S1052 diode termination arrays help suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients by the diode tracks the current-voltage characteristic curve for the diode. A typical current-voltage curve for the SN74S1050/S1052 is shown in Figure 3.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 4 was evaluated. The resulting waveforms with and without the diode are shown in Figure 5.

The maximum effectiveness of the diode in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

VARIABLE 1:
V$_I$ −CH1
LINEAR SWEEP
START   0.000 V
STOP   −2.000 V
STOP   −0.010 V

CONSTANTS:
V$_H$ V$_{s1}$ 3.5000 V
V$_L$ V$_{s2}$ 0.0000 V

FIGURE 3. TYPICAL CURRENT-VOLTAGE CURVE

$Z_O = 50 \ \Omega$
LENGTH = 36 IN

FIGURE 4. DIODE TEST SETUP

31.500 ns	56.500 ns	81.500 ns

END OF
LINE
WITHOUT
DIODE

END OF LINE WITH DIODE

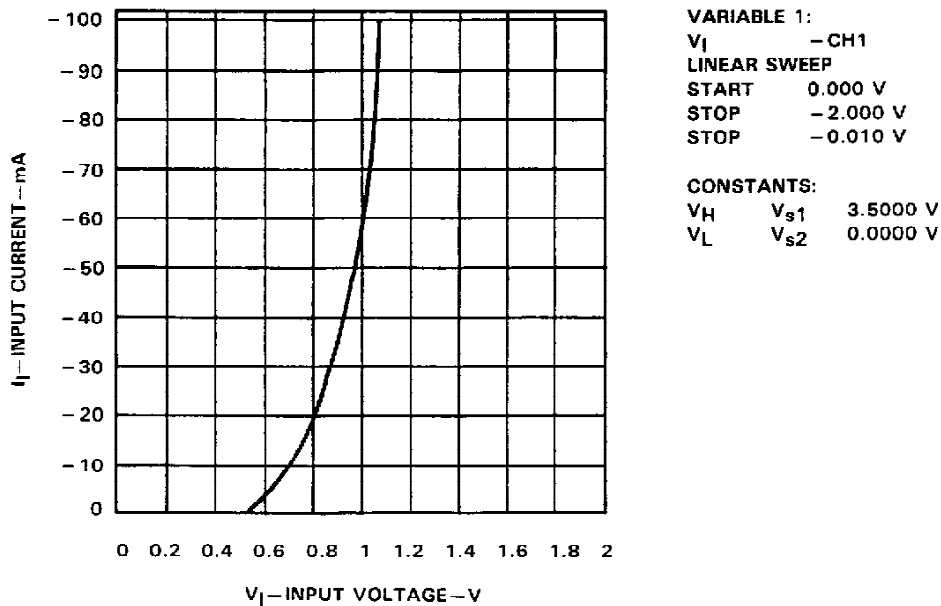| Y-COORDINATE	= 1,800 VOLTS/DIV	OFFSET	= 0.000 VOLTS
TIMEBASE	= 5.00 ns/VOLTS	DELAY	= 56.500 ns
VMARKER 1	= −1.353 VOLTS	DELTA V	= −2.293 VOLTS
VMARKER 2	= −3.647 VOLTS		

FIGURE 5. SCOPE DISPLAY

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74S1052DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74S1052DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74S1052N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S1052NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60) / 0.240 (6,10)

1   8

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ | 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AC.

MECHANICAL DATA

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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