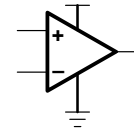


TLV4110, TLV4111, TLV4112, TLV4113 FAMILY OF HIGH OUTPUT DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN

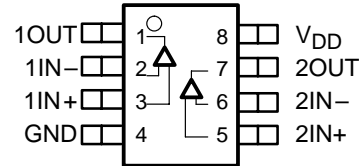
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- High Output Drive . . . >300 mA
- Rail-To-Rail Output
- Unity-Gain Bandwidth . . . 2.7 MHz
- Slew Rate . . . 1.5 V/ μ s
- Supply Current . . . 700 μ A/Per Channel
- Supply Voltage Range . . . 2.5 V to 6 V
- Specified Temperature Range:
 - $T_A = 0^\circ\text{C}$ to 70°C . . . Commercial Grade
 - $T_A = -40^\circ\text{C}$ to 125°C . . . Industrial Grade
- Universal OpAmp EVM

Operational Amplifier



TLV4112
D, DGN, OR P PACKAGE
(TOP VIEW)



description

The TLV411x single supply operational amplifiers provide output currents in excess of 300 mA at 5 V. This enables standard pin-out amplifiers to be used as high current buffers or in coil driver applications. The TLV4110 and TLV4113 come with a shutdown feature.

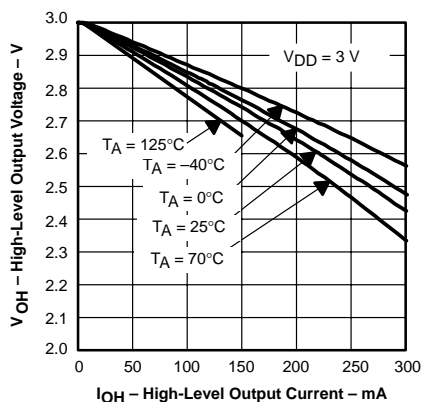
The TLV411x is available in the ultra small MSOP PowerPAD™ package, which offers the exceptional thermal impedance required for amplifiers delivering high current levels.

All TLV411x devices are offered in PDIP, SOIC (single and dual) and MSOP PowerPAD (dual).

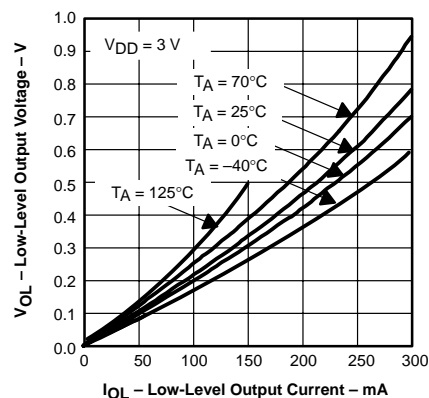
FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES			SHUTDOWN	UNIVERSAL EVM BOARD
		MSOP	PDIP	SOIC		
TLV4110	1	8	8	8	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV4111	1	8	8	8	—	
TLV4112	2	8	8	8	—	
TLV4113	2	10	14	14	Yes	

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TLV4110 AND TLV4111 AVAILABLE OPTIONS

T _A	PACKAGED DEVICES			
	SMALL OUTLINE (D)†‡	MSOP		PLASTIC DIP (P)
		SMALL OUTLINE (DGN)†	SYMBOL	
0°C to 70°C	TLV4110CD	TLV4110CDGN	xxTIAHL	TLV4110CP
	TLV4111CD	TLV4111CDGN	xxTIAHN	TLV4111CP
–40°C to 125°C	TLV4110ID	TLV4110IDGN	xxTIAHM	TLV4110IP
	TLV4111ID	TLV4111IDGN	xxTIAHO	TLV4111IP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV4110CDR).

‡ In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.

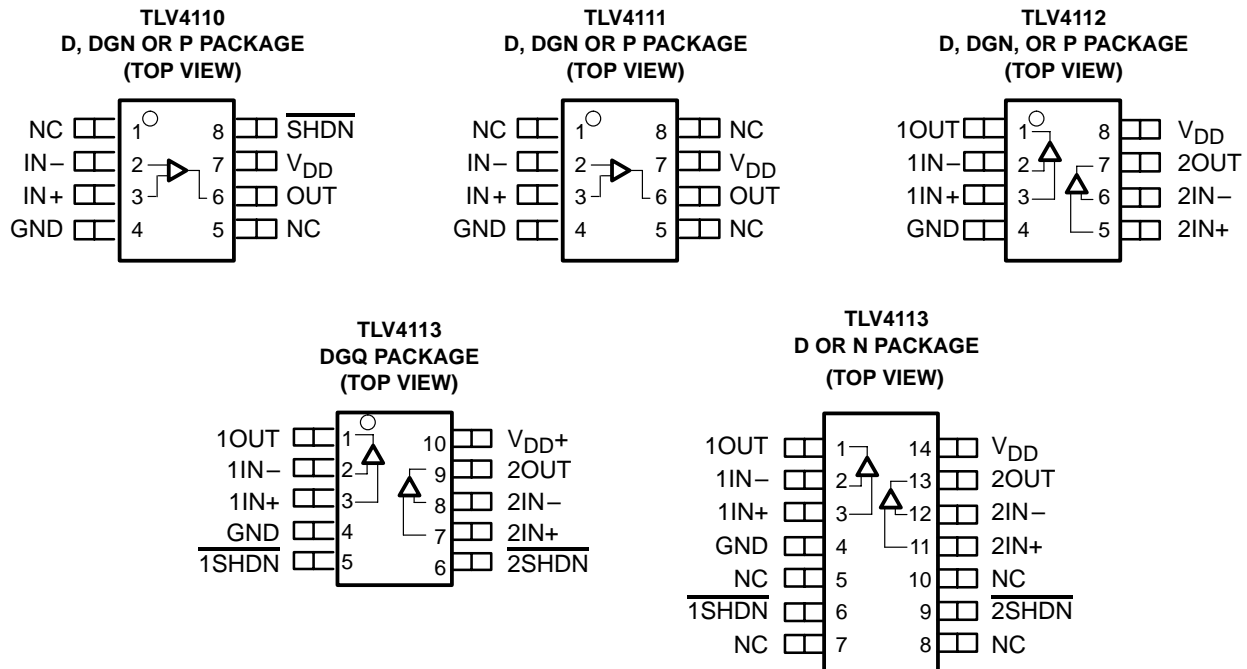
TLV4112 AND TLV4113 AVAILABLE OPTIONS

T _A	PACKAGED DEVICES					
	SMALL OUTLINE (D)†‡	MSOP				PLASTIC DIP (P)
		SMALL OUTLINE (DGN)†	SYMBOL	SMALL OUTLINE (DGQ)†	SYMBOL	
0°C to 70°C	TLV4112CD	TLV4112DGN	xxTIAHP	—	—	TLV4112CP
	TLV4113CD	—	—	TLV4113CDGQ	xxTIAHR	TLV4113CN
–40°C to 125°C	TLV4112ID	TLV4112IDGN	xxTIAHQ	—	—	TLV4112IP
	TLV4113ID	—	—	TLV4113IDGQ	xxTIAHS	TLV4113IN

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV4112CDR).

‡ In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.

TLV411x PACKAGE PINOUTS



NC – No internal connection

TLV4110, TLV4111, TLV4112, TLV4113 FAMILY OF HIGH OUTPUT DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	7 V
Differential input voltage, V_{ID}	$\pm V_{DD}$
Input voltage range, V_I	$\pm V_{DD}$
Output current, I_O (see Note 2)	800 mA
Continuous /RMS output current, I_O (each output of amplifier):	
$T_J \leq 105^\circ\text{C}$	350 mA
$T_J \leq 150^\circ\text{C}$	110 mA
Peak output current, I_O (each output of amplifier):	
$T_J \leq 105^\circ\text{C}$	500 mA
$T_J \leq 150^\circ\text{C}$	155 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A :	
C suffix	0°C to 70°C
I suffix	-40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. To prevent permanent damage the die temperature must not exceed the maximum junction temperature.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} ($^\circ\text{C}/\text{W}$)	θ_{JA} ($^\circ\text{C}/\text{W}$)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.3	1022 mW	204.4 mW
DGN (8)‡	4.7	52.7	2.37 W	474.4 mW
DGQ (10)‡	4.7	52.3	2.39 W	478 mW
P (8)	41	104	1200 mW	240.4 mW
N (14)	32	78	1600 mW	320.5 mW

‡ See The Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}			2.5	6	V
Common-mode input voltage range, V_{ICR}			0	$V_{DD}-1.5$	V
Operating free-air temperature, T_A	C-suffix		0	70	$^\circ\text{C}$
	I-suffix		-40	125	
Shutdown turnon/off voltage level§	V(on)	$V_{DD} = 3\text{ V}$	2.1		V
		$V_{DD} = 5\text{ V}$	3.8		
	V(off)	$V_{DD} = 3\text{ V}$		0.9	
		$V_{DD} = 5\text{ V}$		1.65	

§ Relative to GND



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electrical characteristics at recommend operating conditions, $V_{DD} = 3\text{ V}$ and 5 V (unless otherwise noted)

dc performance

PARAMETER		TEST CONDITIONS		T_A^\dagger	MIN	TYP	MAX	UNITS
V_{IO}	Input offset voltage	$V_{IC} = V_{DD}/2,$ $R_L = 100\ \Omega,$	$V_O = V_{DD}/2,$ $R_S = 50\ \Omega$	25°C	175	3500		μV
				Full range		4000		
αV_{IO}	Offset voltage draft			25°C		3		$\mu\text{V}/^\circ\text{C}$
CMRR	Common-mode rejection ratio	$V_{DD} = 3\text{ V},$ $R_S = 50\ \Omega$	$V_{IC} = 0\text{ to }2\text{ V},$	25°C		63		dB
			$V_{IC} = 0\text{ to }4\text{ V},$	25°C		68		
A _{VD}	Large-signal differential voltage amplification	$V_{DD} = 3\text{ V},$ $V_{O(PP)} = 0\text{ to }1\text{ V}$	$R_L = 100\ \Omega$	25°C	78	84		dB
				Full range		67		
			$R_L = 10\ \text{k}\Omega$	25°C	85	100		
				Full range		75		
		$V_{DD} = 5\text{ V},$ $V_{O(PP)} = 0\text{ to }3\text{ V}$	$R_L = 100\ \Omega$	25°C	88	94		
				Full range		75		
			$R_L = 10\ \text{k}\Omega$	25°C	90	110		
				Full range		85		

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

input characteristics

PARAMETER		TEST CONDITIONS		T_A^\dagger	MIN	TYP	MAX	UNITS
I_{IO}	Input offset current	$V_{IC} = V_{DD}/2$	TLV411xC	25°C	0.3	25		pA
				Full range		50		
			TLV411xI			250		
I_{IB}	Input bias current	$V_O = V_{DD}/2,$ $R_S = 50\ \Omega$	TLV411xC	25°C	0.3	50		pA
				Full range		100		
			TLV411xI			500		
$r_{i(d)}$	Differential input resistance			25°C		1000		G Ω
C_{IC}	Common-mode input capacitance	$f = 100\ \text{Hz}$		25°C		5		pF

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ and 5 V (unless otherwise noted) (continued)

output characteristics

PARAMETER	TEST CONDITIONS	T_A †	MIN	TYP	MAX	UNITS
V_{OH} High-level output voltage	$V_{DD} = 3\text{ V}$, $V_{IC} = V_{DD}/2$	$I_{OH} = -10\text{ mA}$	25°C	2.7	2.97	V
			Full range	2.7		
		$I_{OH} = -100\text{ mA}$	25°C	2.6	2.73	
			Full range	2.6		
	$V_{DD} = 5\text{ V}$, $V_{IC} = V_{DD}/2$	$I_{OH} = -10\text{ mA}$	25°C	4.7	4.96	V
			Full range	4.7		
		$I_{OH} = -100\text{ mA}$	25°C	4.6	4.76	
			Full range	4.6		
$I_{OH} = -200\text{ mA}$	25°C	4.45	4.6			
	-40°C to 85°C	4.35				
V_{OL} Low-level output voltage	$V_{DD} = 3\text{ V}$ and 5 V , $V_{IC} = V_{DD}/2$	$I_{OL} = 10\text{ mA}$	25°C	0.03	0.1	V
			Full range		0.1	
		$I_{OL} = 100\text{ mA}$	25°C	0.33	0.4	
			Full range		0.55	
	$V_{DD} = 5\text{ V}$, $V_{IC} = V_{DD}/2$	$I_{OL} = 200\text{ mA}$	25°C	0.38	0.6	
			-40°C to 85°C		0.7	
I_O Output current‡	Measured at 0.5 V from rail	$V_{DD} = 3\text{ V}$	25°C	±220		mA
		$V_{DD} = 5\text{ V}$		±320		
I_{OS} Short-circuit output current‡	Sourcing	25°C	800		mA	
	Sinking		800			

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

‡ When driving output currents in excess of 200 mA, the MSOP PowerPAD package is required for thermal dissipation.

power supply

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNITS
I_{DD} Supply current (per channel)	$V_O = V_{DD}/2$	25°C		700	1000	μA
		Full range			1500	
PSRR Power supply rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ to }3.3\text{ V}$, No load, $V_{IC} = V_{DD}/2\text{ V}$	25°C	70	82	dB	
		Full range	65			
	$V_{DD} = 4.5\text{ to }5.5\text{ V}$, No load, $V_{IC} = V_{DD}/2\text{ V}$	25°C	70	79		
		Full range	65			

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.



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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ and 5 V (unless otherwise noted) (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		T_A^\dagger	MIN	TYP	MAX	UNITS
GBWP	Gain bandwidth product	$R_L = 100\ \Omega$	$C_L = 10\ \text{pF}$	25°C		2.7		MHz
SR	Slew rate at unity gain	$V_{O(pp)} = 2\text{ V}$, $R_L = 100\ \Omega$, $C_L = 10\ \text{pF}$	$V_{DD} = 3\text{ V}$	25°C	0.8	1.57		V/ μs
				Full range	0.55			
			$V_{DD} = 5\text{ V}$	25°C	1	1.57		
				Full range	0.7			
ϕ_M	Phase margin	$R_L = 100\ \Omega$,	$C_L = 10\ \text{pF}$	25°C	66			
	Gain margin				16			dB
t_s	Settling time	$V(\text{STEP})_{pp} = 1\text{ V}$, $A_V = -1$, $C_L = 10\ \text{pF}$, $R_L = 100\ \Omega$	0.1%	25°C	0.7			μs
			0.01%		1.3			

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

noise/distortion performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNITS
THD+N	Total harmonic distortion plus noise	$V_{O(pp)} = V_{DD}/2\text{ V}$, $R_L = 100\ \Omega$, $f = 100\ \text{Hz}$	$A_V = 1$	25°C	0.025			
			$A_V = 10$		0.035			
			$A_V = 100$		0.15			
V_n	Equivalent input noise voltage	$f = 100\ \text{Hz}$ $f = 10\ \text{kHz}$		25°C	55			nV/ $\sqrt{\text{Hz}}$
					10			
I_n	Equivalent input noise current	$f = 1\ \text{kHz}$		25°C	0.31			fA/ $\sqrt{\text{Hz}}$

shutdown characteristics

PARAMETER		TEST CONDITIONS		T_A^\dagger	MIN	TYP	MAX	UNITS
$I_{DD}(\text{SHDN})$	Supply current in shutdown mode (per channel) (TLV4110, TLV4113)	$\overline{\text{SHDN}} = 0\text{ V}$		25°C	3.4	10		μA
				Full range	15			
$t(\text{ON})$	Amplifier turnon time ‡	$R_L = 100\ \Omega$		25°C	1			μs
$t(\text{Off})$	Amplifier turnoff time ‡		3.3					

† Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

‡ Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

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AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
CMRR	Common-mode rejection ratio	vs Frequency	3
V_{OH}	High-level output voltage	vs High-level output current	4, 6
V_{OL}	Low-level output voltage	vs Low-level output current	5, 7
Z_o	Output impedance	vs Frequency	8
I_{DD}	Supply current	vs Supply voltage	9
k_{SVR}	Power supply voltage rejection ratio	vs Frequency	10
AVD	Differential voltage amplification and phase	vs Frequency	11
	Gain-bandwidth product	vs Supply voltage	12
SR	Slew rate	vs Supply voltage	13
		vs Temperature	14
	Total harmonic distortion+noise	vs Frequency	15
V_n	Equivalent input voltage noise	vs Frequency	16
	Phase margin	vs Capacitive load	17
	Voltage-follower signal pulse response		18, 19
	Inverting large-signal pulse response		20, 21
	Small-signal inverting pulse response		22
	Crosstalk	vs Frequency	23
	Shutdown forward and reverse isolation		24
	Shutdown supply current	vs Free-air temperature	25
	Shutdown supply current/output voltage		26

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TYPICAL CHARACTERISTICS

**INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE**

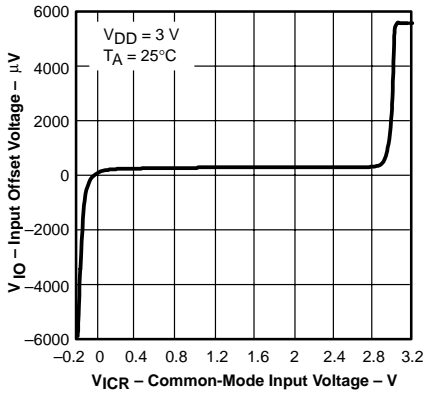


Figure 1

**INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE**

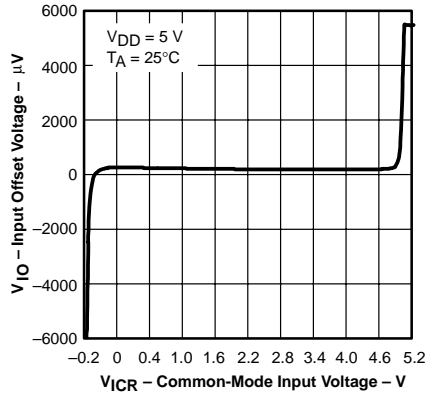


Figure 2

**COMMON-MODE REJECTION RATIO
vs
FREQUENCY**

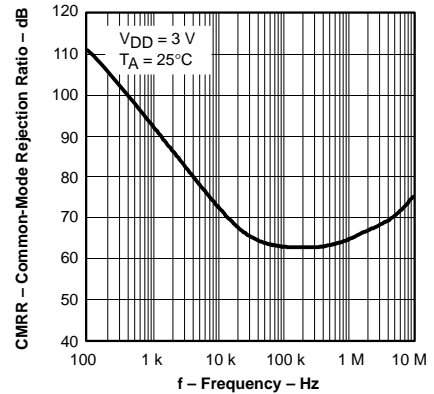


Figure 3

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

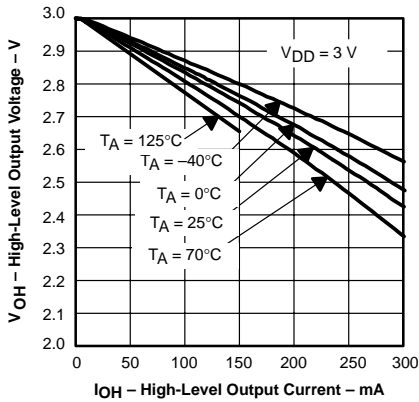


Figure 4

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

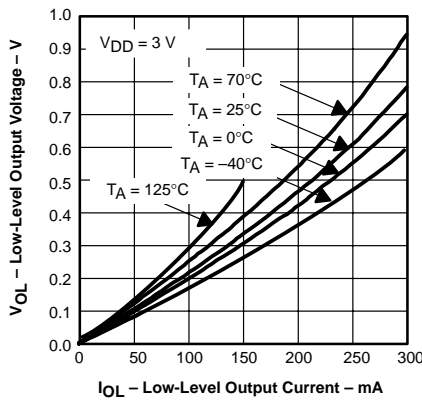


Figure 5

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

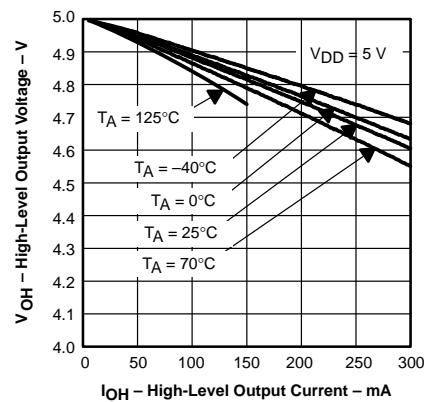


Figure 6

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

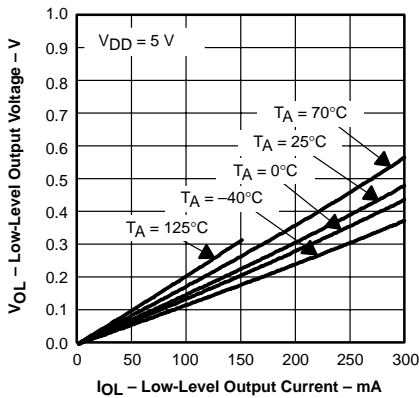


Figure 7

**OUTPUT IMPEDANCE
vs
FREQUENCY**

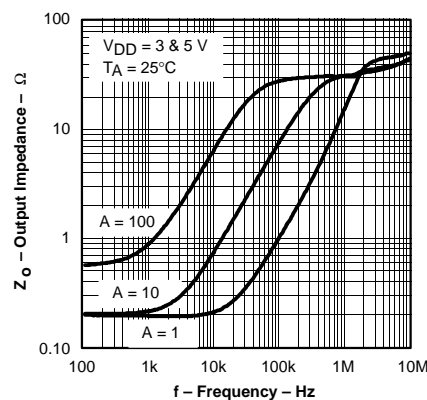


Figure 8

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

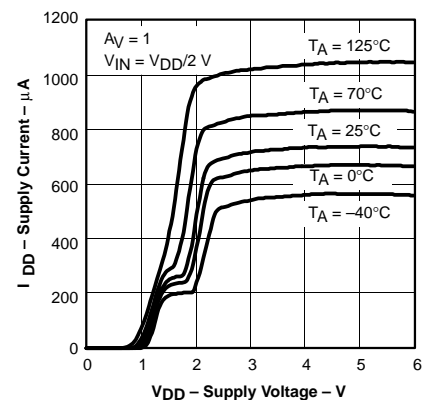


Figure 9



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TYPICAL CHARACTERISTICS

**POWER SUPPLY REJECTION RATIO
VS
FREQUENCY**

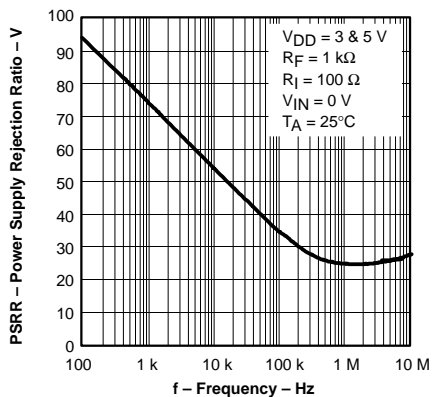


Figure 10

**DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE
VS
FREQUENCY**

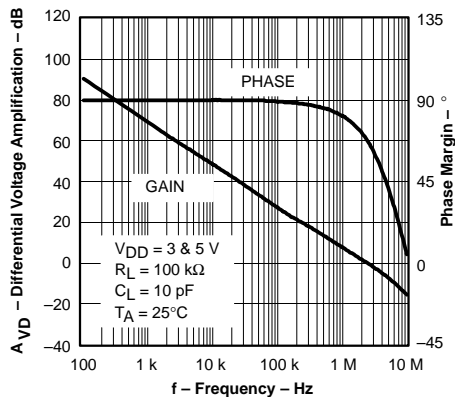


Figure 11

**GAIN-BANDWIDTH PRODUCT
VS
SUPPLY VOLTAGE**

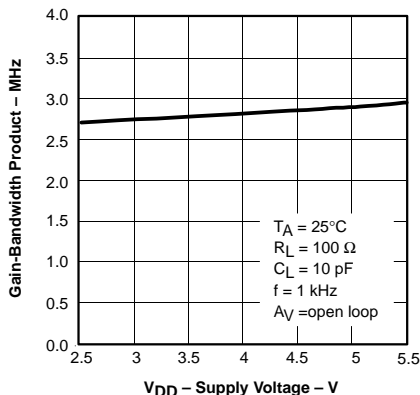


Figure 12

**SLEW RATE
VS
SUPPLY VOLTAGE**

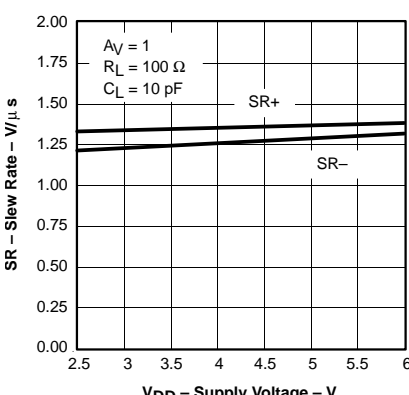


Figure 13

**SLEW RATE
VS
TEMPERATURE**

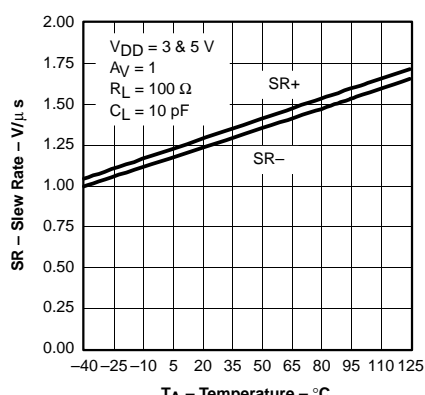


Figure 14

**TOTAL HARMONIC DISTORTION+NOISE
VS
FREQUENCY**

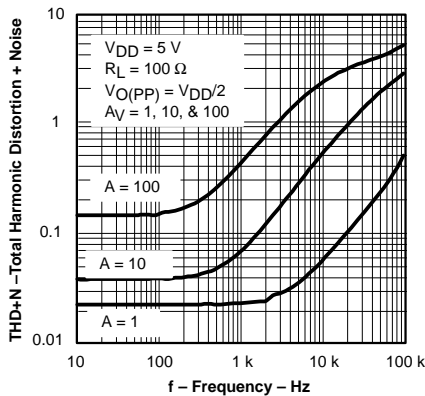


Figure 15

**EQUIVALENT INPUT VOLTAGE NOISE
VS
FREQUENCY**

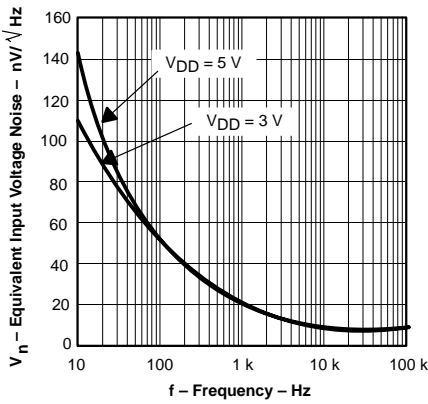


Figure 16

**PHASE MARGIN
VS
CAPACITIVE LOAD**

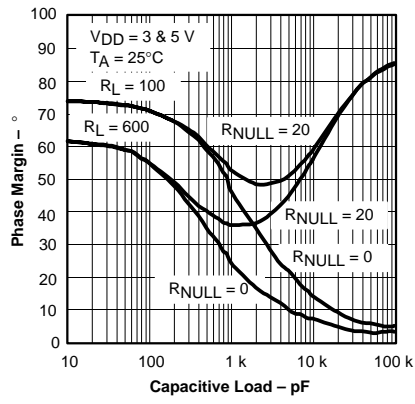


Figure 17

TLV4110, TLV4111, TLV4112, TLV4113 FAMILY OF HIGH OUTPUT DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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TYPICAL CHARACTERISTICS

**VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE**

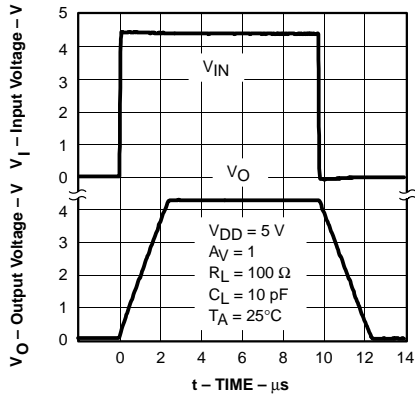


Figure 18

**VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE**

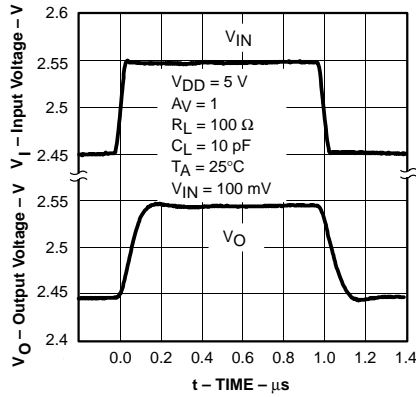


Figure 19

**INVERTING LARGE-SIGNAL
PULSE RESPONSE**

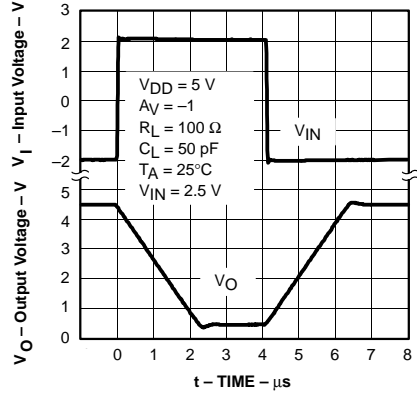


Figure 20

**INVERTING LARGE-SIGNAL
PULSE RESPONSE**

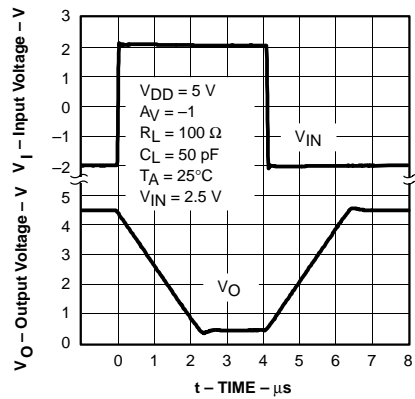


Figure 21

**SMALL-SIGNAL INVERTING
PULSE RESPONSE**

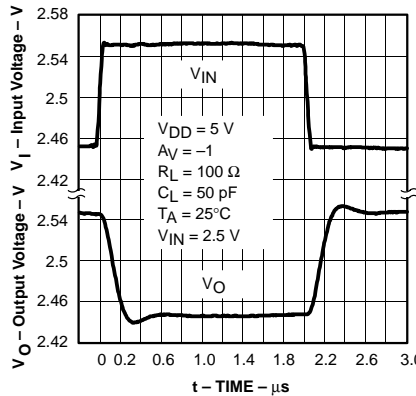


Figure 22

**CROSSTALK
vs
FREQUENCY**

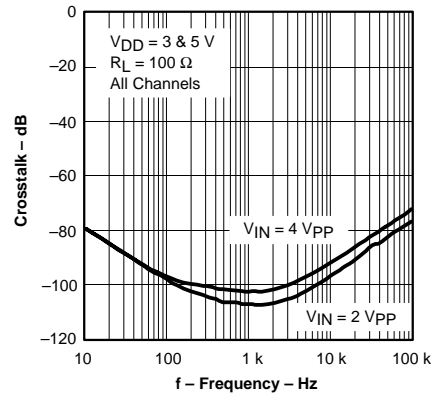


Figure 23

**SHUTDOWN FORWARD AND
REVERSE ISOLATION**

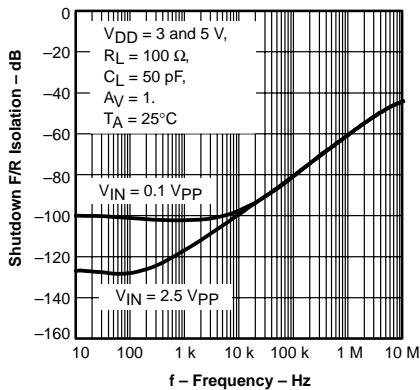


Figure 24

**SHUTDOWN SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

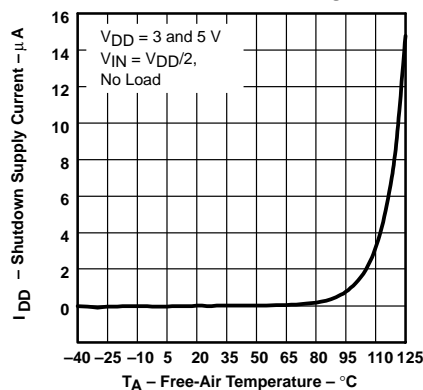


Figure 25

TYPICAL CHARACTERISTICS

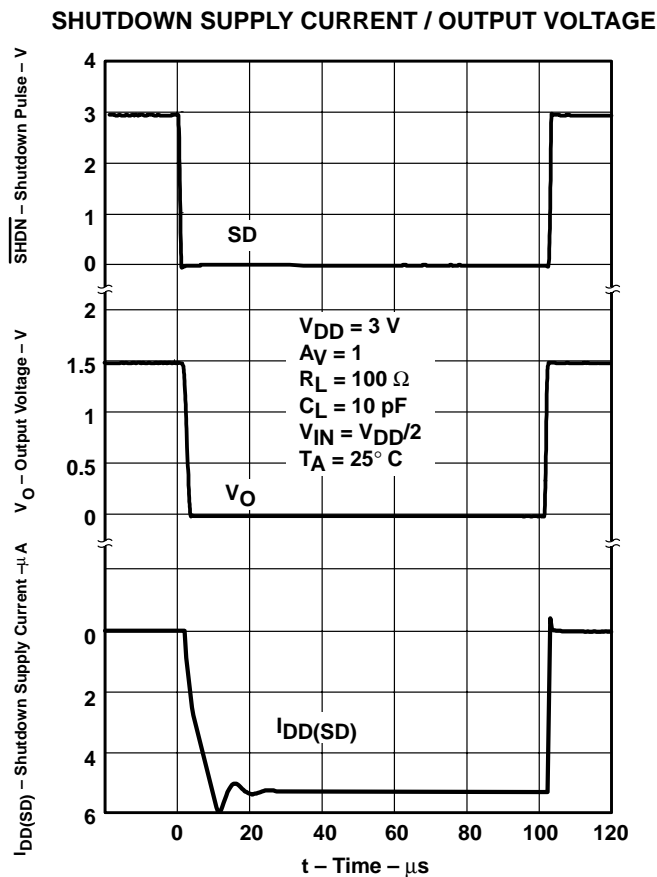


Figure 26

APPLICATION INFORMATION

shutdown function

Two members of the TLV411x family (TLV4110/3) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to just nano amps per channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. In order to save power in shutdown mode, an external pullup resistor is required, therefore, to enable the amplifier the shutdown terminal must be pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 1 nF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 27. A maximum value of 20 Ω should work well for most applications.

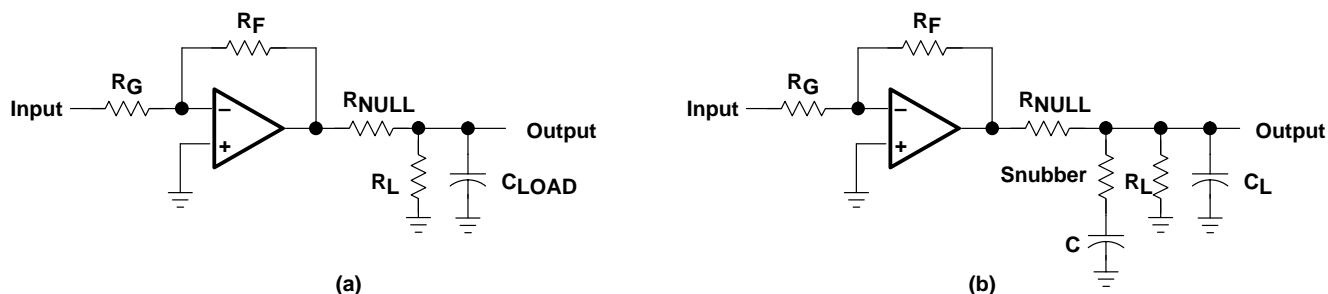


Figure 27. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

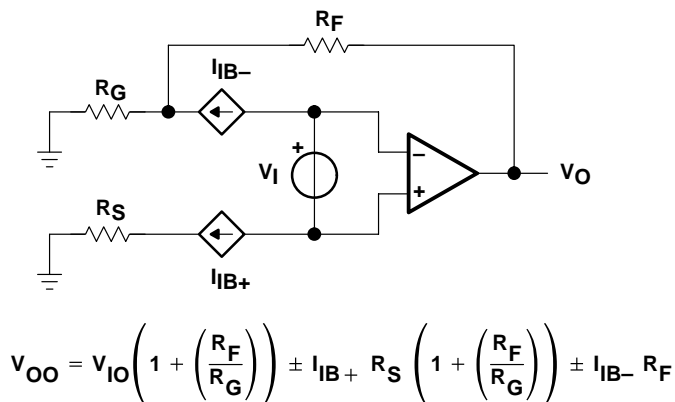


Figure 28. Output Offset Voltage Model

APPLICATION INFORMATION

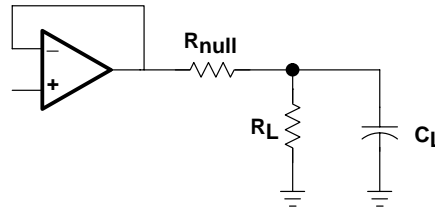


Figure 29

general power design considerations

When driving heavy loads at high junction temperatures there is an increased probability of electromigration affecting the long term reliability of ICs. Therefore for this not to be an issue either:

- The output current must be limited (at these high junction temperatures).
- or
- The junction temperature must be limited.

The maximum continuous output current at a die temperature 150°C will be 1/3 of the current at 105°C.

The junction temperature will be dependent on the ambient temperature around the IC, thermal impedance from the die to the ambient and power dissipated within the IC.

$$T_J = T_A + \theta_{JA} \times P_{DIS}$$

Where:

P_{DIS} is the IC power dissipation and is equal to the output current multiplied by the voltage dropped across the output of the IC.

θ_{JA} is the thermal impedance between the junction and the ambient temperature of the IC.

T_J is the junction temperature.

T_A is the ambient temperature.

Reducing one or more of these factors results in a reduced die temperature. The 8-pin SOIC (small outline integrated circuit) has a thermal impedance from junction to ambient of 176°C/W. For this reason it is recommended that the maximum power dissipation of the 8-pin SOIC package be limited to 350 mW, with peak dissipation of 700 mW as long as the RMS value is less than 350 mW.

The use of the MSOP PowerPAD™ dramatically reduces the thermal impedance from junction to case. And with correct mounting, the reduced thermal impedance greatly increases the IC's permissible power dissipation and output current handling capability. For example, the power dissipation of the PowerPAD™ is increased to above 1 W. Sinusoidal and pulse-width modulated output signals also increase the output current capability. The equivalent dc current is proportional to the square-root of the duty cycle:

$$I_{DC(EQ)} = I_{Cont} \times \sqrt{\text{duty cycle}}$$

CURRENT DUTY CYCLE AT PEAK RATED CURRENT	EQUIVALENT DC CURRENT AS A PERCENTAGE OF PEAK
100	100
70	84
50	71

Note that with an operational amplifier, a duty cycle of 70% would often result in the op amp sourcing current 70% of the time and sinking current 30%, therefore, the equivalent dc current would still be 0.84 times the continuous current rating at a particular junction temperature.

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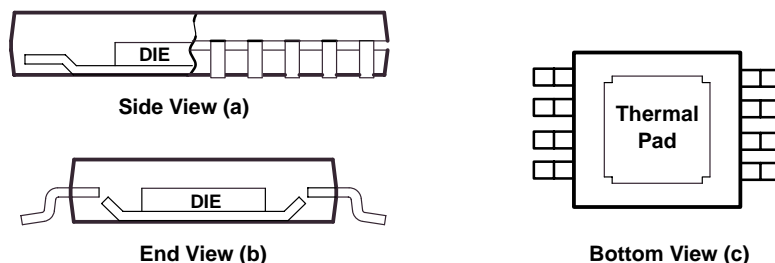
APPLICATION INFORMATION

general PowerPAD design considerations

The TLV411x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 30(a) and Figure 30(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 30(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 30. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

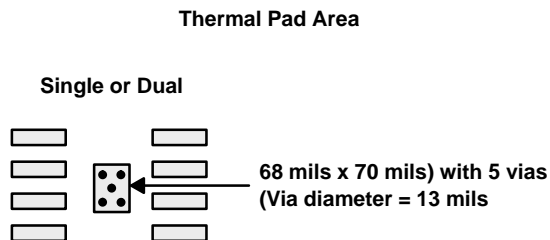


Figure 31. PowerPAD PCB Etch and Via Pattern

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

1. Prepare the PCB with a top side etch pattern as shown in Figure 31. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLV411x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLV411x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the TLV411x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA} , the maximum power dissipation is shown in Figure 32 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV411x IC (watts)

T_{MAX} = Absolute maximum junction temperature (150°C)

T_A = Free-ambient air temperature (°C)

θ_{JA} = $\theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case

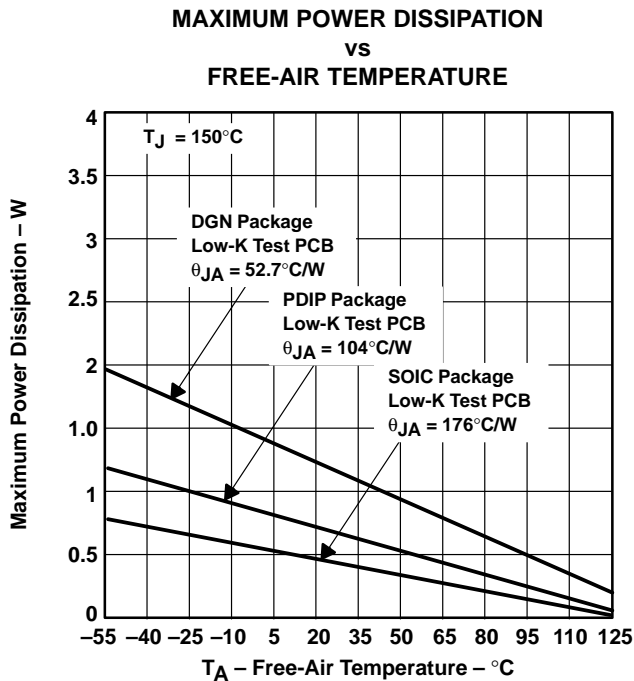
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

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general PowerPAD design considerations (continued)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 32. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.



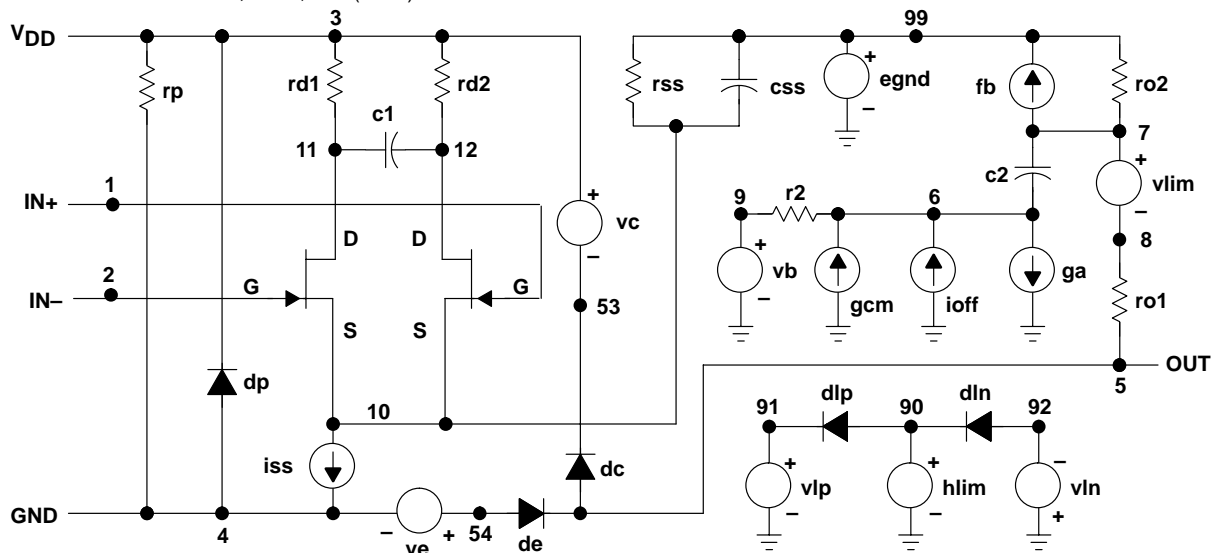
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*[™], the model generation software used with Microsim *PSpice*[™]. The Boyle macromodel (see Note 3) and subcircuit in Figure 33 are generated using the TLV411x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 3: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



* TLV4112_5V operational amplifier "macromodel" subcircuit
 * updated using Model Editor release 9.1 on 01/18/00 at 15:50
 Model Editor is an OrCAD product.

```

*
* connections: non-inverting input
*               | inverting input
*               | positive power supply
*               | negative power supply
*               | output
*
*
.subckt TLV4112_5V 1 2 3 4 5
*
c1      11   12   2.2439E-12
c2      6    7    10.000E-12
css     10   99   454.55E-15
dc      5    53   dc
de      54   5    dy
dlp     90   91   dx
dln     92   90   dx
dp      4    3    dx
egnd    99   0    poly(2) (3,0) (4,0) 0 .5 .5
fb      7    99   poly(5) vb vc ve vlp vln 0
+ 33.395E6 -1E3 1E3 33E6 -33E6
ga      6    0    11   12 168.39E-6
gcm     0    6    10   99 168.39E-12
    
```

```

iss     10   4    dc      13.800E-6
hlim    90   0    vlim 1K
ioff    0    6    dc      75E-9
j1      11   2    10 jx1
j2      12   1    10 jx2
r2      6    9    100.00E3
rd1     3    11   5.9386E3
rd2     3    12   5.9386E3
ro1     8    5    10
ro2     7    99   10
rp      3    4    3.3333E3
rss     10   99   14.493E6
vb      9    0    dc 0
vc      3    53   dc .86795
ve      54   4    dc .86795
vlim    7    8    dc 0
vlp     91   0    dc 300
vln     0    92   dc 300
.model  dx    D(Is=800.00E-18)
.model  dy    D(Is=800.00E-18 Rs=1m Cjo=10p)
.model  jx1   NJF(Is=150.00E-12 Beta=2.0547E-3 +Vto=-1)
.model  jx2   NJF(Is=150.00E-12 Beta=2.0547E-3 +Vto=-1)
.ends
*$
    
```

Figure 33. Boyle Macromodel and Subcircuit

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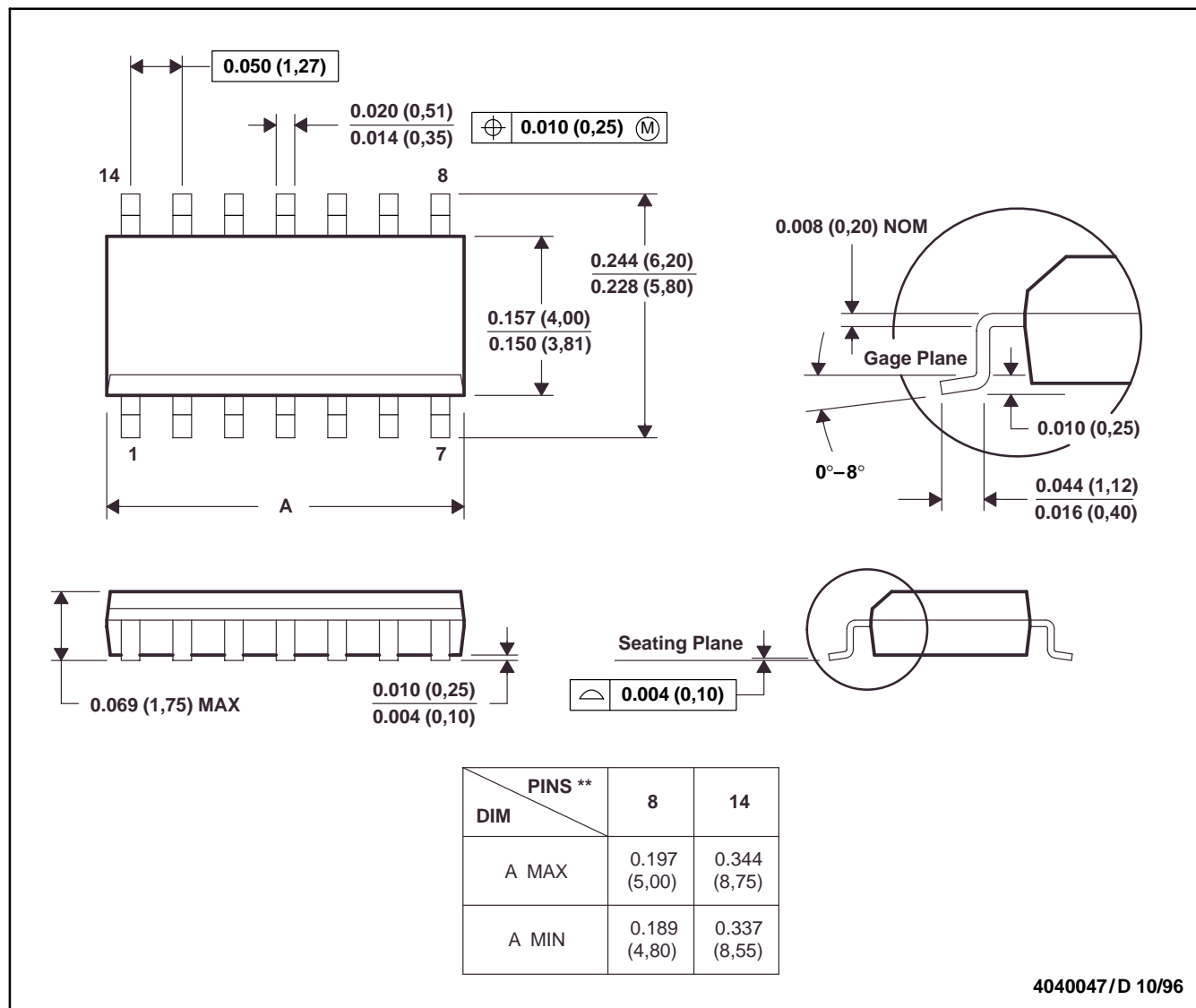
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MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

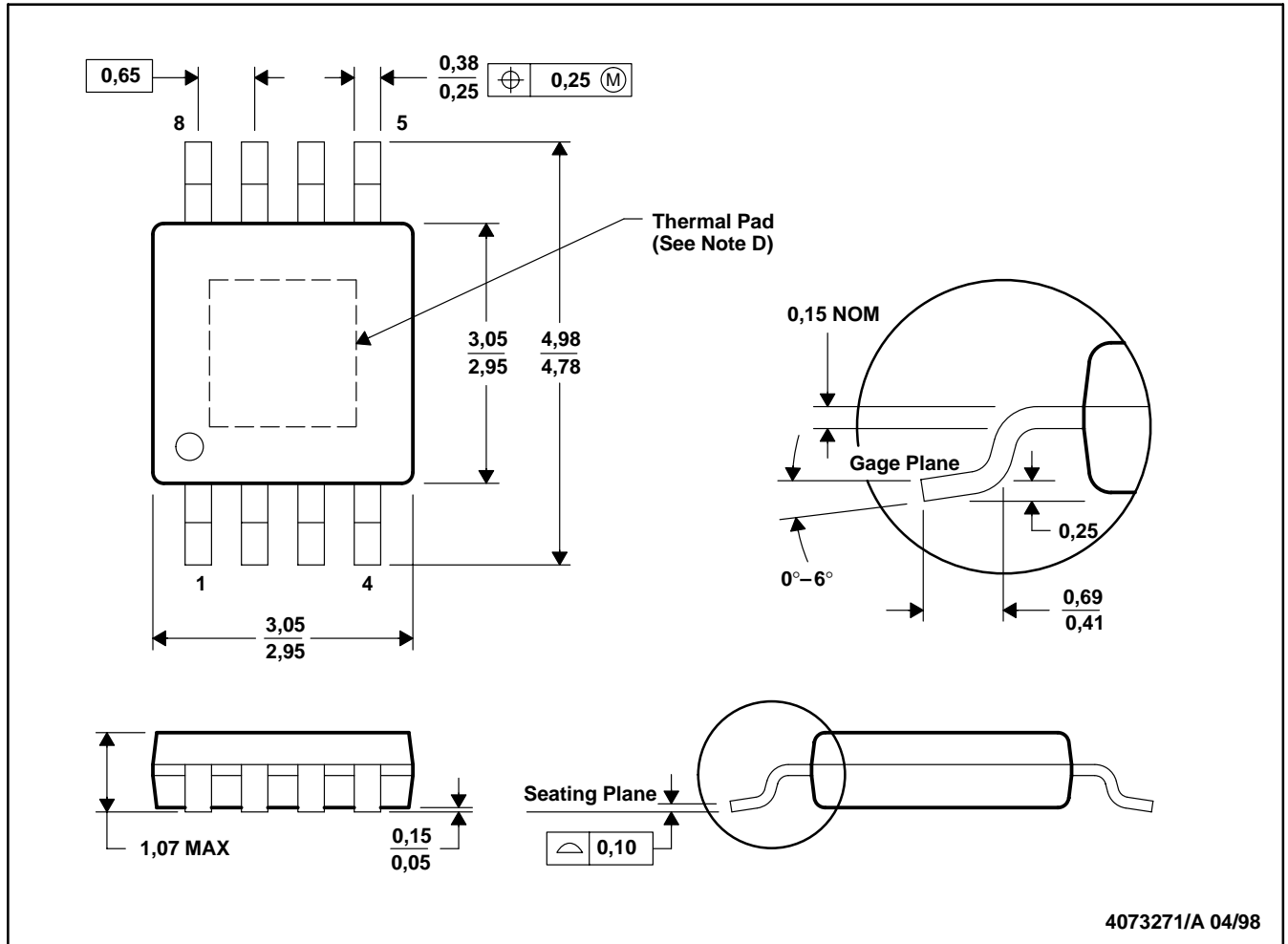
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MECHANICAL INFORMATION

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusions.
 D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 E. Falls within JEDEC MO-187

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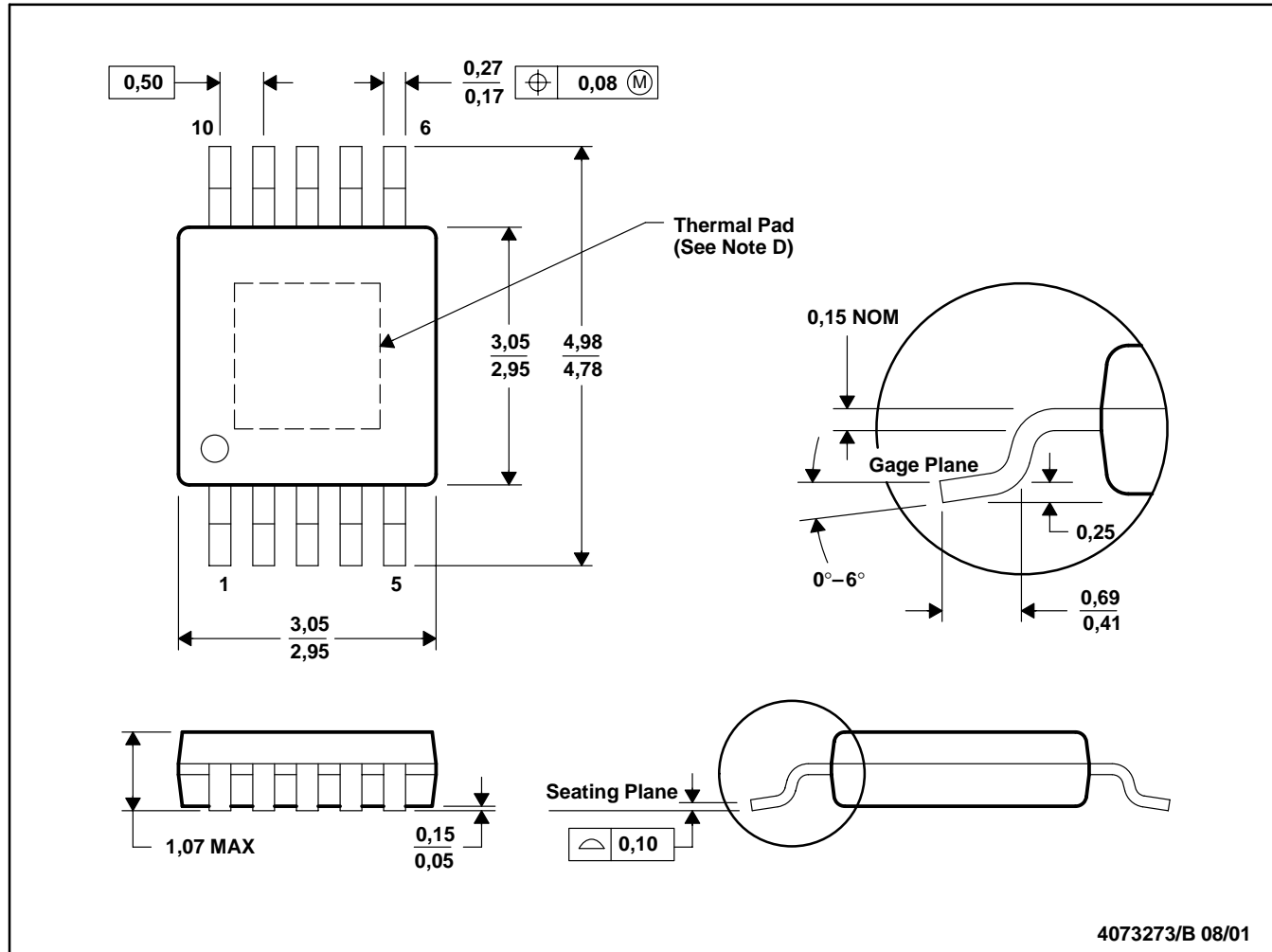
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MECHANICAL INFORMATION

DGQ (S-PDSO-G10)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



4073273/B 08/01

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
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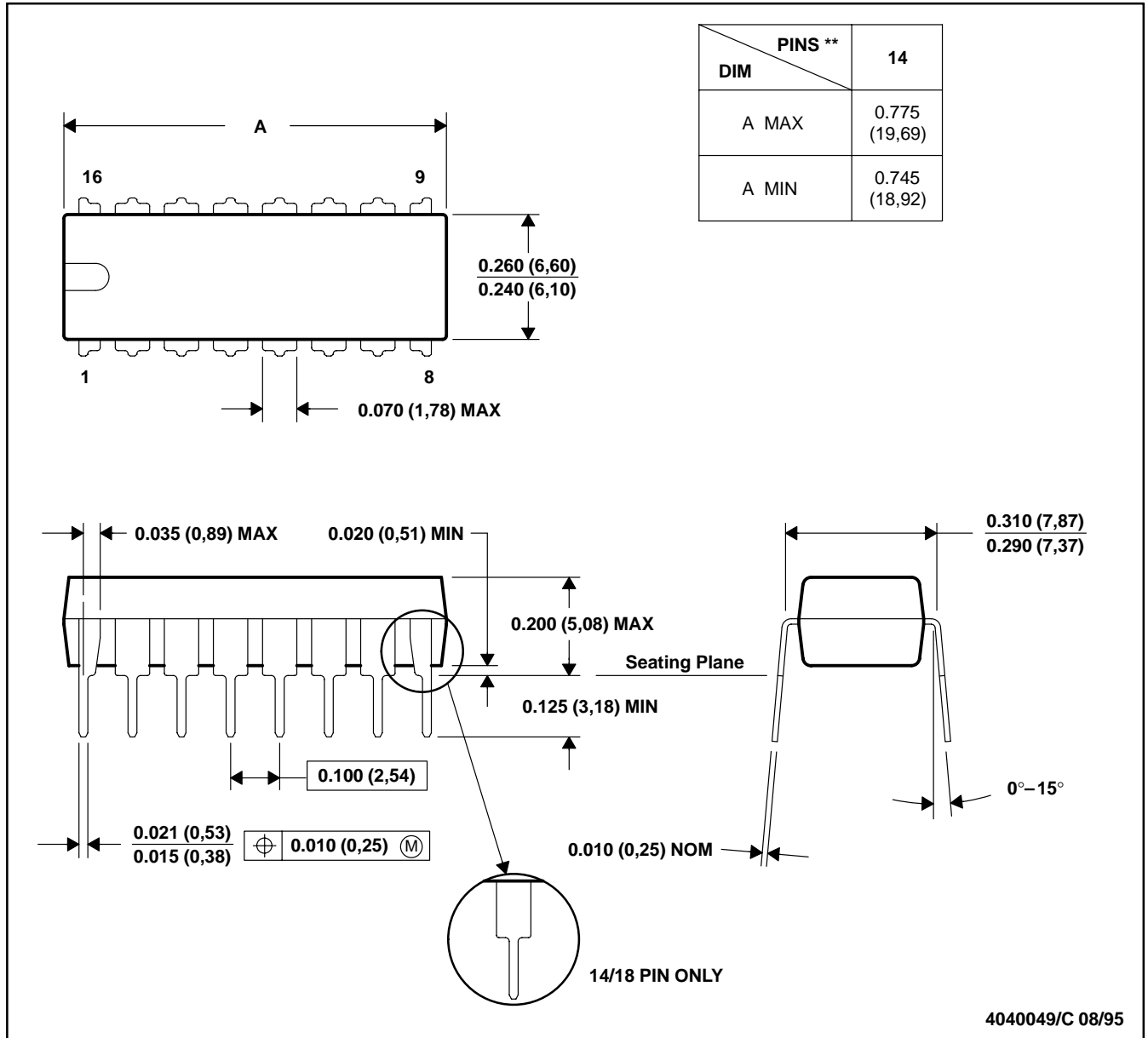
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MECHANICAL INFORMATION

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

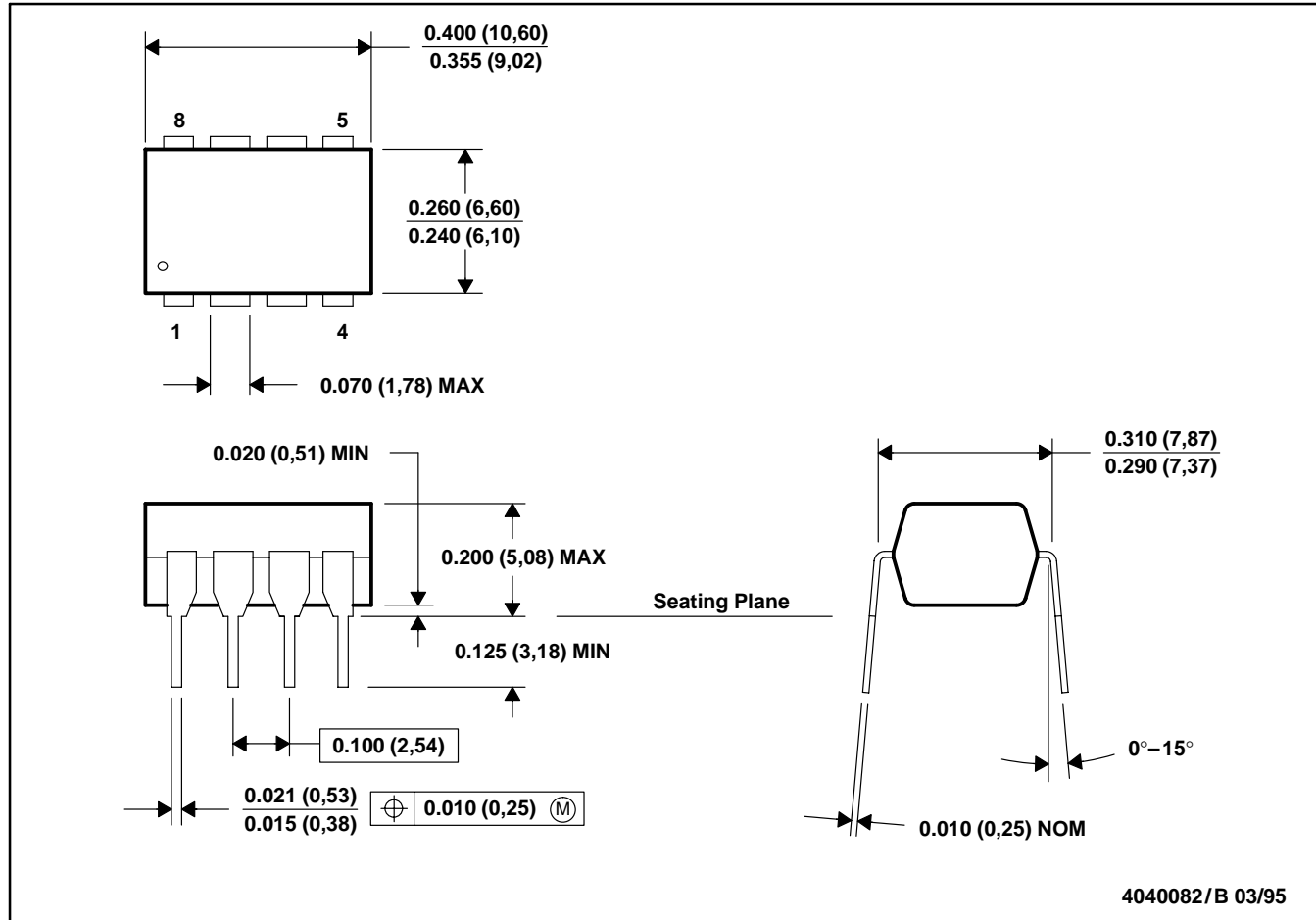
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MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

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