

# TPS3617-50 BATTERY-BACKUP SUPERVISOR FOR RAM RETENTION

SLVS339B – DECEMBER 2000 – REVISED DECEMBER 2002

- Supply Current of 40  $\mu\text{A}$  (Max)
- Battery Supply Current of 100 nA (Max)
- Precision 5-V Supply Voltage Monitor, Other Voltage Options on Request
- Backup-Battery Voltage Can Exceed  $V_{\text{DD}}$
- Watchdog Timer With 800-ms Time-Out
- Power-On Reset Generator With Fixed 100-ms Reset Delay Time
- Voltage Monitor for Power-Fail or Low-Battery Monitoring
- Battery Freshness Seal
- 8-Pin MSOP Package
- Temperature Range . . .  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

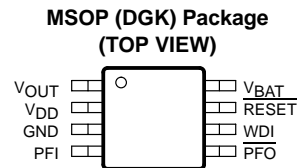
## typical applications

- Fax Machines
- Set-Top Boxes
- Advanced Voice Mail Systems
- Portable Battery Powered Equipment
- Computer Equipment
- Advanced Modems
- Automotive Systems
- Portable Long-Time Monitoring Equipment
- Point of Sale Equipment

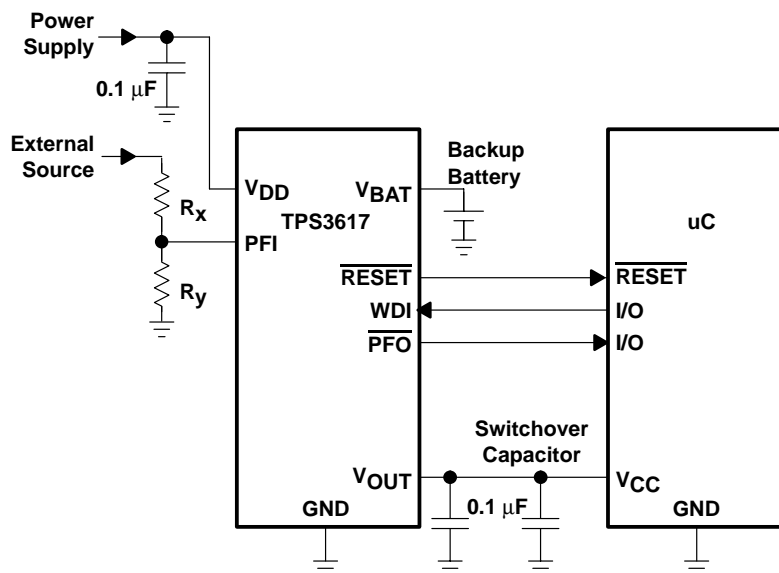
## description

The TPS3617-50 supervisory circuit monitors and controls processor activity by providing backup-battery switchover for data retention of CMOS RAM.

During power on,  $\overline{\text{RESET}}$  is asserted when the supply voltage ( $V_{\text{DD}}$  or  $V_{\text{BAT}}$ ) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors  $V_{\text{DD}}$  and keeps  $\overline{\text{RESET}}$  output active as long as  $V_{\text{DD}}$  remains below the threshold voltage ( $V_{\text{IT}}$ ). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after  $V_{\text{DD}}$  has risen above the threshold voltage ( $V_{\text{IT}}$ ).



## typical operating circuit



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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## description (continued)

When the supply voltage drops below the threshold voltage ( $V_{IT}$ ), the output becomes active (low) again.

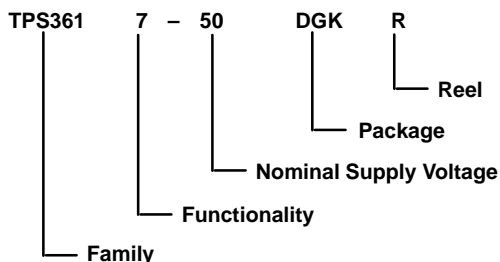
The product spectrum is designed for supply voltages of 5.0 V. The TPS3617-50 is available in a 8-pin MSOP package and is characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### PACKAGE INFORMATION

$T_A$	DEVICE NAME	MARKING
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	TPS3617-50DGKR†	ASD

† The DGKR passive indicates tape and reel of 2500 parts.

## ordering information application specific versions



DEVICE NAME	NOMINAL VOLTAGE‡, $V_{NOM}$
TPS3617-50 DGK	5 V

‡ For other threshold voltages, contact the local TI sales office for availability and lead-time.

### FUNCTION TABLE

$V_{DD} > V_{IT}$	$V_{DD} > V_{BAT}$	$V_{OUT}$	$\overline{\text{RESET}}$
0	0	$V_{BAT}$	0
0	1	$V_{DD}$	0
1	0	$V_{DD}$	1
1	1	$V_{DD}$	1

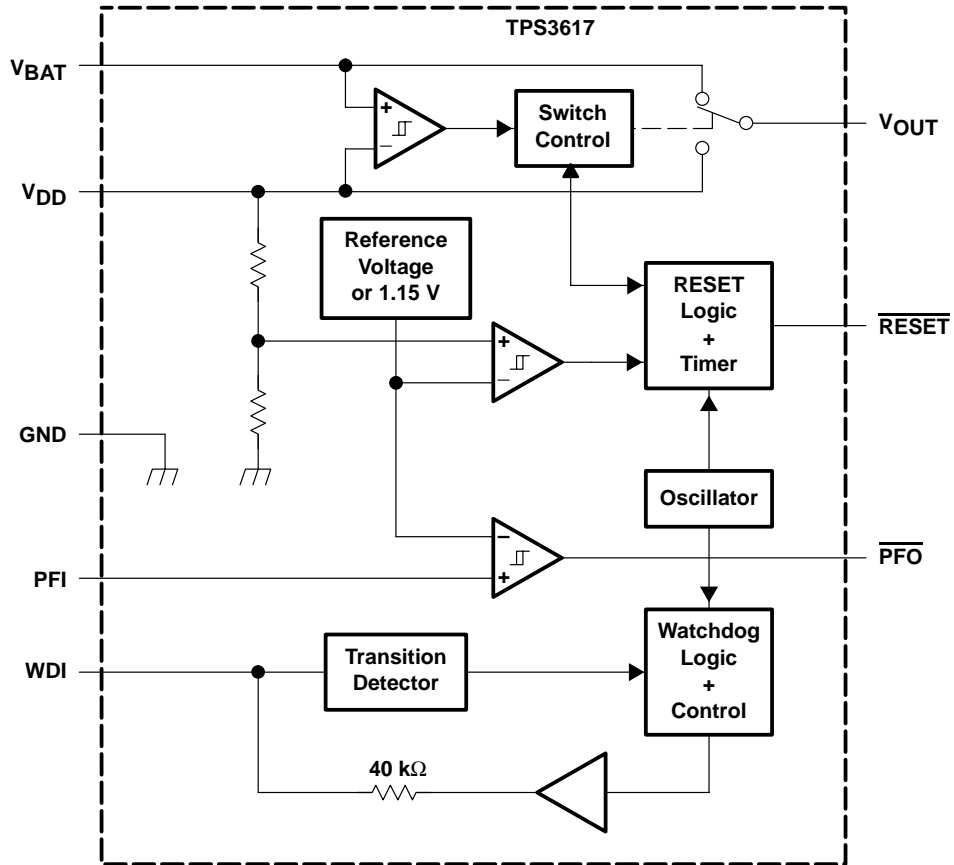
$PFI > V_{PFI}$	$\overline{\text{PFO}}$
0	0
1	1

CONDITION:  $V_{DD} > V_{DD(\text{min})}$

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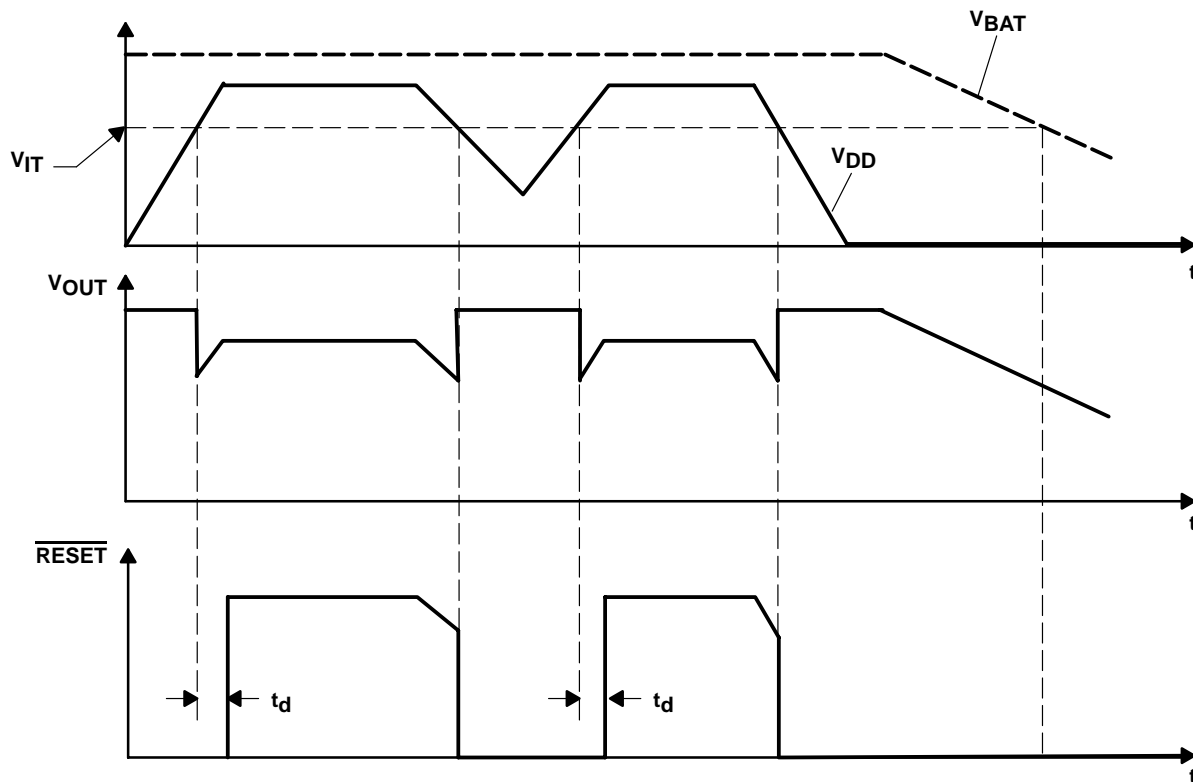
**functional schematic**



# TPS3617-50 BATTERY-BACKUP SUPERVISOR FOR RAM RETENTION

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## timing diagram



## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	3	I	Ground
PFI	4	I	Power-fail comparator input
PFO	5	O	Power-fail comparator output
RESET	7	O	Active-low reset output
VBAT	8	I	Backup-battery input
VDD	2	I	Input supply voltage
VOUT	1	O	Supply output
WDI	6	I	Watchdog input

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## detailed description

### battery freshness seal

The battery freshness seal of the TPS3617 family disconnects the backup battery from the internal circuitry until it is needed. This ensures that the backup battery connected to  $V_{BAT}$  should be fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect  $V_{BAT}$  ( $V_{BAT} > V_{BAT(min)}$ )
2. Ground  $\overline{PFO}$
3. Connect PFI to  $V_{DD}$  ( $PFI = V_{DD}$ )
4. Connect  $V_{DD}$  to power supply ( $V_{DD} > V_{IT}$ ) and keep connected for  $5\text{ ms} < t < 35\text{ ms}$

The battery freshness seal mode is disabled by the positive-going edge of  $\overline{RESET}$  when  $V_{DD}$  is applied.

### power-fail comparator (PFI and $\overline{PFO}$ )

An additional comparator monitors voltages other than the nominal supply voltage. The power-fail-input (PFI) can be compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold ( $V_{(PFI)}$ ) of 1.15 V typical, the power-fail output ( $\overline{PFO}$ ) goes low. If it goes above  $V_{(PFI)}$  plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors it is possible to supervise any voltages above  $V_{(PFI)}$ . The sum of both resistors should be about 1 M $\Omega$ , to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of the sensed voltage. If the power-fail comparator is unused, connect PFI to ground and leave the  $\overline{PFO}$  unconnected.

### watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or DSP has to toggle the watchdog input within 0.8 s typically, to avoid a time out from occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected, the watchdog is disabled and should be retriggered internally.

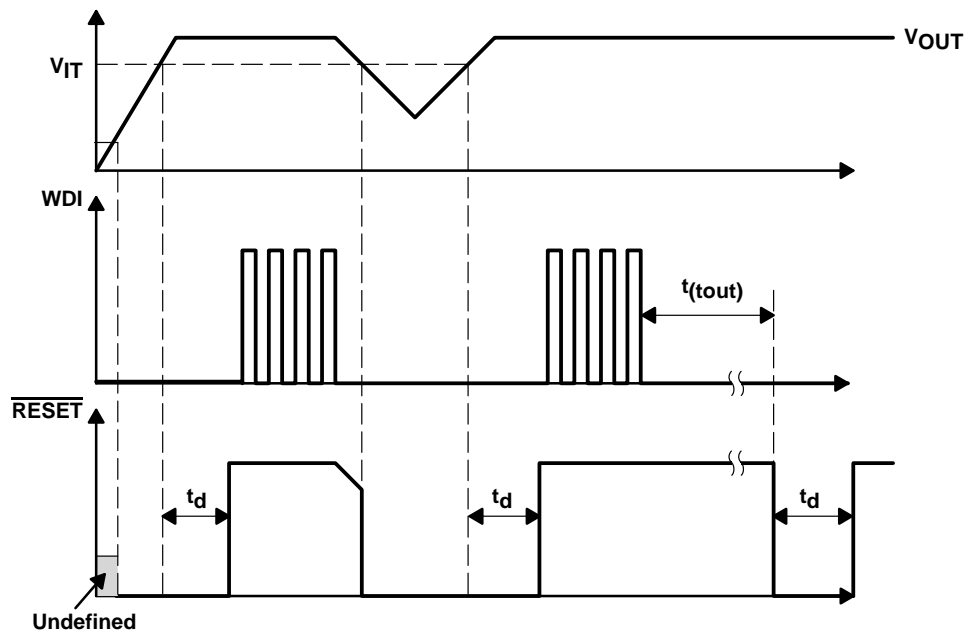
### saving current while using the watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead, WDI is externally driven high for the majority of the time-out period, a current of e.g.  $5.0\text{ V}/40\text{ k}\Omega \approx 125\text{ }\mu\text{A}$  can flow into WDI.

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**detailed description (continued)**



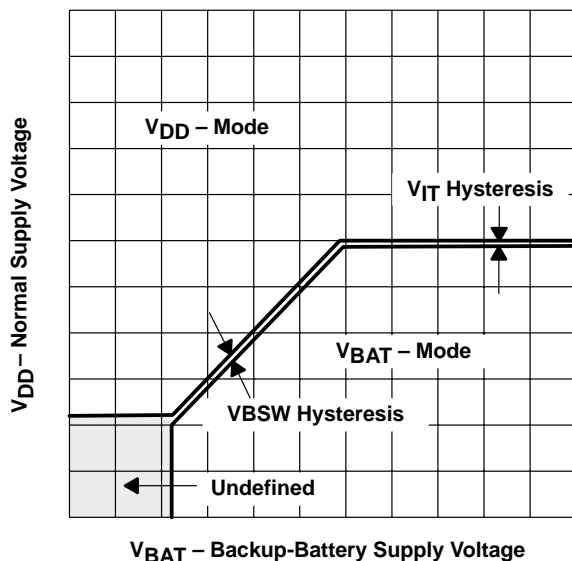
**Figure 1. Watchdog Timing**

**backup-battery switchover**

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at  $V_{BAT}$ , the device automatically switches the connected RAM to backup power when  $V_{DD}$  fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than  $V_{DD}$ , these supervisors should not connect  $V_{BAT}$  to  $V_{OUT}$  when  $V_{BAT}$  is greater than  $V_{DD}$ .  $V_{BAT}$  only connects to  $V_{OUT}$  (through a 15- $\Omega$  switch) when  $V_{DD}$  falls below  $V_{IT}$  and  $V_{BAT}$  is greater than  $V_{DD}$ . When  $V_{DD}$  recovers, switchover is deferred either until  $V_{DD}$  crosses  $V_{BAT}$ , or until  $V_{DD}$  rises above the reset threshold  $V_{IT}$ .  $V_{OUT}$  connects to  $V_{DD}$  through a 1- $\Omega$  (max) PMOS switch when  $V_{DD}$  crosses the reset threshold.

$V_{DD} > V_{BAT}$	$V_{DD} > V_{IT}$	$V_{OUT}$
1	1	$V_{DD}$
1	0	$V_{DD}$
0	1	$V_{DD}$
0	0	$V_{BAT}$

**backup-battery switchover (continued)**



**Figure 2.  $V_{DD} - V_{BAT}$  Switchover**

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage: $V_{DD}$ (see Note1) .....	7 V
PFI pin (see Note 1) .....	-0.3 V to ( $V_{DD} + 0.3$ V)
Continuous output current at $V_{OUT}$ : $I_O$ .....	400 mA
All other pins, $I_O$ .....	$\pm 10$ mA
Continuous total power dissipation .....	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ .....	-40°C to 85°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than  $t=1000h$  continuously.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
	POWER RATING	ABOVE $T_A = 25^\circ\text{C}$	POWER RATING	POWER RATING
DGK	470 mW	3.76 mW/°C	301 mW	241 mW

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## recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$	1.65	5.5	V
Battery supply voltage, $V_{BAT}$	1.5	5.5	V
Input voltage, $V_I$	0	$V_{DD} + 0.3$	V
High-level input voltage, $V_{IH}$	$0.7 \times V_{DD}$		V
Low-level input voltage, $V_{IL}$	$0.3 \times V_{DD}$		V
Continuous output current at $V_{OUT}$ , $I_O$	300		mA
Input transition rise and fall rate at $\overline{MR}$ , $\Delta t/\Delta V$ , $WDI$	100		ns/V
Slew rate at $V_{DD}$ or $V_{BAT}$	1		V/ $\mu$ s
Operating free-air temperature range, $T_A$	-40	85	$^{\circ}$ C

## electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$\overline{RESET}$	$V_{DD} = 1.8$ V, $I_{OH} = -400$ $\mu$ A	$V_{DD} - 0.2$ V		V
			$V_{DD} = 3.3$ V, $I_{OH} = -2$ mA	$V_{DD} - 0.4$ V		
			$V_{DD} = 5$ V, $I_{OH} = -3$ mA			
		$\overline{PFO}$	$V_{DD} = 1.8$ V, $I_{OH} = -20$ $\mu$ A	$V_{DD} - 0.3$ V		
			$V_{DD} = 3.3$ V, $I_{OH} = -80$ $\mu$ A	$V_{DD} - 0.4$ V		
			$V_{DD} = 5$ V, $I_{OH} = -120$ $\mu$ A			
$V_{OL}$	Low-level output voltage	$\overline{RESET}$ $\overline{PFO}$	$V_{DD} = 1.8$ V, $I_{OL} = 400$ $\mu$ A	0.2		V
			$V_{DD} = 3.3$ V, $I_{OL} = 2$ mA	0.4		
			$V_{DD} = 5$ V, $I_{OL} = 3$ mA			
$V_{res}$	Power-up reset voltage (see Note 2)	$V_{BAT} > 1.1$ V, or $V_{DD} > 1.1$ V, $I_{OL} = 20$ $\mu$ A	0.4		V	
$V_{OUT}$	Normal mode		$I_O = 8.5$ mA, $V_{DD} = 1.8$ V, $V_{BAT} = 0$ V	$V_{DD} - 50$ mV		V
			$I_O = 125$ mA, $V_{DD} = 3.3$ V, $V_{BAT} = 0$ V	$V_{DD} - 150$ mV		
			$I_O = 200$ mA, $V_{DD} = 5$ V, $V_{BAT} = 0$ V	$V_{DD} - 200$ mV		
	Battery-backup mode		$I_O = 0.5$ mA, $V_{BAT} = 1.5$ V, $V_{DD} = 0$ V	$V_{BAT} - 20$ mV		
			$I_O = 7.5$ mA, $V_{BAT} = 3.3$ V, $V_{DD} = 0$ V	$V_{BAT} - 113$ mV		

NOTE 2: The lowest supply voltage at which  $\overline{RESET}$  becomes active.  $t_r$ ,  $V_{DD} \geq 15$   $\mu$ s/V.

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**electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
R <sub>DSt(on)</sub>	V <sub>DD</sub> to V <sub>OUT</sub> on-resistance	V <sub>DD</sub> = 5 V		0.6	1	Ω	
	V <sub>BAT</sub> to V <sub>OUT</sub> on-resistance	V <sub>BAT</sub> = 3.3 V		8	15		
V <sub>IT</sub>	Negative-going input threshold voltage (see Note 3)	TPS3617-50	T <sub>A</sub> = -40°C to 85°C	4.46	4.55	4.64	V
V <sub>PFI</sub>		PFI		1.13	1.15	1.17	
V <sub>hys</sub>	Hysteresis	V <sub>IT</sub>	1.65 V < V <sub>IT</sub> < 2.5 V	20		mV	
			2.5 V < V <sub>IT</sub> < 3.5 V	40			
			3.5 V < V <sub>IT</sub> < 5.5 V	60			
		PFI	12				
	V <sub>BSW</sub> (see Note 4)	V <sub>DD</sub> = 1.8 V	55				
I <sub>IH</sub>	High-level input current	WDI (see Note 5)	WDI = V <sub>DD</sub> = 5 V	150		μA	
I <sub>IL</sub>	Low-level input current		WDI = 0 V, V <sub>DD</sub> = 5 V	-150			
I <sub>I</sub>	Input current	PFI	V <sub>I</sub> < V <sub>DD</sub>	-25	25	nA	
I <sub>OS</sub>	Short-circuit current	PFO	PFO = 0 V, V <sub>DD</sub> = 1.8 V	-0.3		mA	
			PFO = 0 V, V <sub>DD</sub> = 3.3 V	-1.1			
			PFO = 0 V, V <sub>DD</sub> = 5 V	-2.4			
I <sub>DD</sub>	V <sub>DD</sub> supply current		V <sub>OUT</sub> = V <sub>DD</sub>	40		μA	
			V <sub>OUT</sub> = V <sub>BAT</sub>	40			
I <sub>BAT</sub>	V <sub>BAT</sub> supply current		V <sub>OUT</sub> = V <sub>DD</sub>	-0.1	0.1	μA	
			V <sub>OUT</sub> = V <sub>BAT</sub>	0.5			
C <sub>i</sub>	Input capacitance		V <sub>I</sub> = 0 V to 5 V	5		pF	

NOTES: 3. To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near to the supply terminals.

4. For V<sub>DD</sub> < 1.6 V, V<sub>OUT</sub> switches to V<sub>BAT</sub> regardless of V<sub>BAT</sub>.

5. For details on how to optimize current consumption when using WDI, refer to *detailed watchdog* description.

**timing requirements at R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = -40°C to 85°C**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>w</sub>	Pulse width	V <sub>DD</sub>	V <sub>IH</sub> = V <sub>IT</sub> + 0.2 V,	V <sub>IL</sub> = V <sub>IT</sub> - 0.2 V		6	μs
		WDI	V <sub>DD</sub> > V <sub>IT</sub> + 0.2 V	V <sub>IL</sub> = 0.3 x V <sub>DD</sub> ,	V <sub>IH</sub> = 0.7 x V <sub>DD</sub>	100	ns

**switching characteristics at R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = -40 °C to 85 °C**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>d</sub>	Delay time	V <sub>DD</sub> ≥ V <sub>IT</sub> + 0.2 V, See timing diagram	60	100	140	ms	
t <sub>(tout)</sub>	Watchdog time-out	V <sub>DD</sub> > V <sub>IT</sub> + 0.2 V, See timing diagram	0.48	0.8	1.12	s	
t <sub>PHL</sub>	Propagation (delay) time, high-to-low-level output	V <sub>DD</sub> to $\overline{\text{RESET}}$	V <sub>IL</sub> = V <sub>IT</sub> - 0.2 V, V <sub>IH</sub> = V <sub>IT</sub> + 0.2 V	2		5	μs
		PFI to $\overline{\text{PFO}}$	V <sub>IL</sub> = V <sub>PFI</sub> - 0.2 V, V <sub>IH</sub> = V <sub>PFI</sub> + 0.2 V	3		5	
	Transition time	V <sub>DD</sub> to V <sub>BAT</sub>			3		



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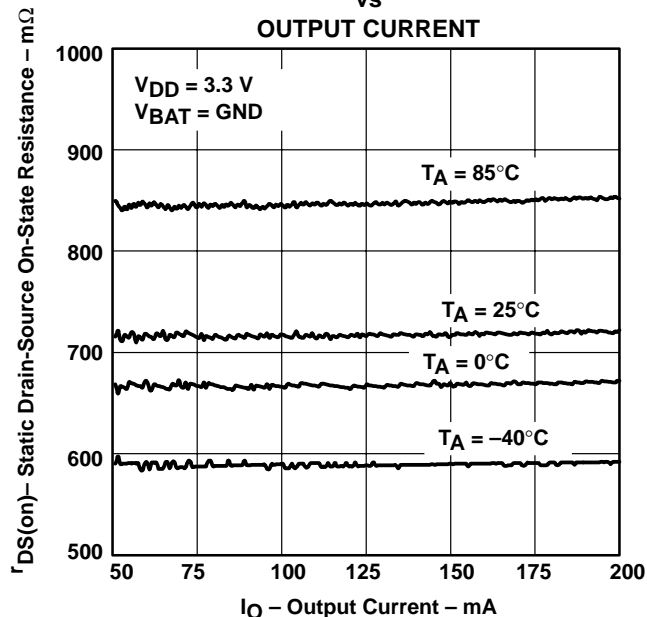
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**TYPICAL CHARACTERISTICS**

**Table of Graphs**

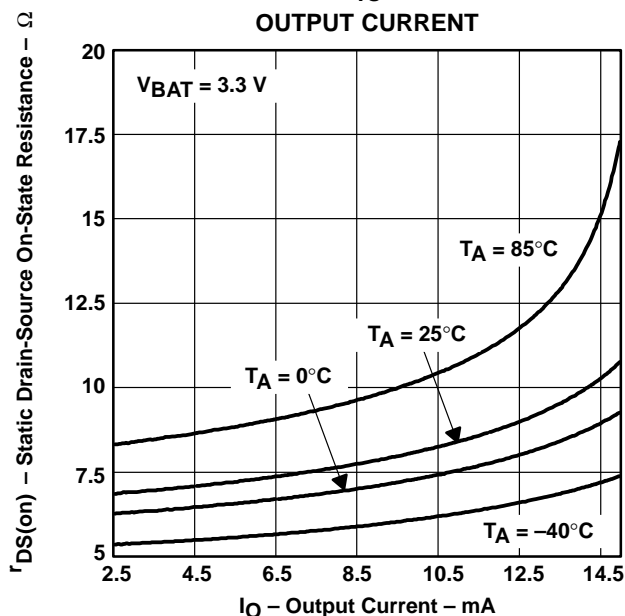
			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance ( $V_{DD}$ to $V_{OUT}$ )	vs Output current	3
	Static drain-source on-state resistance ( $V_{BAT}$ to $V_{OUT}$ )	vs Output current	4
$I_{DD}$	Supply current	vs Supply voltage	5
$V_{IT}$	Input threshold voltage at $\overline{RESET}$	vs Free-air temperature	6
$V_{OH}$	High-level output voltage at $\overline{RESET}$	vs High-level output current	7, 8
	High-level output voltage at $\overline{PFO}$		9, 10
$V_{OL}$	Low-level output voltage at $\overline{RESET}$	vs Low-level output current	11, 12
	Minimum pulse duration at $V_{DD}$	vs Threshold voltage overdrive at $V_{DD}$	13
	Minimum pulse duration at PFI	vs Threshold voltage overdrive at PFI	14

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE**  
**( $V_{DD}$  to  $V_{OUT}$ )**  
**vs**  
**OUTPUT CURRENT**



**Figure 3**

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE**  
**( $V_{BAT}$  to  $V_{OUT}$ )**  
**vs**  
**OUTPUT CURRENT**



**Figure 4**

TYPICAL CHARACTERISTICS

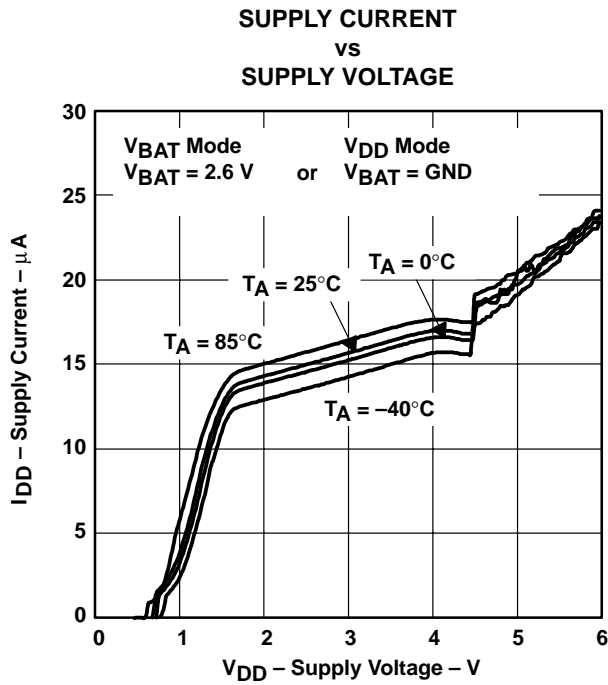


Figure 5

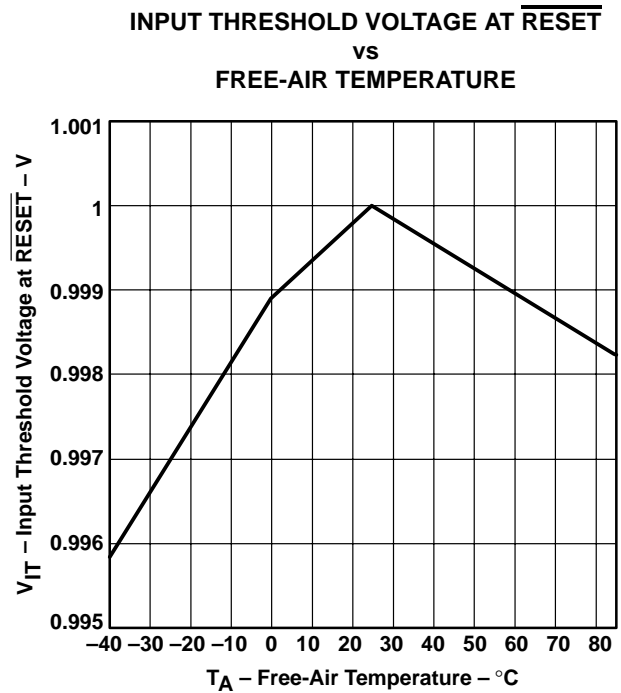


Figure 6

**HIGH-LEVEL OUTPUT VOLTAGE AT  $\overline{RESET}$   
vs  
HIGH-LEVEL OUTPUT CURRENT**

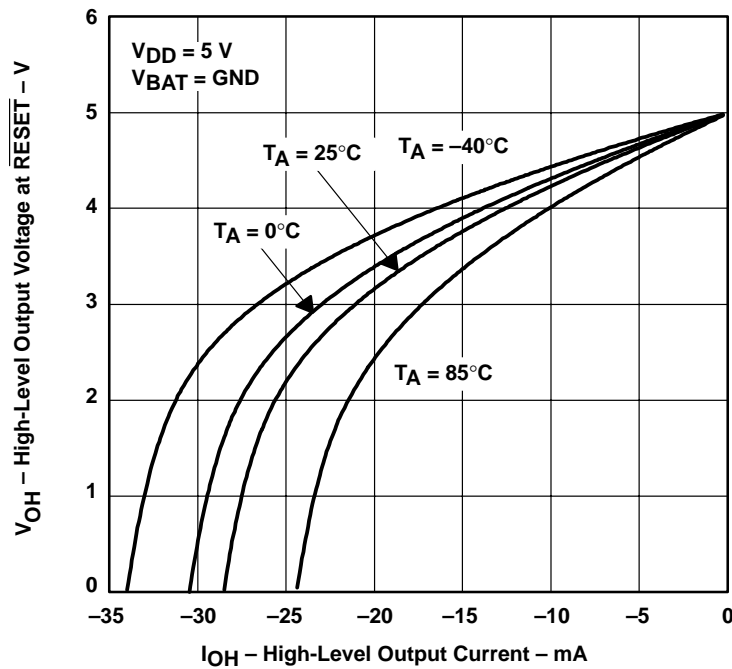


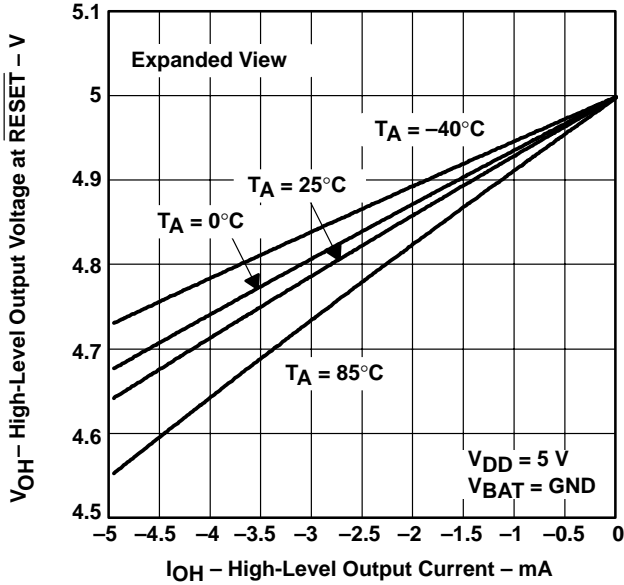
Figure 7

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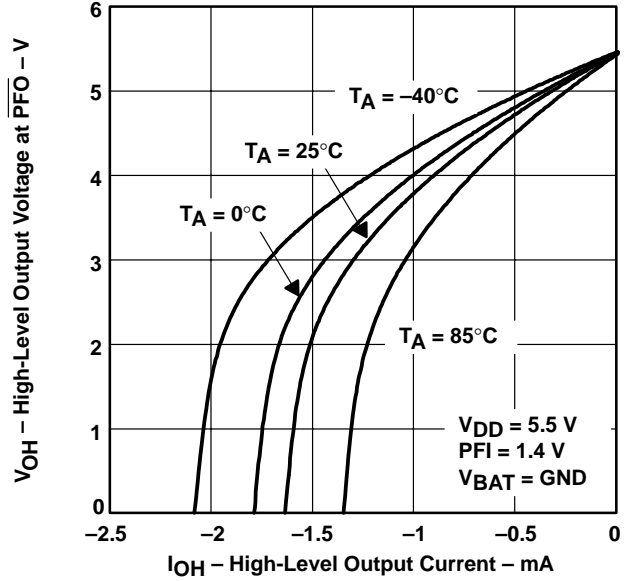
**TYPICAL CHARACTERISTICS**

**HIGH-LEVEL OUTPUT VOLTAGE AT RESET**  
**vs**  
**HIGH-LEVEL OUTPUT CURRENT**



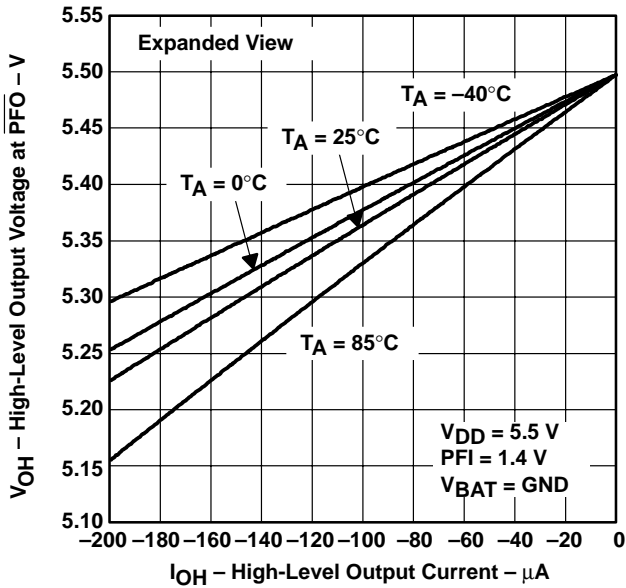
**Figure 8**

**HIGH-LEVEL OUTPUT VOLTAGE AT PFO**  
**vs**  
**HIGH-LEVEL OUTPUT CURRENT**



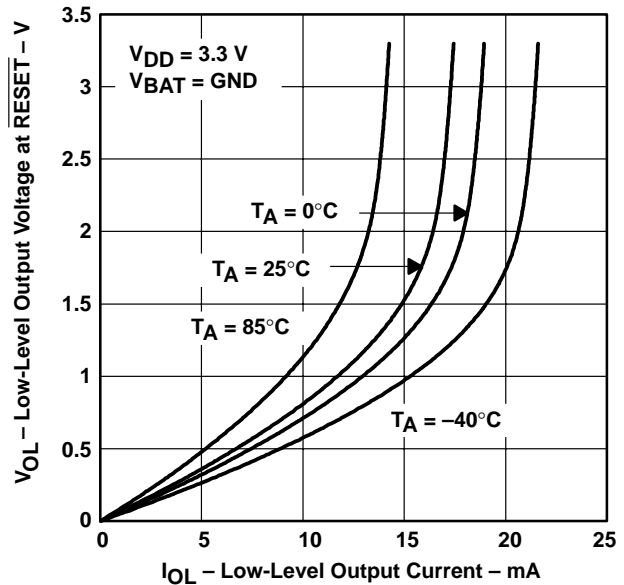
**Figure 9**

**HIGH-LEVEL OUTPUT VOLTAGE AT PFO**  
**vs**  
**HIGH-LEVEL OUTPUT CURRENT**



**Figure 10**

**LOW-LEVEL OUTPUT VOLTAGE AT RESET**  
**vs**  
**LOW-LEVEL OUTPUT CURRENT**



**Figure 11**



TYPICAL CHARACTERISTICS

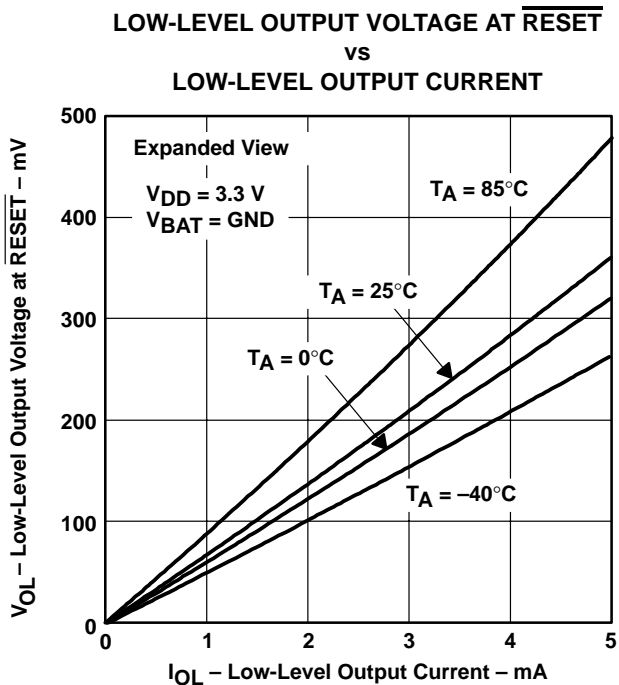


Figure 12

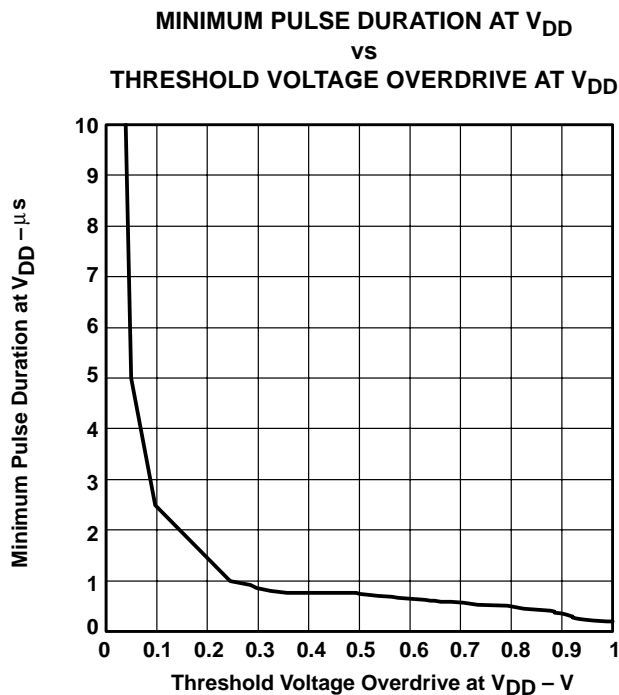


Figure 13

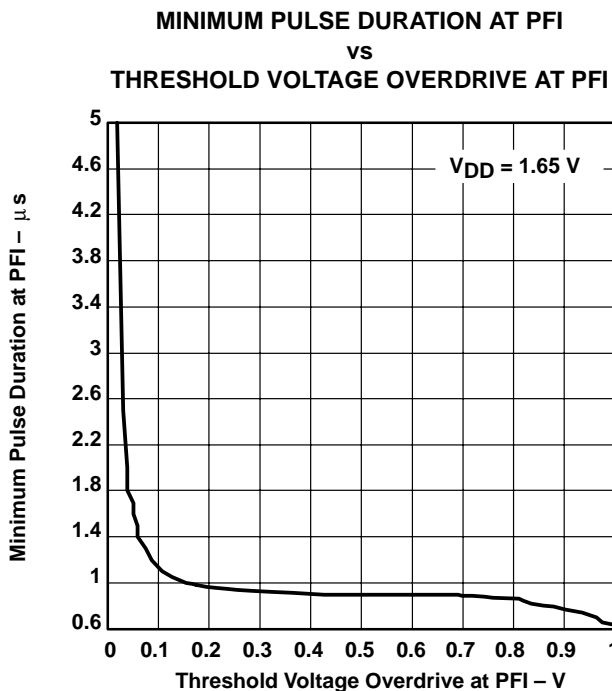


Figure 14

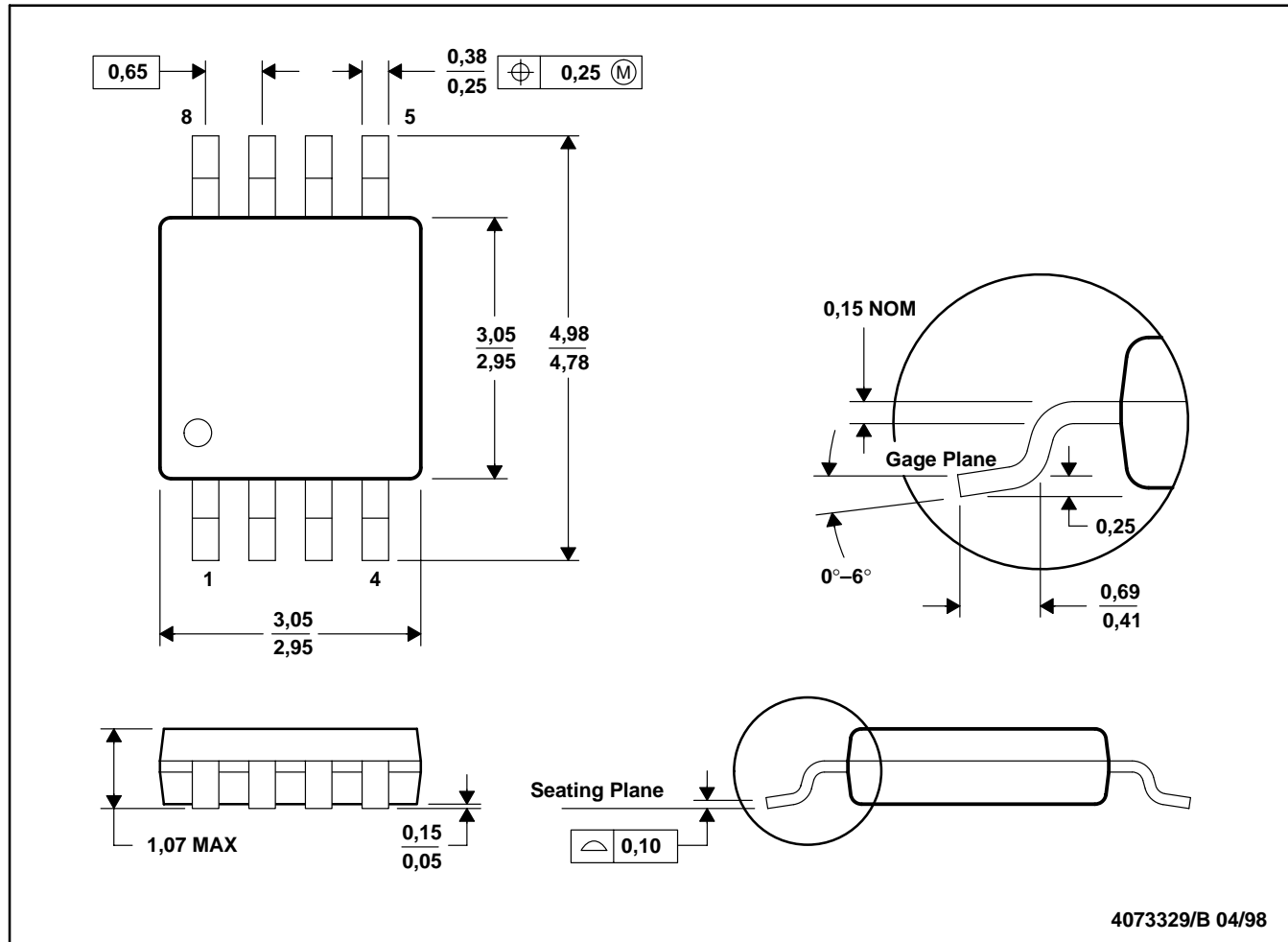
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**MECHANICAL DATA**

**DGK (R-PDSO-G8)**

**PLASTIC SMALL-OUTLINE PACKAGE**



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-187

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