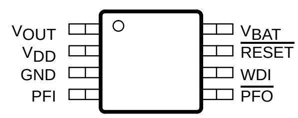
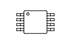
- **Supply Current of 40 μA (Max)**
- **Battery Supply Current of 100 nA (Max)**
- **Precision 5-V Supply Voltage Monitor, Other Voltage Options on Request**
- **Backup-Battery Voltage Can Exceed V_{DD}**
- **Watchdog Timer With 800-ms Time-Out**
- **Power-On Reset Generator With Fixed 100-ms Reset Delay Time**
- **Voltage Monitor for Power-Fail or Low-Battery Monitoring**
- **Battery Freshness Seal**
- **8-Pin MSOP Package**
- **Temperature Range . . . –40°C to 85°C**

typical applications

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice Mail Systems**
- **Portable Battery Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point of Sale Equipment**

MSOP (DGK) Package
(TOP VIEW)





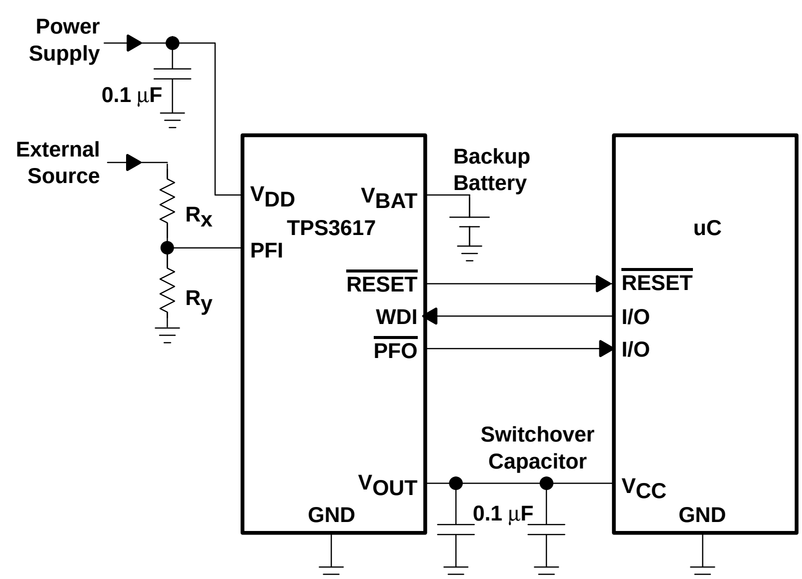
ACTUAL SIZE
3,05 mm x 4,98 mm

description

The TPS3617-50 supervisory circuit monitors and controls processor activity by providing backup-battery switchover for data retention of CMOS RAM.

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above the threshold voltage (V_{IT}).

typical operating circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

When the supply voltage drops below the threshold voltage (V_{IT}), the output becomes active (low) again.

The product spectrum is designed for supply voltages of 5.0 V. The TPS3617-50 is available in a 8-pin MSOP package and is characterized for operation over a temperature range of –40°C to 85°C.

PACKAGE INFORMATION

T_A	DEVICE NAME	MARKING
–40°C to 85°C	TPS3617–50DGKR†	ASD

† The DGKR passive indicates tape and reel of 2500 parts.

ordering information application specific versions

TPS361 7 – 50 DGK R

- **R** — Reel
- **DGK** — Package
- **50** — Nominal Supply Voltage
- **7** — Functionality
- **TPS361** — Family

DEVICE NAME	NOMINAL VOLTAGE‡, V_{NOM}
TPS3617–50 DGK	5 V

‡ For other threshold voltages, contact the local TI sales office for availability and lead-time.

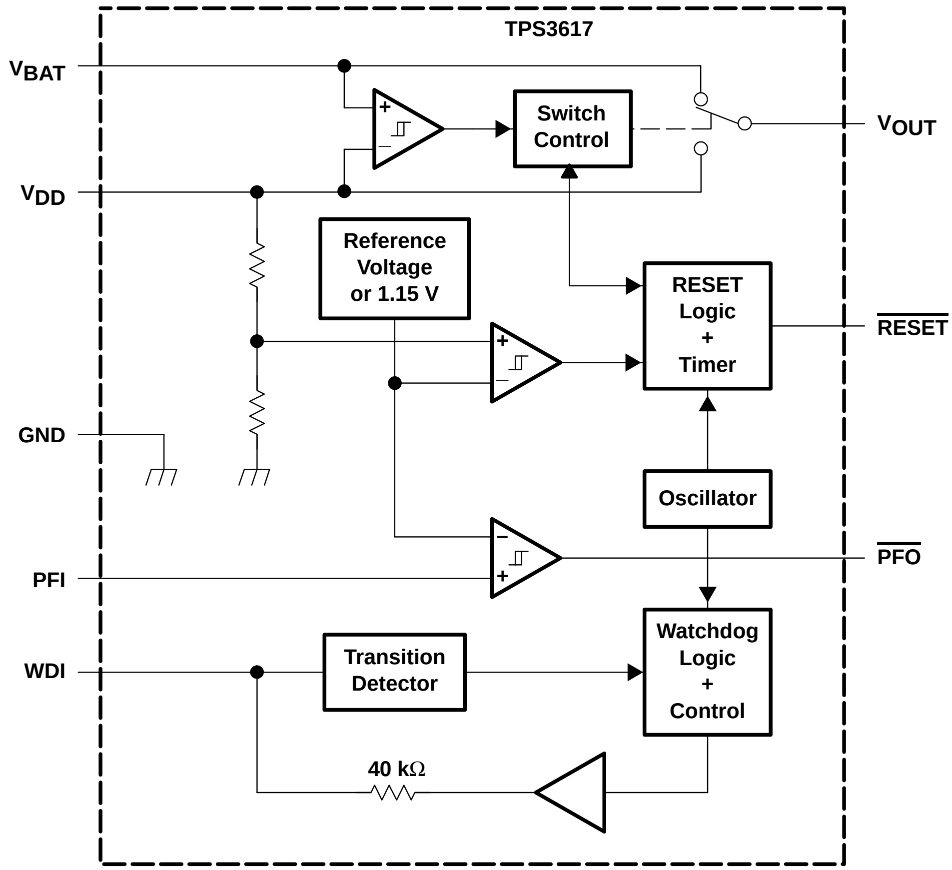
FUNCTION TABLE

$V_{DD} > V_{IT}$	$V_{DD} > V_{BAT}$	V_{OUT}	$\overline{RESET}$
0	0	V_{BAT}	0
0	1	V_{DD}	0
1	0	V_{DD}	1
1	1	V_{DD}	1

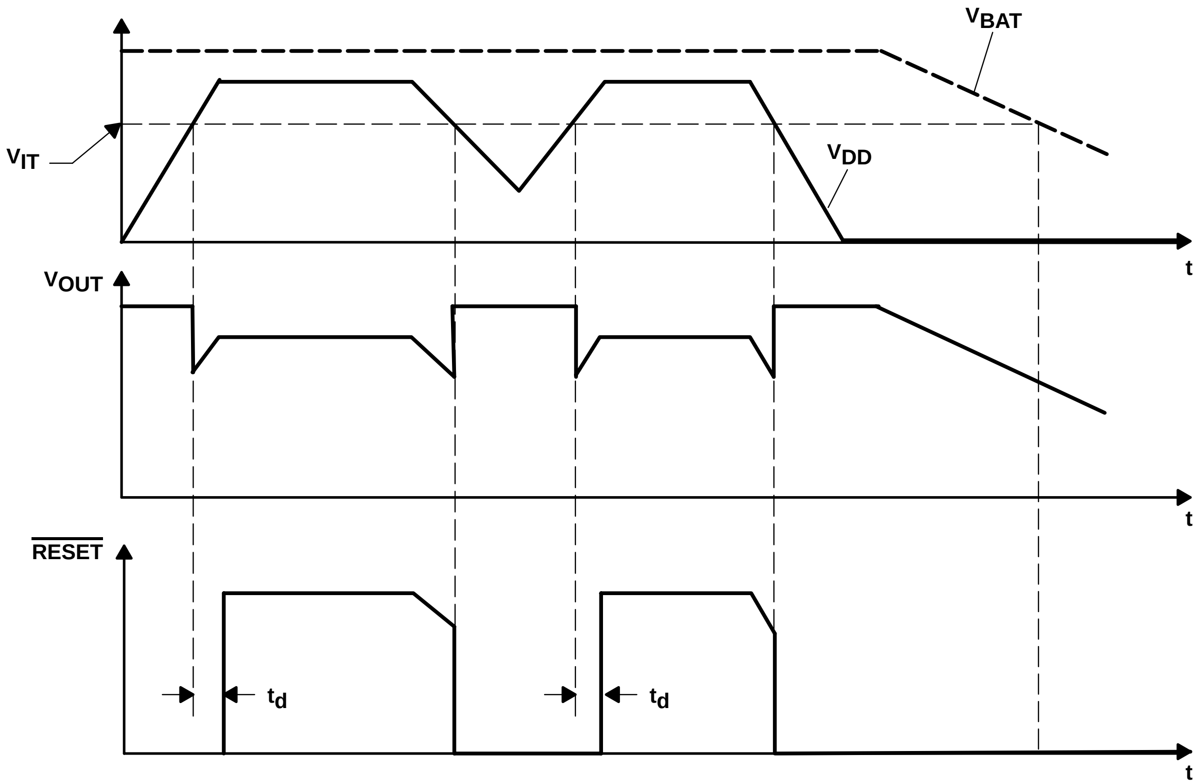
PFI > V_{PFI}	$\overline{PFO}$
0	0
1	1

CONDITION: $V_{DD} > V_{DD(min)}$

functional schematic



timing diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	3	I	Ground
PFI	4	I	Power-fail comparator input
$\overline{PFO}$	5	O	Power-fail comparator output
$\overline{RESET}$	7	O	Active-low reset output
V_{BAT}	8	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
V_{OUT}	1	O	Supply output
WDI	6	I	Watchdog input

detailed description

battery freshness seal

The battery freshness seal of the TPS3617 family disconnects the backup battery from the internal circuitry until it is needed. This ensures that the backup battery connected to V_{BAT} should be fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect V_{BAT} ($V_{BAT} > V_{BAT(min)}$
2. Ground $\overline{PFO}$
3. Connect PFI to V_{DD} (PFI = V_{DD})
4. Connect V_{DD} to power supply ($V_{DD} > V_{IT}$) and keep connected for 5 ms < t < 35 ms

The battery freshness seal mode is disabled by the positive-going edge of $\overline{RESET}$ when V_{DD} is applied.

power-fail comparator (PFI and $\overline{PFO}$)

An additional comparator monitors voltages other than the nominal supply voltage. The power-fail-input (PFI) can be compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold ($V_{(PFI)}$) of 1.15 V typical, the power-fail output ($\overline{PFO}$) goes low. If it goes above $V_{(PFI)}$ plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors it is possible to supervise any voltages above $V_{(PFI)}$. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of the sensed voltage. If the power-fail comparator is unused, connect PFI to ground and leave the $\overline{PFO}$ unconnected.

watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or DSP has to toggle the watchdog input within 0.8 s typically, to avoid a time out from occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected, the watchdog is disabled and should be retriggered internally.

saving current while using the watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead, WDI is externally driven high for the majority of the time-out period, a current of e.g. 5.0 V/40 kΩ ≈ 125 µA can flow into WDI.

detailed description (continued)

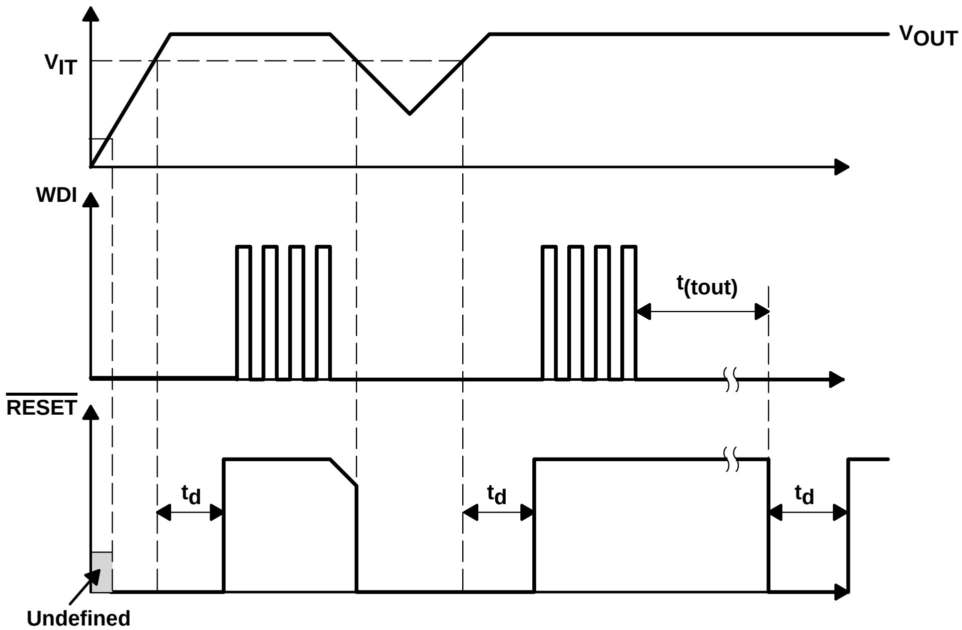


Figure 1. Watchdog Timing

backup-battery switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at V_{BAT}, the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD}, these supervisors should not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 15-Ω switch) when V_{DD} falls below V_{IT} and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or until V_{DD} rises above the reset threshold V_{IT}. V_{OUT} connects to V_{DD} through a 1-Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

$V_{DD} > V_{BAT}$	$V_{DD} > V_{IT}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

backup-battery switchover (continued)

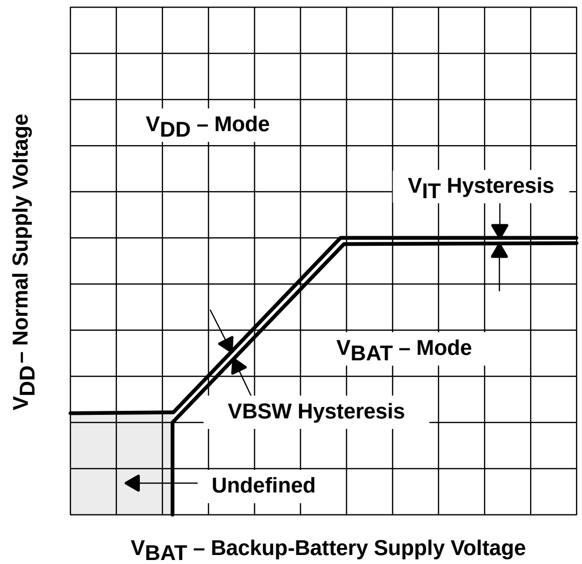


Figure 2. V_{DD} – V_{BAT} Switchover

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{DD} (see Note1) . . . 7 V
PFI pin (see Note 1) . . . –0.3 V to (V_{DD} + 0.3 V)
Continuous output current at V_{OUT}: I_O . . . 400 mA
All other pins, I_O . . . ±10 mA
Continuous total power dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t=1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGK	470 mW	3.76 mW/°C	301 mW	241 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.65	5.5	V
Battery supply voltage, V_{BAT}	1.5	5.5	V
Input voltage, V_I	0	V_{DD} + 0.3	V
High-level input voltage, V_{IH}	0.7 x V_{DD}		V
Low-level input voltage, V_{IL}		0.3 x V_{DD}	V
Continuous output current at V_{OUT}, I_O		300	mA
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$, WDI		100	ns/V
Slew rate at V_{DD} or V_{BAT}		1	V/µs
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$	V_{DD} = 1.8 V, I_{OH} = –400 µA	V_{DD} – 0.2 V			V
			V_{DD} = 3.3 V, I_{OH} = –2 mA V_{DD} = 5 V, I_{OH} = –3 mA	V_{DD} – 0.4 V			
		$\overline{PFO}$	V_{DD} = 1.8 V, I_{OH} = –20 µA	V_{DD} – 0.3 V			
			V_{DD} = 3.3 V, I_{OH} = –80 µA V_{DD} = 5 V, I_{OH} = –120 µA	V_{DD} – 0.4 V			
V_{OL}	Low-level output voltage	$\overline{RESET}$ $\overline{PFO}$	V_{DD} = 1.8 V, I_{OL} = 400 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA V_{DD} = 5 V, I_{OL} = 3 mA			0.4	
V_{res}	Power-up reset voltage (see Note 2)		V_{BAT} > 1.1 V, or V_{DD} > 1.1 V, I_{OL} = 20 µA			0.4	V
V_{OUT}	Normal mode		I_O = 8.5 mA, V_{DD} = 1.8 V, V_{BAT} = 0 V	V_{DD} – 50 mV			V
			I_O = 125 mA, V_{DD} = 3.3 V, V_{BAT} = 0 V	V_{DD} – 150 mV			
			I_O = 200 mA, V_{DD} = 5 V, V_{BAT} = 0 V	V_{DD} – 200 mV			
	Battery-backup mode		I_O = 0.5 mA, V_{BAT} = 1.5 V, V_{DD} = 0 V	V_{BAT} – 20 mV			
			I_O = 7.5 mA, V_{BAT} = 3.3 V, V_{DD} = 0 V	V_{BAT} – 113 mV			

NOTE 2: The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_{r,\ VDD} \geq 15$ µs/V.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	V_{DD} to V_{OUT} on-resistance		V_{DD} = 5 V		0.6	1	Ω
	V_{BAT} to V_{OUT} on-resistance		V_{BAT} = 3.3 V		8	15	
V_{IT}	Negative-going input threshold voltage (see Note 3)	TPS3617–50	T_A = –40°C to 85°C	4.46	4.55	4.64	V
V_{PFI}		PFI		1.13	1.15	1.17	
V_{hys}	Hysteresis	V_{IT}	1.65 V < V_{IT} < 2.5 V		20		mV
			2.5 V < V_{IT} < 3.5 V		40		
			3.5 V < V_{IT} < 5..5 V		60		
		PFI			12		
		V_{BSW} (see Note 4)	V_{DD} = 1.8 V		55		
I_{IH}	High-level input current	WDI (see Note 5)	WDI = V_{DD} = 5 V			150	µA
I_{IL}	Low-level input current		WDI = 0 V, V_{DD} = 5 V			–150	
I_I	Input current	PFI	V_I < V_{DD}	–25		25	nA
I_{OS}	Short-circuit current	$\overline{PFO}$	$\overline{PFO}$ = 0 V, V_{DD} = 1.8 V			–0.3	mA
			$\overline{PFO}$ = 0 V, V_{DD} = 3.3 V			–1.1	
			$\overline{PFO}$ = 0 V, V_{DD} = 5 V			–2.4	
I_{DD}	V_{DD} supply current		V_{OUT} = V_{DD}			40	µA
			V_{OUT} = V_{BAT}			40	
I_{BAT}	V_{BAT} supply current		V_{OUT} = V_{DD}	–0.1		0.1	µA
			V_{OUT} = V_{BAT}			0.5	
C_i	Input capacitance		V_I = 0 V to 5 V		5		pF

NOTES: 3. To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.
4. For V_{DD} < 1.6 V, V_{OUT} switches to V_{BAT} regardless of V_{BAT}.
5. For details on how to optimize current consumption when using WDI, refer to *detailed watchdog* description.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	V_{DD}	V_{IH} = V_{IT} + 0.2 V, V_{IL} = V_{IT} – 0.2 V	6			µs
		WDI	V_{DD} > V_{IT} + 0.2 V V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}	100			ns

switching characteristics at R_L = 1 MΩ, C_L= 50 pF, T_A = –40 °C to 85 °C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		V_{DD} ≥ V_{IT} + 0.2 V, See timing diagram	60	100	140	ms
$t_{(tout)}$	Watchdog time-out		V_{DD} > V_{IT} + 0.2 V, See timing diagram	0.48	0.8	1.12	s
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$	V_{IL} = V_{IT} – 0.2 V, V_{IH} = V_{IT} + 0.2 V		2	5	µs
		PFI to $\overline{PFO}$	V_{IL} = V_{PFI} – 0.2 V, V_{IH} = V_{PFI} + 0.2 V		3	5	
	Transition time	V_{DD} to V_{BAT}				3	

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance (V_{DD} to V_{OUT})	vs Output current	3
	Static drain-source on-state resistance (V_{BAT} to V_{OUT})	vs Output current	4
I_{DD}	Supply current	vs Supply voltage	5
V_{IT}	Input threshold voltage at $\overline{RESET}$	vs Free-air temperature	6
V_{OH}	High-level output voltage at $\overline{RESET}$	vs High-level output current	7, 8
	High-level output voltage at $\overline{PFO}$		9, 10
V_{OL}	Low-level output voltage at $\overline{RESET}$	vs Low-level output current	11, 12
	Minimum pulse duration at V_{DD}	vs Threshold voltage overdrive at V_{DD}	13
	Minimum pulse duration at PFI	vs Threshold voltage overdrive at PFI	14

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{DD} to V_{OUT}) vs OUTPUT CURRENT

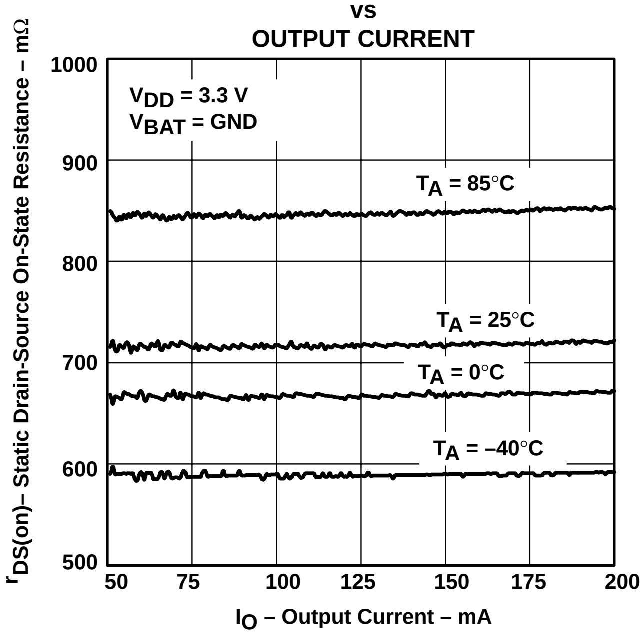


Figure 3

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{BAT} to V_{OUT}) vs OUTPUT CURRENT

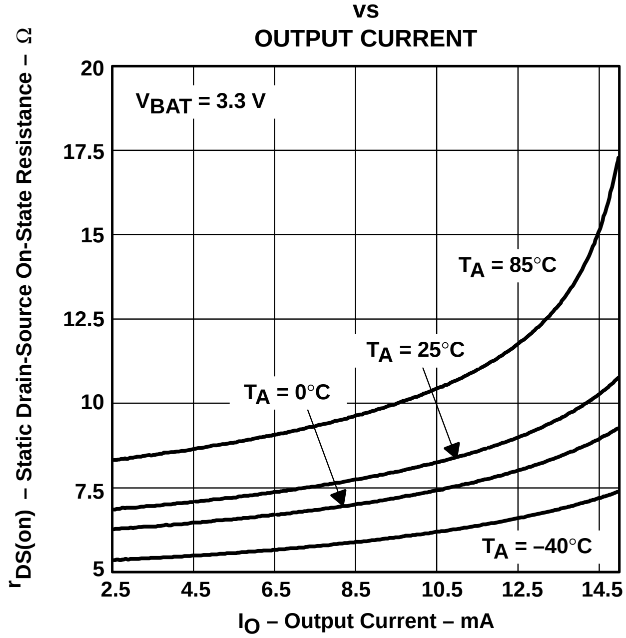


Figure 4

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

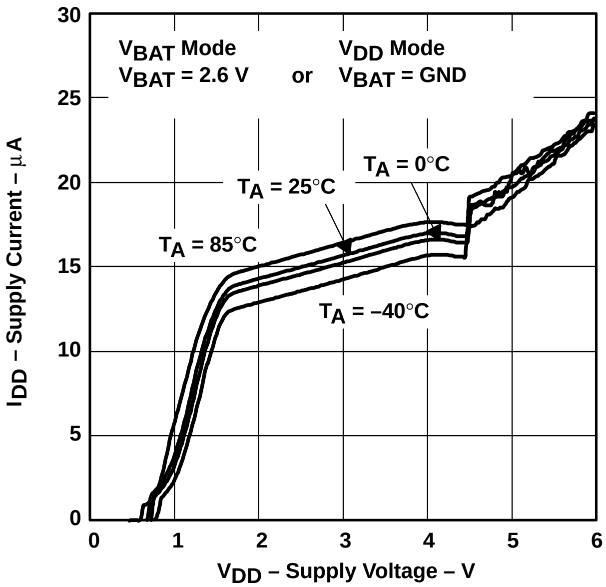


Figure 5

INPUT THRESHOLD VOLTAGE AT $\overline{\text{RESET}}$ vs FREE-AIR TEMPERATURE

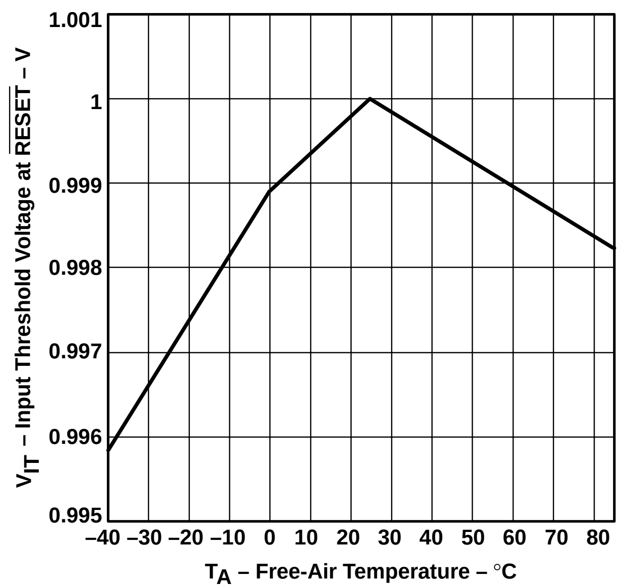


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$ vs HIGH-LEVEL OUTPUT CURRENT

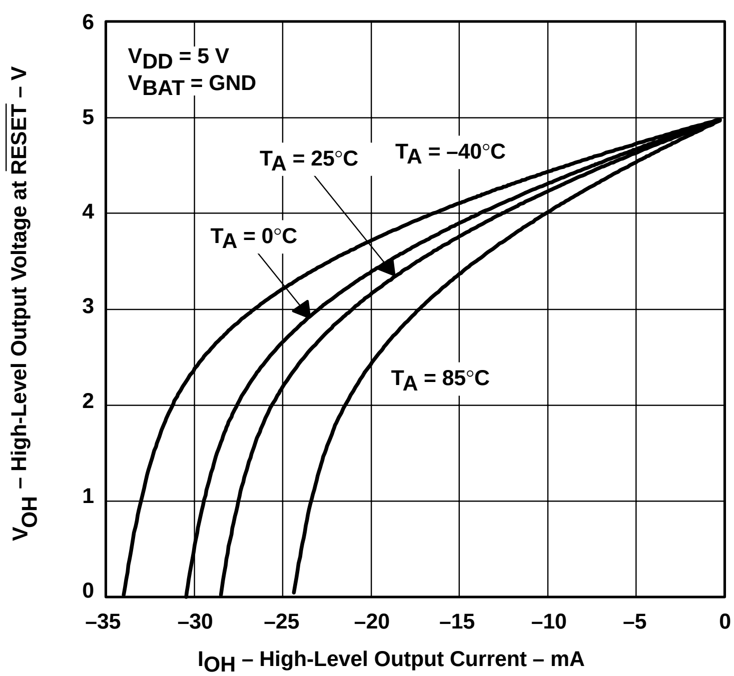


Figure 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{RESET}$
vs
HIGH-LEVEL OUTPUT CURRENT

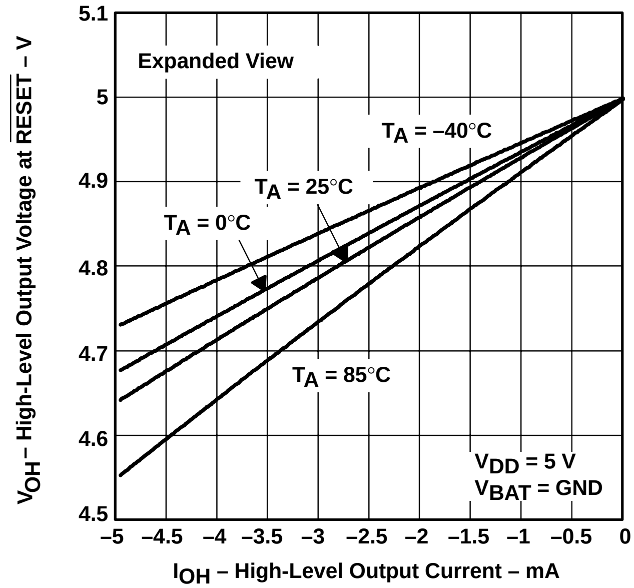


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{PFO}$
vs
HIGH-LEVEL OUTPUT CURRENT

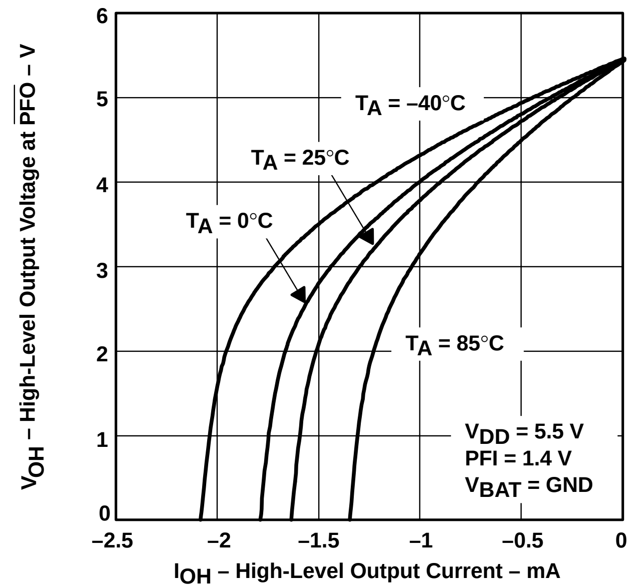


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{PFO}$
vs
HIGH-LEVEL OUTPUT CURRENT

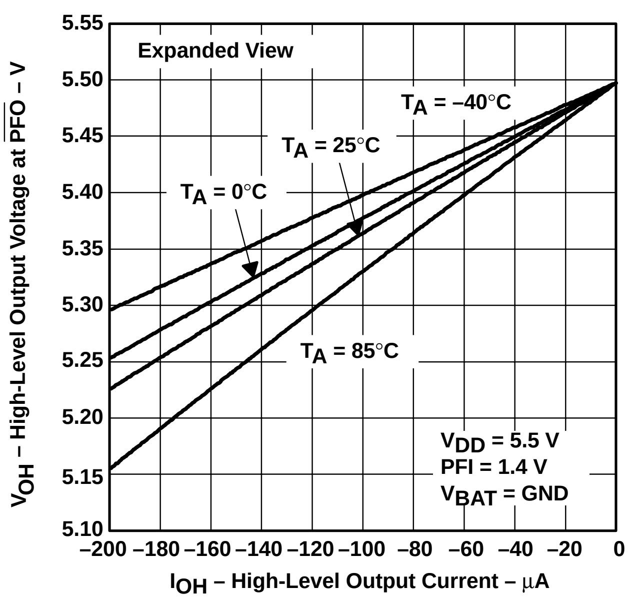


Figure 10

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{RESET}$
vs
LOW-LEVEL OUTPUT CURRENT

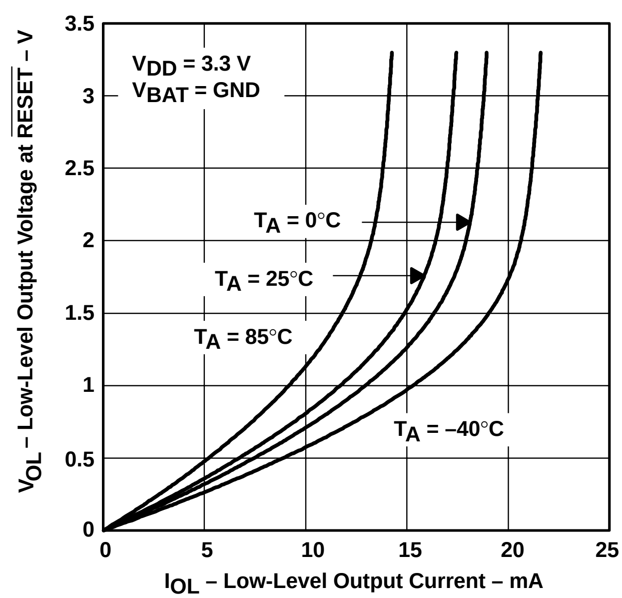


Figure 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{RESET}$
vs
LOW-LEVEL OUTPUT CURRENT

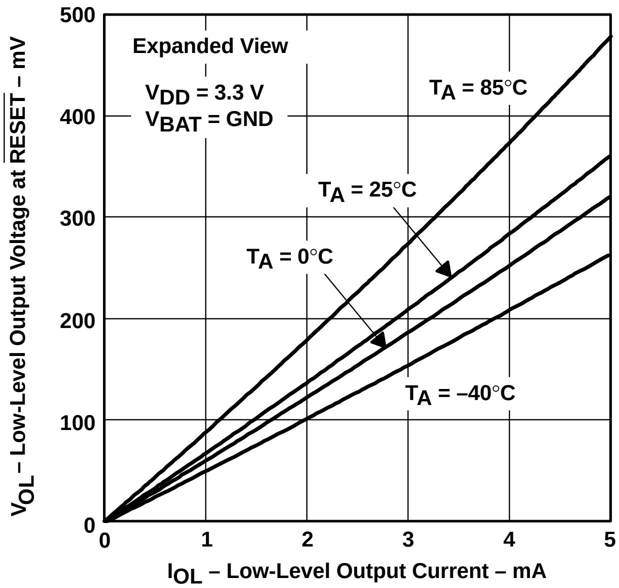


Figure 12

MINIMUM PULSE DURATION AT V_{DD}
vs
THRESHOLD VOLTAGE OVERDRIVE AT V_{DD}

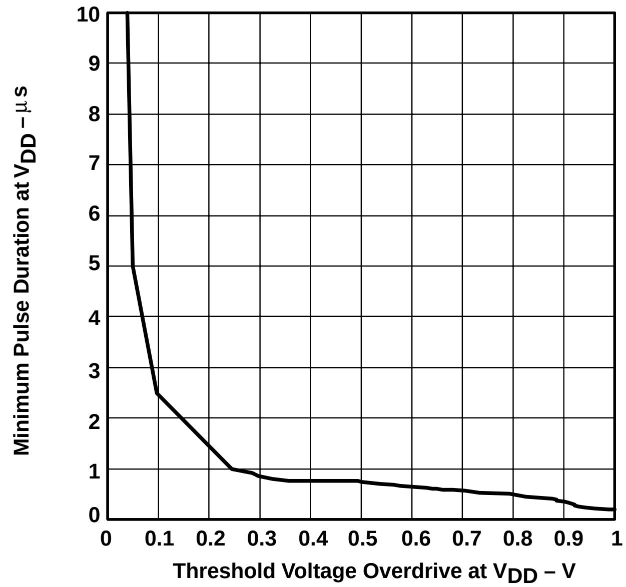


Figure 13

MINIMUM PULSE DURATION AT PFI
vs
THRESHOLD VOLTAGE OVERDRIVE AT PFI

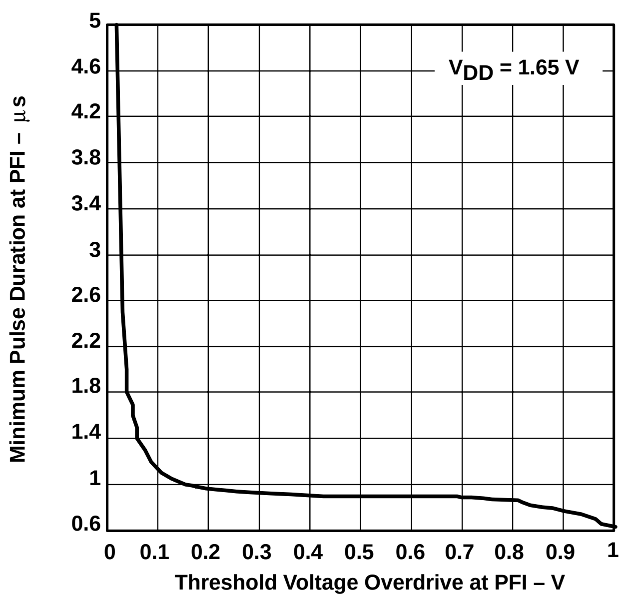
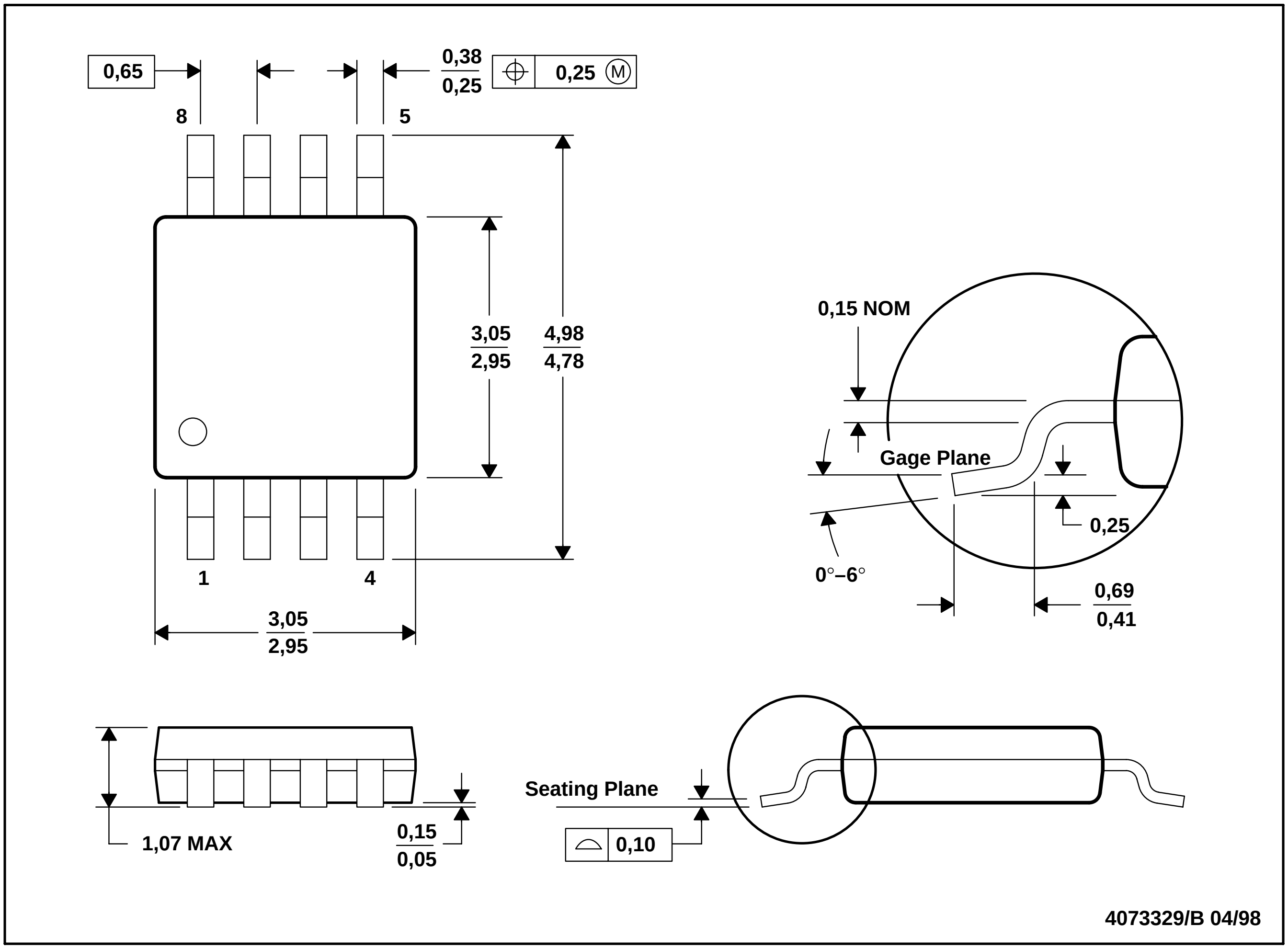


Figure 14

MECHANICAL DATA

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

IMPORTANT NOTICE

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