



VP11A



**P-Channel Enhancement-Mode
Vertical DMOS Power FETs**

T-39-19

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-60V	2Ω	-5A	VP1106N1	VP1106N2	VP1106N5	VP1106ND
-100V	2Ω	-5A	VP1110N1	VP1110N2	VP1110N5	VP1110ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

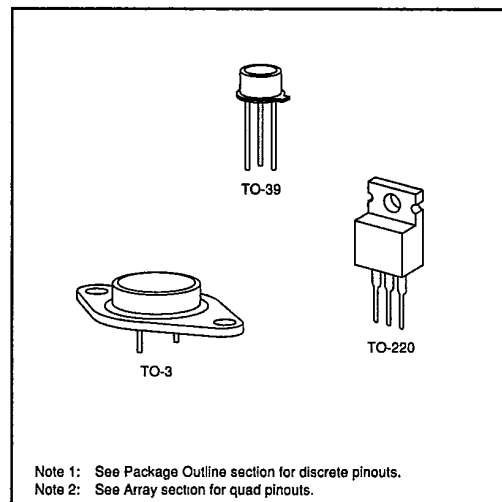
Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

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Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JA} $^\circ\text{C/W}$	θ_{JC} $^\circ\text{C/W}$	I_{DR}	I_{DRM}
TO-3	-6.0A	-15A	75W	50	1.66	-6A	-15A
TO-39	-1.5A	-7A	6W	125	20.8	-1.5A	-7A
TO-220	-4.0A	-12A	45W	70	2.78	-4A	-12A

* I_D (continuous) is limited by max rated T_J .

Electrical Characteristics (@ 25°C unless otherwise specified)

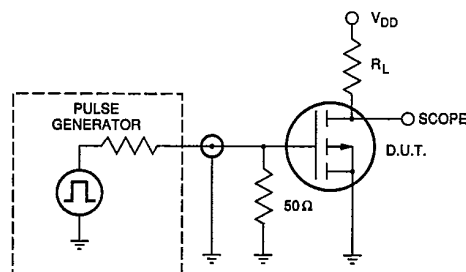
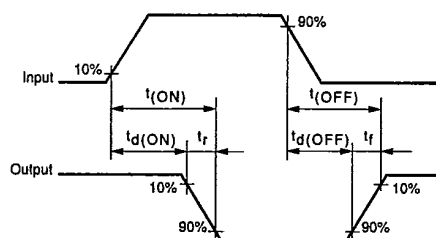
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1110 VP1106	-100 -60		V	$I_D = -5\text{mA}$, $V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -5\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-4.0		mV/ $^\circ\text{C}$	$I_D = -5\text{mA}$, $V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			-50	μA	$V_{GS} = 0$, $V_{DS} = \text{Max Rating}$
				-5	mA	$V_{GS} = 0$, $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-1.0			A	$V_{GS} = -5\text{V}$, $V_{DS} = -25\text{V}$
		-5.0				$V_{GS} = -10\text{V}$, $V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		2	5	Ω	$V_{GS} = -5\text{V}$, $I_D = -0.5\text{A}$
			1.5	2		$V_{GS} = -10\text{V}$, $I_D = -2.0\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.7	1.0	%/ $^\circ\text{C}$	$I_D = -1.0\text{A}$, $V_{GS} = -10\text{V}$
G_{FS}	Forward Transconductance	0.9	1.3		S	$V_{DS} = -25\text{V}$, $I_D = -2.0\text{A}$
C_{ISS}	Input Capacitance		300	350	pF	$V_{GS} = 0$, $V_{DS} = -20\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		100	150		
C_{RSS}	Reverse Transfer Capacitance		20	35		
$t_{d(ON)}$	Turn-ON Delay Time		35	40	ns	$V_{DD} = -18\text{V}$ $I_D = -2.0\text{A}$ $R_S = 50\Omega$
t_r	Rise Time		20	30		
$t_{d(OFF)}$	Turn-OFF Delay Time		40	50		
t_f	Fall Time		10	20		
V_{SD}	Diode Forward Voltage Drop	-1.4	-2.5		V	$I_{SD} = -1.0\text{A}$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time		400		ns	$I_{SD} = -1.0\text{A}$, $V_{GS} = 0$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

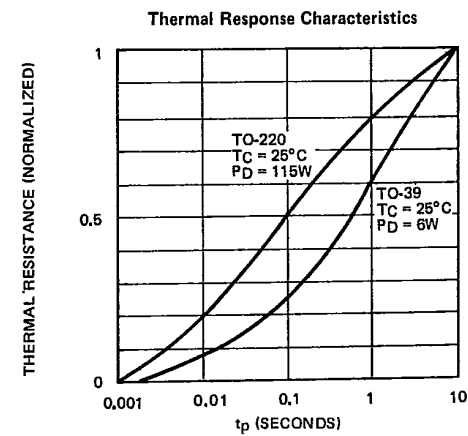
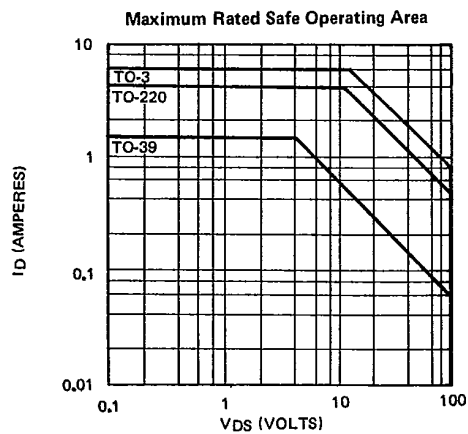
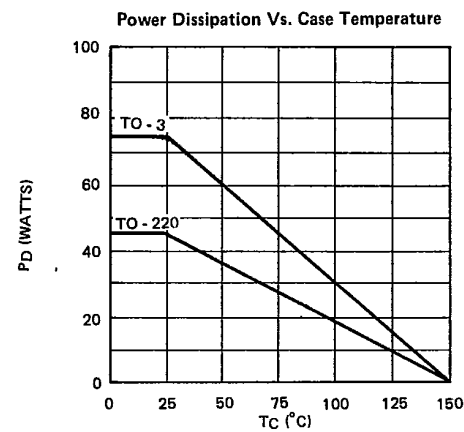
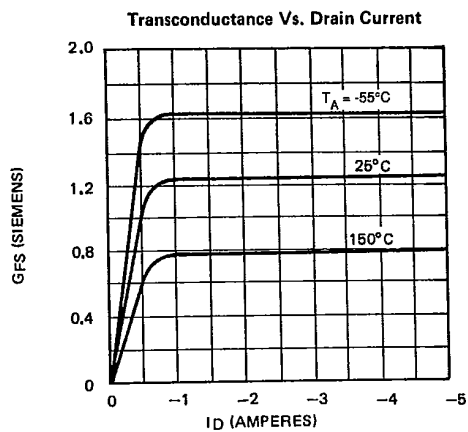
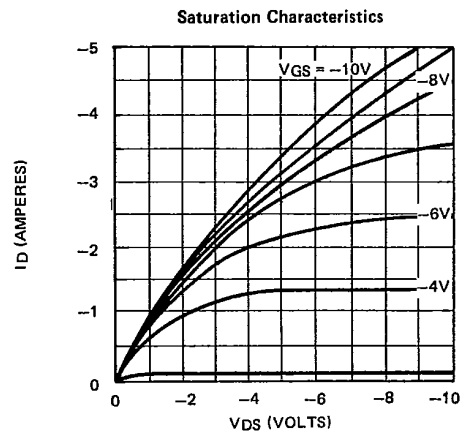
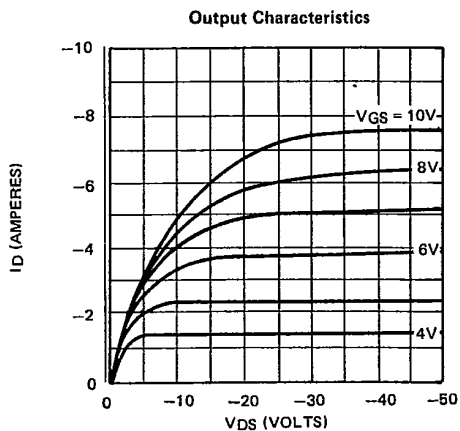
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Typical Performance Curves

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