

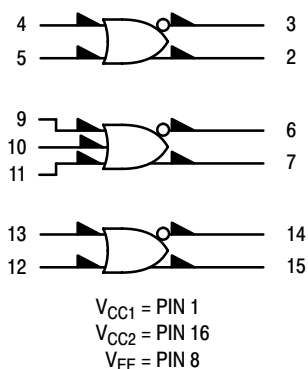
# MC10105

## Triple 2-3-2-Input OR/NOR Gate

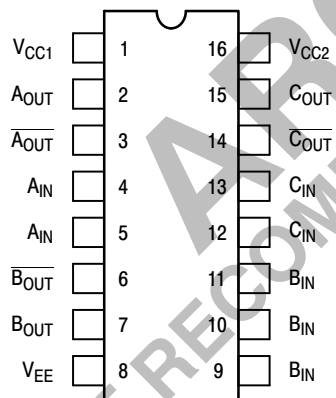
The MC10105 is a triple 2-3-2 input OR/NOR gate.

- $P_D = 30 \text{ mW typ/gate (No Load)}$
- $t_{pd} = 2.0 \text{ ns typ}$
- $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$

### LOGIC DIAGRAM



### DIP PIN ASSIGNMENT



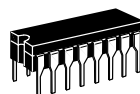
Pin assignment is for Dual-in-Line Package.  
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



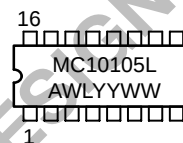
ON Semiconductor

<http://onsemi.com>

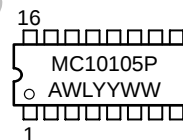
### MARKING DIAGRAMS



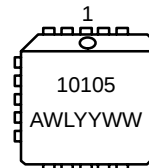
CDIP-16  
L SUFFIX  
CASE 620



PDIP-16  
P SUFFIX  
CASE 648



PLCC-20  
FN SUFFIX  
CASE 775



A = Assembly Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week

### ORDERING INFORMATION

| Device    | Package | Shipping        |
|-----------|---------|-----------------|
| MC10105L  | CDIP-16 | 25 Units / Rail |
| MC10105P  | PDIP-16 | 25 Units / Rail |
| MC10105FN | PLCC-20 | 46 Units / Rail |

# MC10105

## ELECTRICAL CHARACTERISTICS

| Characteristic                       | Symbol            | Pin Under Test | Test Limits |        |        |     |        |        |        | Unit |
|--------------------------------------|-------------------|----------------|-------------|--------|--------|-----|--------|--------|--------|------|
|                                      |                   |                | -30°C       |        | +25°C  |     |        | +85°C  |        |      |
|                                      |                   |                | Min         | Max    | Min    | Typ | Max    | Min    | Max    |      |
| Power Supply Drain Current           | I <sub>E</sub>    | 8              |             | 23     |        | 17  | 21     |        | 23     | mAdc |
| Input Current                        | I <sub>inH</sub>  | 4              |             | 425    |        |     | 265    |        | 265    | μAdc |
|                                      | I <sub>inL</sub>  | 4              | 0.5         |        | 0.5    |     |        | 0.3    |        | μAdc |
| Output Voltage      Logic 1          | V <sub>OH</sub>   | 3              | -1.060      | -0.890 | -0.960 |     | -0.810 | -0.890 | -0.700 | Vdc  |
|                                      |                   | 2              | -1.060      | -0.890 | -0.960 |     | -0.810 | -0.890 | -0.700 |      |
| Output Voltage      Logic 0          | V <sub>OL</sub>   | 3              | -1.890      | -1.675 | -1.850 |     | -1.650 | -1.825 | -1.615 | Vdc  |
|                                      |                   | 2              | -1.890      | -1.675 | -1.850 |     | -1.650 | -1.825 | -1.615 |      |
| Threshold Voltage      Logic 1       | V <sub>OHA</sub>  | 3              | -1.080      |        | -0.980 |     |        | -0.910 |        | Vdc  |
|                                      |                   | 2              | -1.080      |        | -0.980 |     |        | -0.910 |        |      |
| Threshold Voltage      Logic 0       | V <sub>OLA</sub>  | 3              |             | -1.655 |        |     | -1.630 |        | -1.595 | Vdc  |
|                                      |                   | 2              |             | -1.655 |        |     | -1.630 |        | -1.595 |      |
| Switching Times (50Ω Load)           |                   |                |             |        |        |     |        |        |        | ns   |
| Propagation Delay                    | t <sub>4+3-</sub> | 3              | 1.0         | 3.1    | 1.0    | 2.0 | 2.9    | 1.0    | 3.3    |      |
|                                      | t <sub>4-3+</sub> | 3              | 1.0         | 3.1    | 1.0    | 2.0 | 2.9    | 1.0    | 3.3    |      |
|                                      | t <sub>4+2+</sub> | 2              | 1.0         | 3.1    | 1.0    | 2.0 | 2.9    | 1.0    | 3.3    |      |
|                                      | t <sub>4-2-</sub> | 2              | 1.0         | 3.1    | 1.0    | 2.0 | 2.9    | 1.0    | 3.3    |      |
| Rise Time              (20 to 80%)   | t <sub>3+</sub>   | 3              | 1.1         | 3.6    | 1.1    | 2.0 | 3.3    | 1.1    | 3.7    |      |
|                                      | t <sub>2+</sub>   | 2              | 1.1         | 3.6    | 1.1    | 2.0 | 3.3    | 1.1    | 3.7    |      |
| Fall Time                (20 to 80%) | t <sub>3-</sub>   | 3              | 1.1         | 3.6    | 1.1    | 2.0 | 3.3    | 1.1    | 3.7    |      |
|                                      | t <sub>2-</sub>   | 2              | 1.1         | 3.6    | 1.1    | 2.0 | 3.3    | 1.1    | 3.7    |      |

## ELECTRICAL CHARACTERISTICS (continued)

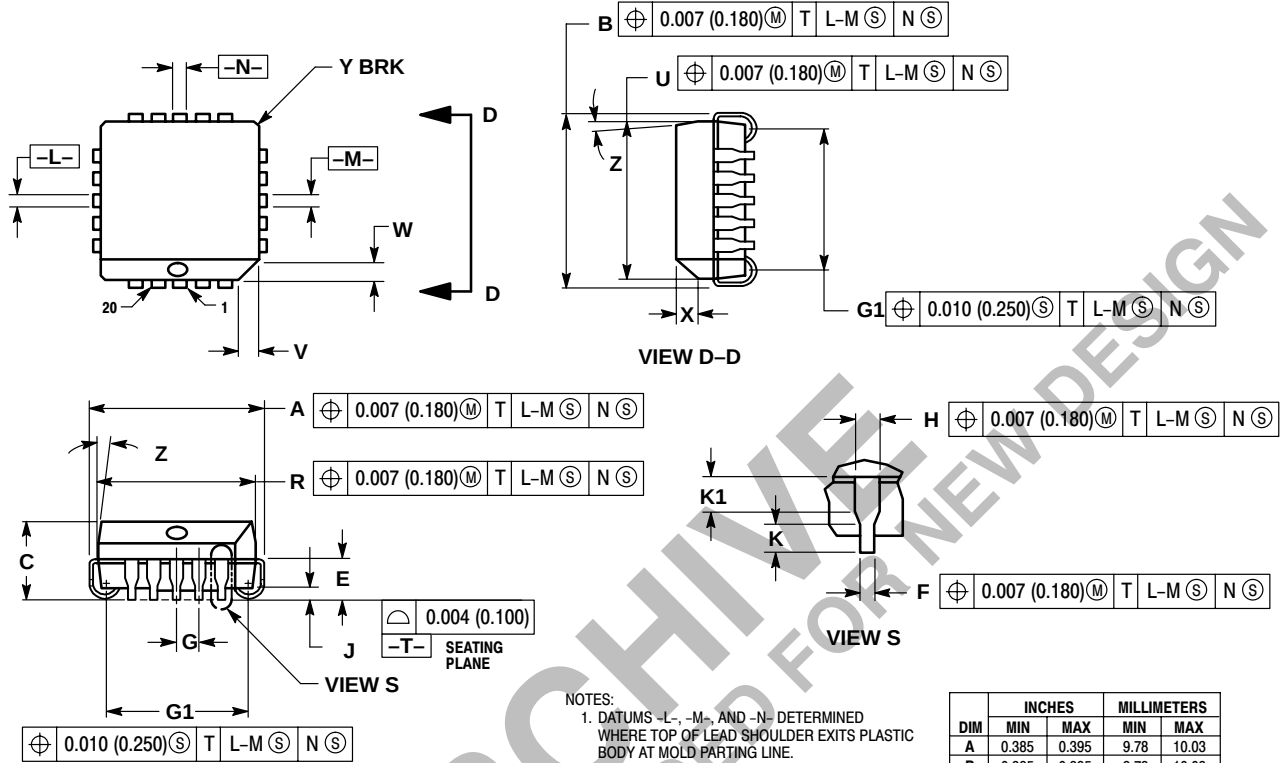
| @ Test Temperature         |                   |                | TEST VOLTAGE VALUES (Volts)               |                    |                     |                     |                 | (V <sub>CC</sub> )<br>Gnd |
|----------------------------|-------------------|----------------|-------------------------------------------|--------------------|---------------------|---------------------|-----------------|---------------------------|
|                            |                   |                | V <sub>IHmax</sub>                        | V <sub>ILmin</sub> | V <sub>IHAmin</sub> | V <sub>ILAmax</sub> | V <sub>EE</sub> |                           |
|                            |                   |                | –30°C                                     | –0.890             | –1.890              | –1.205              | –1.500          | –5.2                      |
|                            |                   |                | +25°C                                     | –0.810             | –1.850              | –1.105              | –1.475          | –5.2                      |
|                            |                   |                | +85°C                                     | –0.700             | –1.825              | –1.035              | –1.440          | –5.2                      |
| Characteristic             | Symbol            | Pin Under Test | TEST VOLTAGE APPLIED TO PINS LISTED BELOW |                    |                     |                     |                 | (V <sub>CC</sub> )<br>Gnd |
|                            |                   |                | V <sub>IHmax</sub>                        | V <sub>ILmin</sub> | V <sub>IHAmin</sub> | V <sub>ILAmax</sub> | V <sub>EE</sub> |                           |
| Power Supply Drain Current | I <sub>E</sub>    | 8              |                                           |                    |                     |                     | 8               | 1, 16                     |
| Input Current              | I <sub>inH</sub>  | 4              | 4                                         |                    |                     |                     | 8               | 1, 16                     |
|                            | I <sub>inL</sub>  | 4              |                                           | 4                  |                     |                     | 8               | 1, 16                     |
| Output Voltage Logic 1     | V <sub>OH</sub>   | 3              |                                           |                    |                     |                     | 8               | 1, 16                     |
|                            |                   | 2              | 4                                         |                    |                     |                     | 8               | 1, 16                     |
| Output Voltage Logic 0     | V <sub>OL</sub>   | 3              |                                           |                    |                     |                     | 8               | 1, 16                     |
|                            |                   | 2              | 4                                         |                    |                     |                     | 8               | 1, 16                     |
| Threshold Voltage Logic 1  | V <sub>OHA</sub>  | 3              |                                           |                    |                     | 4                   | 8               | 1, 16                     |
|                            |                   | 2              |                                           |                    | 4                   | 4                   | 8               | 1, 16                     |
| Threshold Voltage Logic 0  | V <sub>OLA</sub>  | 3              |                                           |                    | 4                   |                     | 8               | 1, 16                     |
|                            |                   | 2              |                                           |                    | 4                   | 4                   | 8               | 1, 16                     |
| Switching Times (50Ω Load) |                   |                |                                           |                    | Pulse In            | Pulse Out           | –3.2 V          | +2.0 V                    |
| Propagation Delay          | t <sub>4+3–</sub> | 3              |                                           |                    | 4                   | 3                   | 8               | 1, 16                     |
|                            | t <sub>4–3+</sub> | 3              |                                           |                    | 4                   | 3                   | 8               | 1, 16                     |
|                            | t <sub>4+2+</sub> | 2              |                                           |                    | 4                   | 2                   | 8               | 1, 16                     |
|                            | t <sub>4–2–</sub> | 2              |                                           |                    | 4                   | 2                   | 8               | 1, 16                     |
| Rise Time (20 to 80%)      | t <sub>3+</sub>   | 3              |                                           |                    | 4                   | 3                   | 8               | 1, 16                     |
|                            | t <sub>2+</sub>   | 2              |                                           |                    | 4                   | 2                   | 8               | 1, 16                     |
| Fall Time (20 to 80%)      | t <sub>3–</sub>   | 3              |                                           |                    | 4                   | 3                   | 8               | 1, 16                     |
|                            | t <sub>2–</sub>   | 2              |                                           |                    | 4                   | 2                   | 8               | 1, 16                     |

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

# MC10105

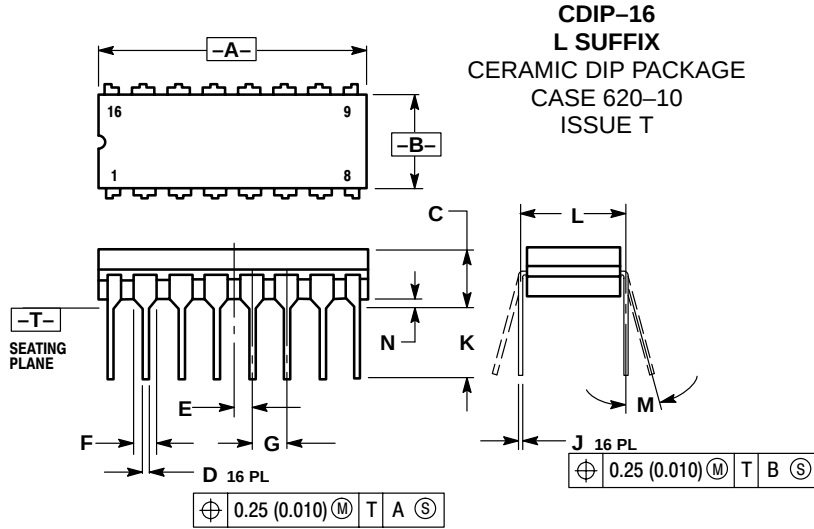
## PACKAGE DIMENSIONS

PLCC-20  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



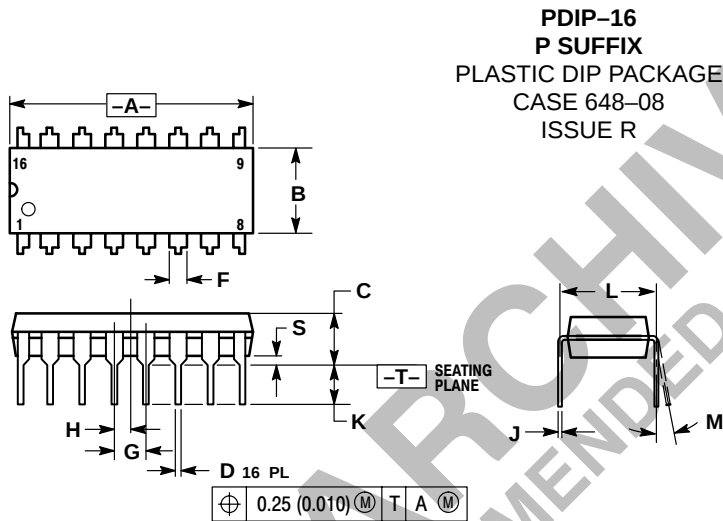
# MC10105

## PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.750     | 0.785 | 19.05       | 19.93 |
| B   | 0.240     | 0.295 | 6.10        | 7.49  |
| C   | ---       | 0.200 | ---         | 5.08  |
| D   | 0.015     | 0.020 | 0.39        | 0.50  |
| E   | 0.050 BSC |       | 1.27 BSC    |       |
| F   | 0.055     | 0.065 | 1.40        | 1.65  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.125     | 0.170 | 3.18        | 4.31  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 15°   | 0°          | 15°   |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

**Notes**

**ARCHIVE**  
DEVICE NOT RECOMMENDED FOR NEW DESIGN

**Notes**

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