

MC74HC74A

Dual D Flip-Flop with Set and Reset

High-Performance Silicon-Gate CMOS

The MC74HC74A is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and \bar{Q} outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

Features

- Pb-Free Packages are Available**
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 128 FETs or 32 Equivalent Gates

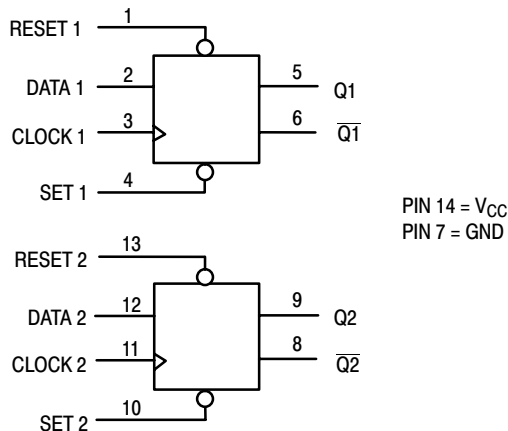


Figure 1. LOGIC DIAGRAM

FUNCTION TABLE

| Inputs | | | | Outputs | |
|--------|-------|------------|------|-----------|-----------|
| Set | Reset | Clock | Data | Q | \bar{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H* | H* |
| H | H | \nearrow | H | H | L |
| H | H | \searrow | L | L | H |
| H | H | L | X | No Change | No Change |
| H | H | H | X | No Change | No Change |
| H | H | \sim | X | No Change | No Change |

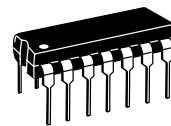
*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.



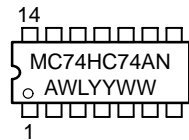
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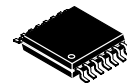
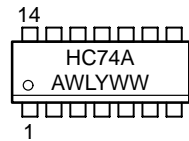
MARKING DIAGRAMS



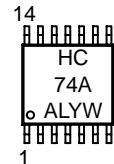
PDIP-14
N SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A

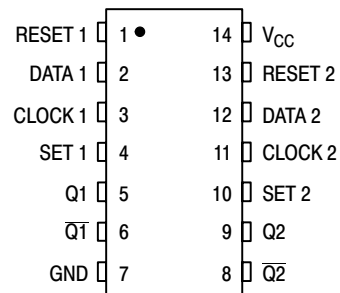


TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

**For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC74A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|---|-------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package† | 750 500 450 | mW |
| T_{stg} | Storage Temperature | - 65 to + 150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) | 260 300 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|--|--|--------------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | - 55 | + 125 | °C |
| t_r, t_f | Input Rise and Fall Time (Figures 1, 2, 3) | $V_{CC} = 2.0 \text{ V}$ $V_{CC} = 3.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ | 0 1000 600 500 400 | ns |

ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|----------------------|-------------------|
| MC74HC74AN | PDIP-14 | 2000 Units / Box |
| MC74HC74ANG | PDIP-14 (Pb-Free) | 2000 Units / Box |
| MC74HC74AD | SOIC-14 | 55 Units / Rail |
| MC74HC74ADR2 | SOIC-14 | 2500 Units / Reel |
| MC74HC74ADR2G | SOIC-14 (Pb-Free) | 2500 Units / Reel |
| MC74HC74ADT | TSSOP-14* | 96 Units / Rail |
| MC74HC74ADTR2 | TSSOP-14* | 2500 Units / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|--|----------------------|------------------|--------|---------|------|
| | | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 3.0 | 2.1 | 2.1 | 2.1 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 3.0 | 0.9 | 0.9 | 0.9 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA | 3.0 | 2.48 | 2.34 | 2.2 | |
| | | | 4.5 | 3.98 | 3.84 | 3.7 | |
| | | | 6.0 | 5.48 | 5.34 | 5.2 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA | 3.0 | 0.26 | 0.33 | 0.4 | |
| | | | 4.5 | 0.26 | 0.33 | 0.4 | |
| | | | 6.0 | 0.26 | 0.33 | 0.4 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 2.0 | 20 | 80 | μA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--|--|----------------------|------------------|--------|---------|------|
| | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| f _{max} | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4) | 2.0 | 6.0 | 4.8 | 4.0 | MHz |
| | | 3.0 | 15 | 10 | 8.0 | |
| | | 4.5 | 30 | 24 | 20 | |
| | | 6.0 | 35 | 28 | 24 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4) | 2.0 | 100 | 125 | 150 | ns |
| | | 3.0 | 75 | 90 | 120 | |
| | | 4.5 | 20 | 25 | 30 | |
| | | 6.0 | 17 | 21 | 26 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Set or Reset to Q or \bar{Q} (Figures 2 and 4) | 2.0 | 105 | 130 | 160 | ns |
| | | 3.0 | 80 | 95 | 130 | |
| | | 4.5 | 21 | 26 | 32 | |
| | | 6.0 | 18 | 22 | 27 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 30 | 40 | 55 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{in} | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Flip-Flop)* | Typical @ 25°C, V _{CC} = 5.0 V | |
|-----------------|--|---|--|
| | | 32 | |

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|---------------------------------|---|----------------------|------------------|--------|---------|------|
| | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{su} | Minimum Setup Time, Data to Clock (Figure 3) | 2.0 | 80 | 100 | 120 | ns |
| | | 3.0 | 35 | 45 | 55 | |
| | | 4.5 | 16 | 20 | 24 | |
| | | 6.0 | 14 | 17 | 20 | |
| t _h | Minimum Hold Time, Clock to Data (Figure 3) | 2.0 | 3.0 | 3.0 | 3.0 | ns |
| | | 3.0 | 3.0 | 3.0 | 3.0 | |
| | | 4.5 | 3.0 | 3.0 | 3.0 | |
| | | 6.0 | 3.0 | 3.0 | 3.0 | |
| t _{rec} | Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2) | 2.0 | 8.0 | 8.0 | 8.0 | ns |
| | | 3.0 | 8.0 | 8.0 | 8.0 | |
| | | 4.5 | 8.0 | 8.0 | 8.0 | |
| | | 6.0 | 8.0 | 8.0 | 8.0 | |
| t _w | Minimum Pulse Width, Clock (Figure 1) | 2.0 | 60 | 75 | 90 | ns |
| | | 3.0 | 25 | 30 | 40 | |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| t _w | Minimum Pulse Width, Set or Reset (Figure 2) | 2.0 | 60 | 75 | 90 | ns |
| | | 3.0 | 25 | 30 | 40 | |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| t _r , t _f | Maximum Input Rise and Fall Times (Figures 1, 2, 3) | 2.0 | 1000 | 1000 | 1000 | ns |
| | | 3.0 | 800 | 800 | 800 | |
| | | 4.5 | 500 | 500 | 500 | |
| | | 6.0 | 400 | 400 | 400 | |

MC74HC74A

SWITCHING WAVEFORMS

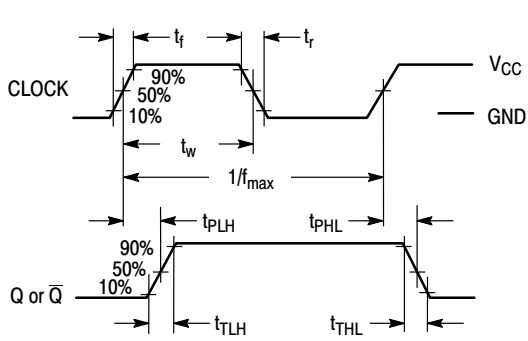


Figure 2.

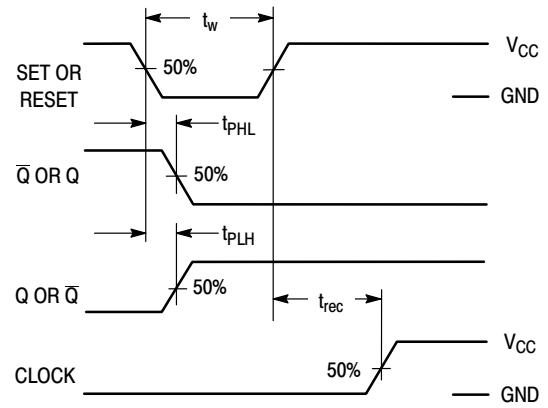


Figure 3.

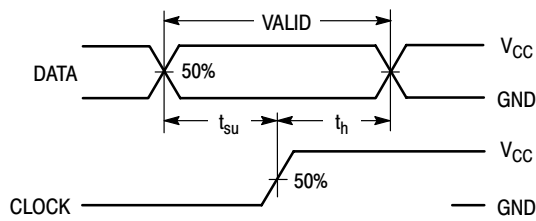
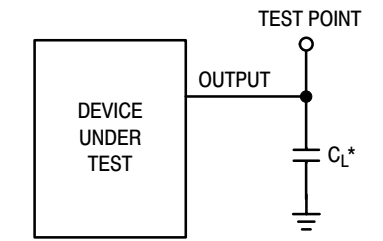


Figure 4.



*Includes all probe and jig capacitance

Figure 5.

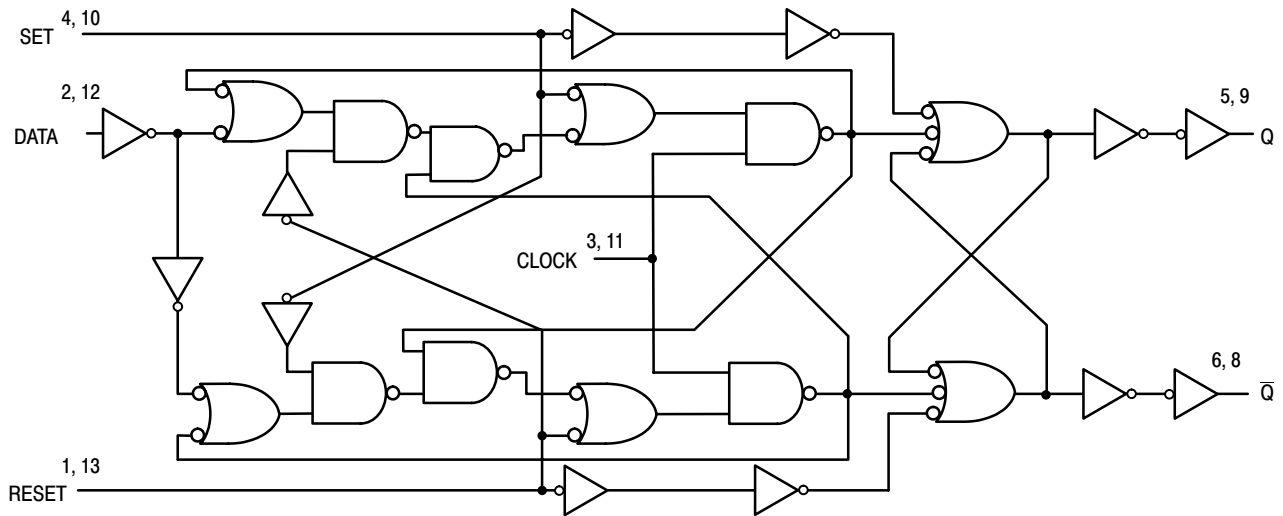
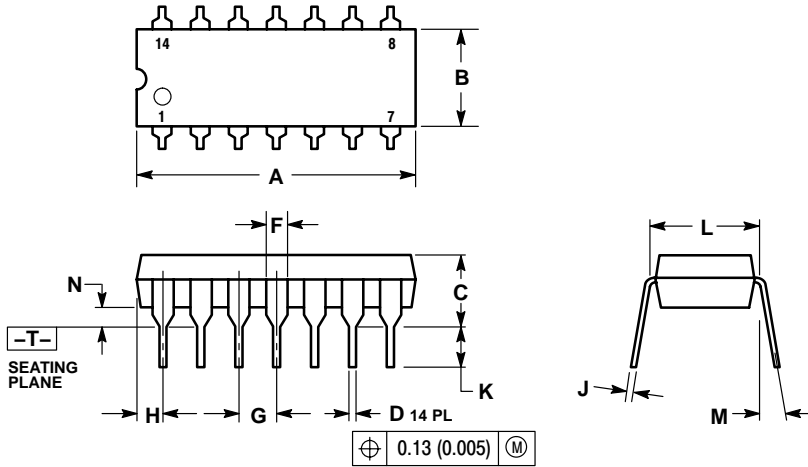


Figure 6. EXPANDED LOGIC DIAGRAM

MC74HC74A

PACKAGE DIMENSIONS

PDIP-14
N SUFFIX
CASE 646-06
ISSUE N

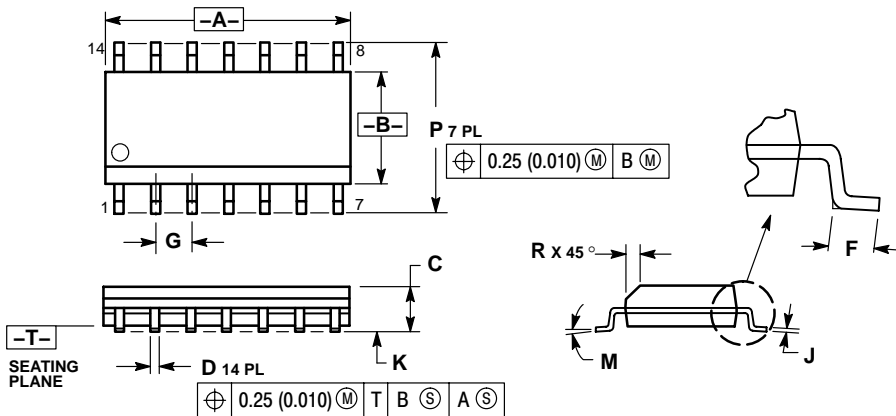


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 18.80 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | --- | 10° | --- | 10° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

SOIC-14
D SUFFIX
CASE 751A-03
ISSUE G



NOTES:

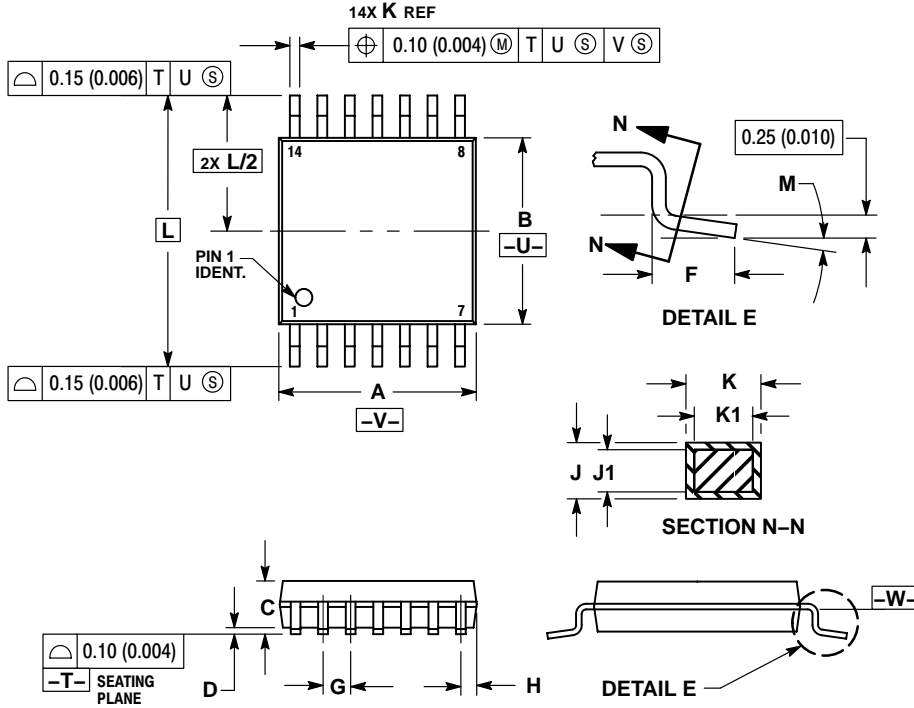
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

MC74HC74A

PACKAGE DIMENSIONS

TSSOP-14
DT SUFFIX
CASE 948G-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC74HC74A

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