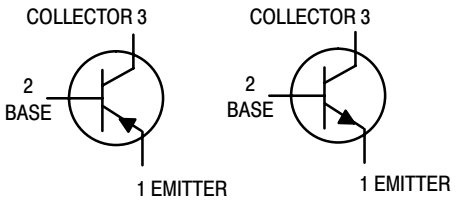
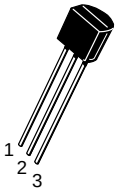
# Amplifier Transistors




**NPN**
**MPS6521***
**PNP**
**MPS6523**

**Voltage and current are negative for PNP transistors**

***ON Semiconductor Preferred Device**




**CASE 29–11, STYLE 1**
**TO–92 (TO–226AA)**

**MAXIMUM RATINGS**

| Rating | Symbol | NPN | PNP | Unit |
|---|---|---|---|---|
| Collector–Emitter Voltage<br>MPS6521<br>MPS6523 | $V_{CEO}$ | <br>25<br>— | <br>—<br>25 | Vdc |
| Collector–Base Voltage<br>MPS6521<br>MPS6523 | $V_{CBO}$ | <br>40<br>— | <br>—<br>25 | Vdc |
| Emitter–Base Voltage | $V_{EBO}$ | 4.0 | | Vdc |
| Collector Current — Continuous | $I_C$ | 100 | | mAdc |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 625<br>5.0 | | mW<br>mW/°C |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 1.5<br>12 | | Watts<br>mW/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient<br>(Printed Circuit Board Mounting) | $R_{\theta JA}$ | 200 | °C/W |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 83.3 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector–Emitter Breakdown Voltage<br>($I_C$ = 0.5 mAdc, $I_B$ = 0) | | $V_{(BR)CEO}$ | 25 | — | Vdc |
| Emitter–Base Breakdown Voltage<br>($I_E$ = 10 μAdc, $I_C$ = 0) | | $V_{(BR)EBO}$ | 4.0 | — | Vdc |
| Collector Cutoff Current<br>($V_{CB}$ = 30 Vdc, $I_E$ = 0)<br>($V_{CB}$ = 20 Vdc, $I_E$ = 0) | <br>MPS6521<br>MPS6523 | $I_{CBO}$ | <br>—<br>— | <br>0.05<br>0.05 | μAdc |

**Preferred** devices are ON Semiconductor recommended choices for future use and best overall value.

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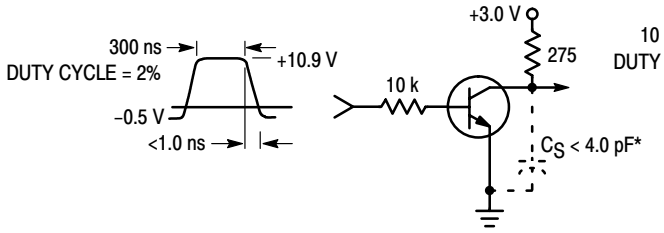
November, 2001 – Rev. 2
Publication Order Number:
MPS6521/D

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Continued)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain | | $h_{FE}$ | | | — |
| ($I_C$ = 100 μAdc, $V_{CE}$ = 10 Vdc) | MPS6521 | | 150 | — | |
| ($I_C$ = 2.0 mAdc, $V_{CE}$ = 10 Vdc) | MPS6521 | | 300 | 600 | |
| ($I_C$ = 100 μAdc, $V_{CE}$ = 10 Vdc) | MPS6523 | | 150 | — | |
| ($I_C$ = 2.0 mAdc, $V_{CE}$ = 10 Vdc) | MPS6523 | | 300 | 600 | |
| Collector–Emitter Saturation Voltage ($I_C$ = 50 mAdc, $I_B$ = 5.0 mAdc) | | $V_{CE(sat)}$ | — | 0.5 | Vdc |
| **SMALL–SIGNAL CHARACTERISTICS** | | | | | |
| Output Capacitance ($V_{CB}$ = 10 Vdc, $I_E$ = 0, f = 1.0 MHz) | | $C_{obo}$ | — | 3.5 | pF |
| Noise Figure ($I_C$ = 10 μAdc, $V_{CE}$ = 5.0 Vdc, $R_S$ = 10 k Ω, Power Bandwidth = 15.7 kHz, 3.0 dB points @ 10 Hz and 10 kHz) | | NF | — | 3.0 | dB |

## NPN
## MPS6521
## EQUIVALENT SWITCHING TIME TEST CIRCUITS




*Total shunt capacitance of test jig and connectors

**Figure 1. Turn–On Time**

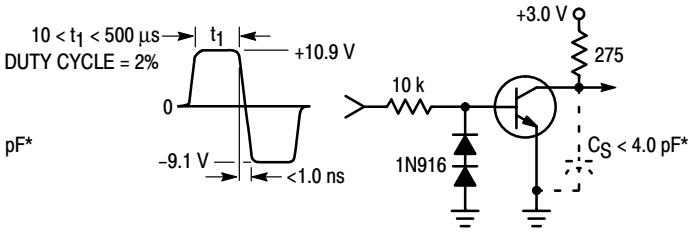



**Figure 2. Turn–Off Time**

## TYPICAL NOISE CHARACTERISTICS
($V_{CE}$ = 5.0 Vdc, $T_A$ = 25°C)

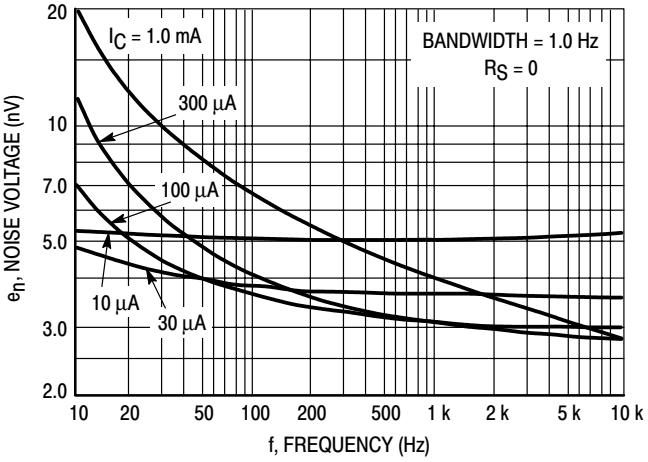



**Figure 3. Noise Voltage**

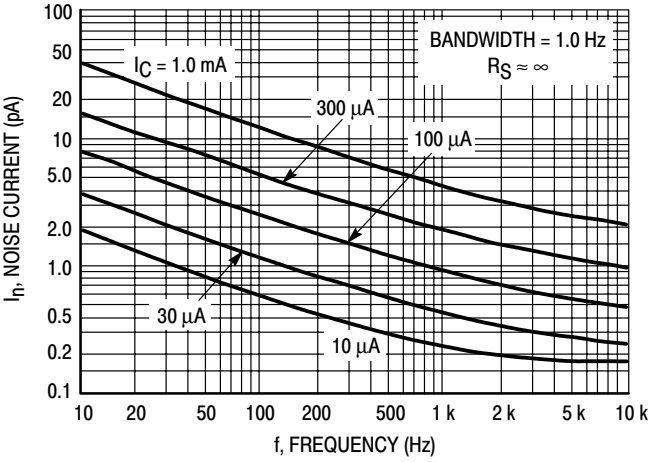



**Figure 4. Noise Current**

**NPN**
**MPS6521**
**NOISE FIGURE CONTOURS**
($V_{CE}$ = 5.0 Vdc, $T_A$ = 25°C)

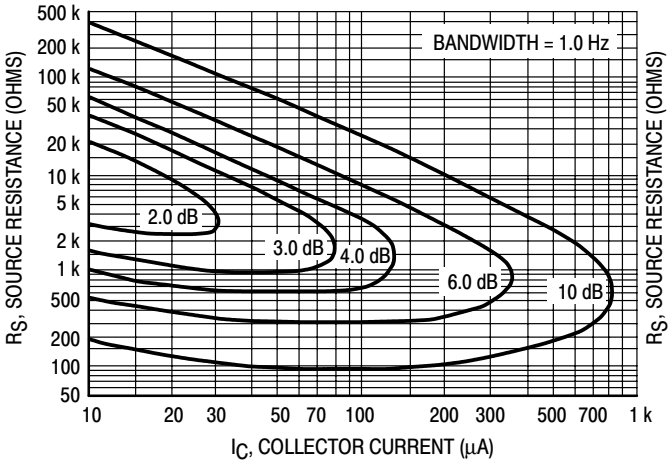



**Figure 5. Narrow Band, 100 Hz**

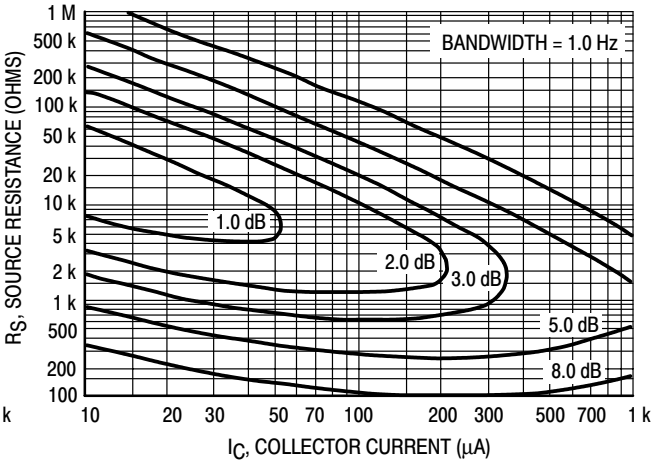



**Figure 6. Narrow Band, 1.0 kHz**

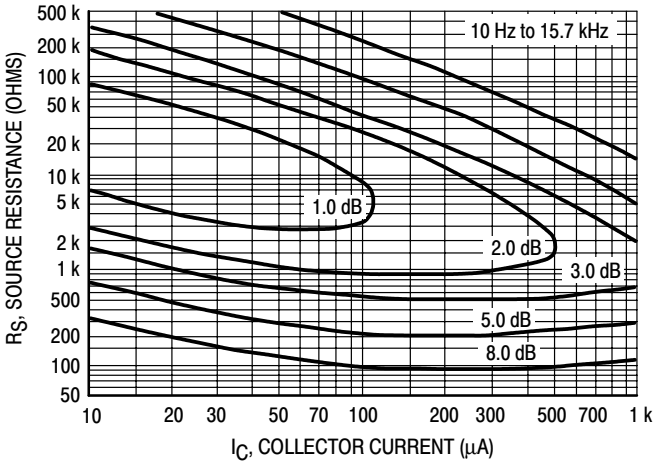



**Figure 7. Wideband**

Noise Figure is defined as:

$$NF = 20 \log_{10}\left(\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S}\right)^{1/2}$$

$e_n$ = Noise Voltage of the Transistor referred to the input. (Figure 3)
$I_n$ = Noise Current of the Transistor referred to the input. (Figure 4)
K = Boltzman's Constant ($1.38 \times 10^{-23}$ j/°K)
T = Temperature of the Source Resistance (°K)
$R_S$ = Source Resistance (Ohms)

## NPN
## MPS6521
## TYPICAL STATIC CHARACTERISTICS

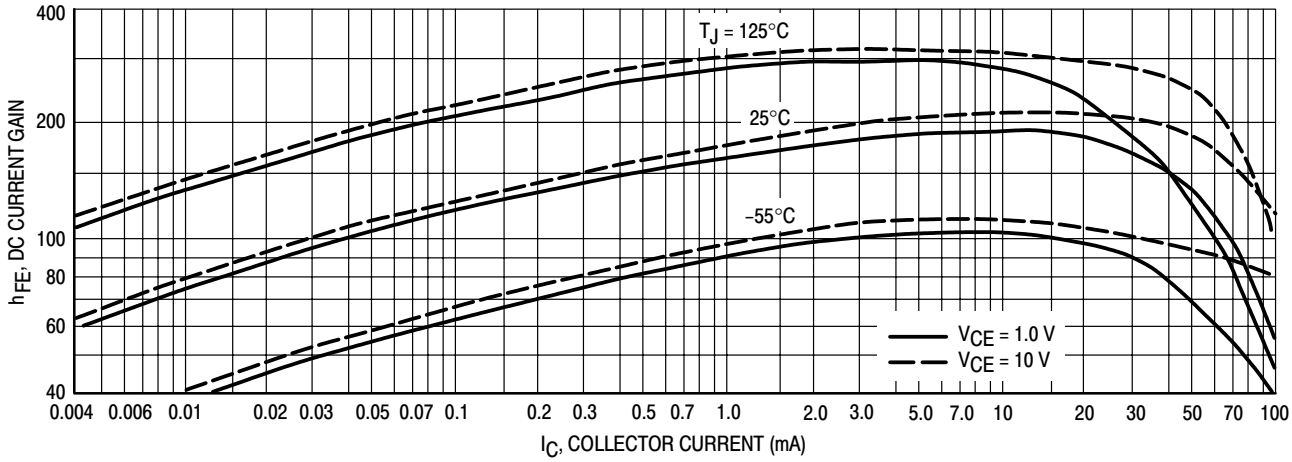



**Figure 8. DC Current Gain**

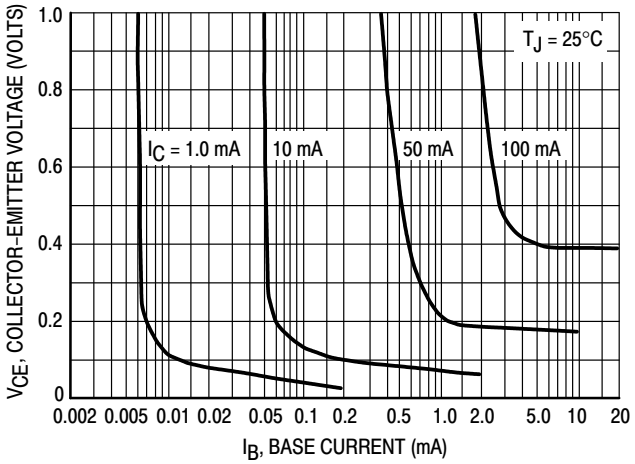



**Figure 9. Collector Saturation Region**

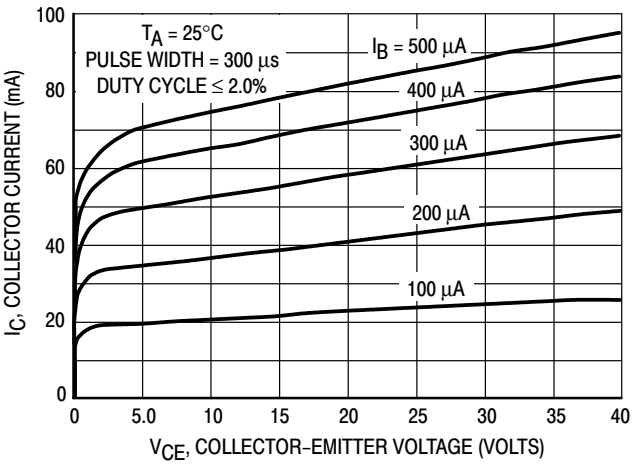



**Figure 10. Collector Characteristics**

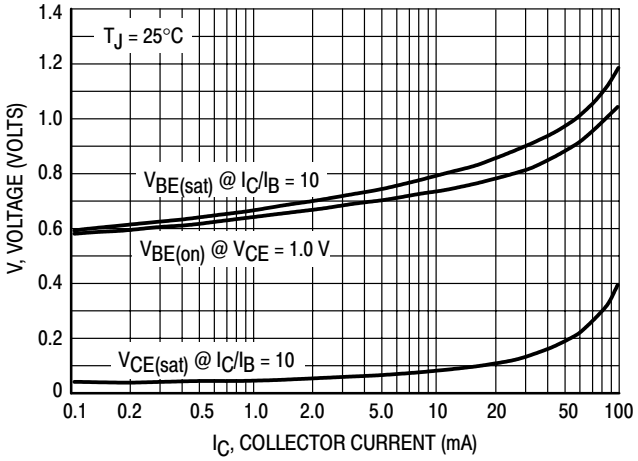



**Figure 11. “On” Voltages**

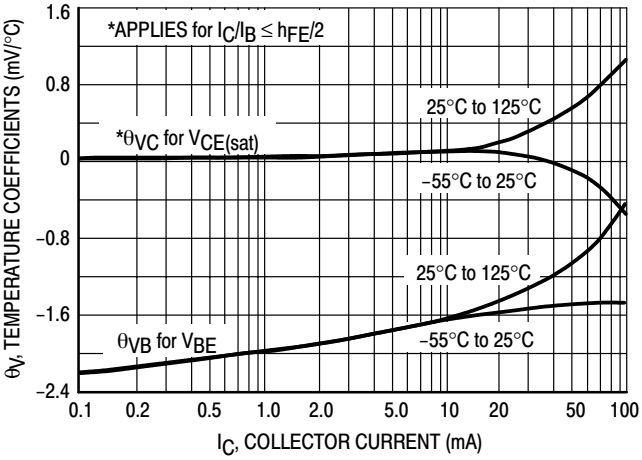



**Figure 12. Temperature Coefficients**

## NPN
## MPS6521
## TYPICAL DYNAMIC CHARACTERISTICS

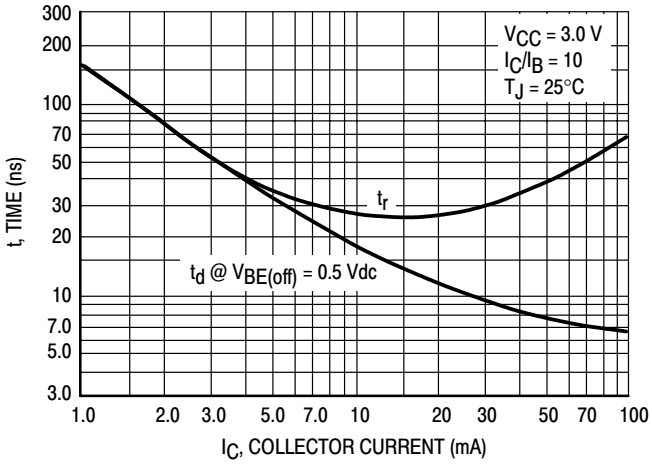



**Figure 13. Turn–On Time**

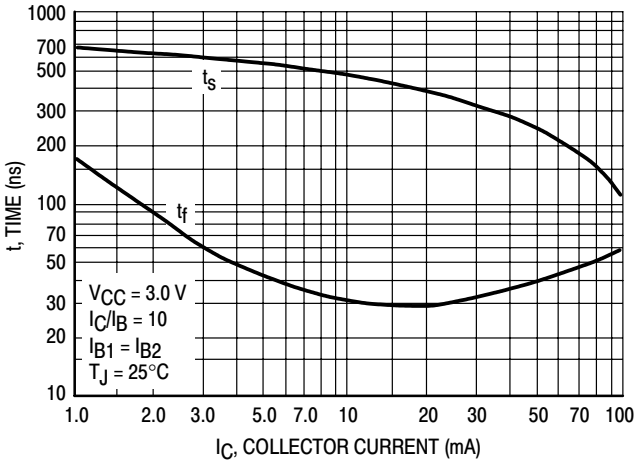



**Figure 14. Turn–Off Time**

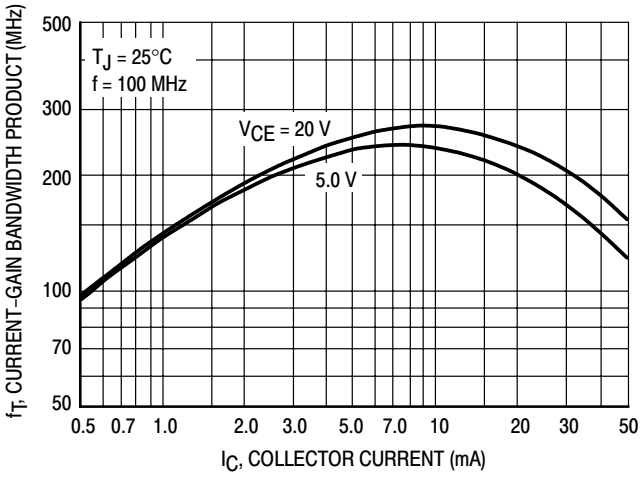



**Figure 15. Current–Gain — Bandwidth Product**

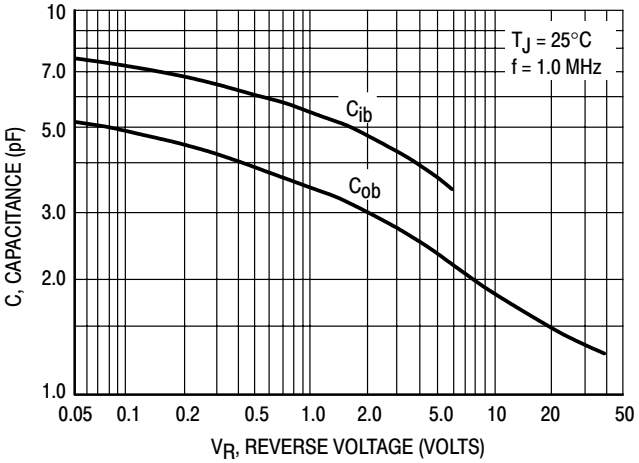



**Figure 16. Capacitance**

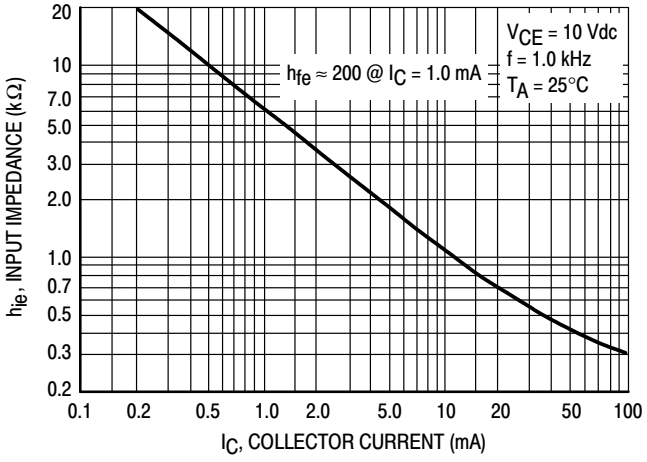



**Figure 17. Input Impedance**

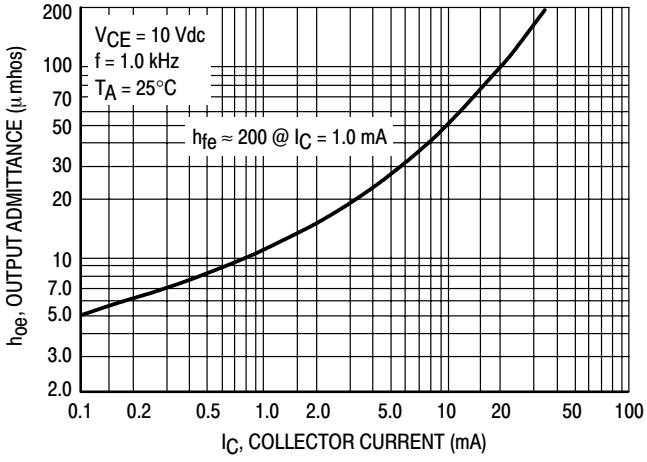



**Figure 18. Output Admittance**

**NPN**
**MPS6521**

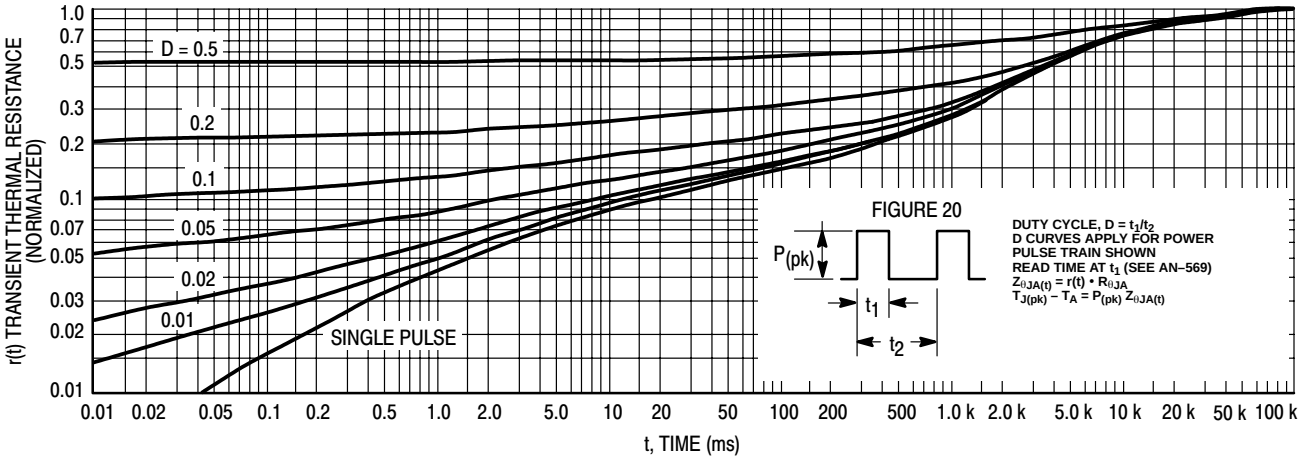



**Figure 19. Thermal Response**

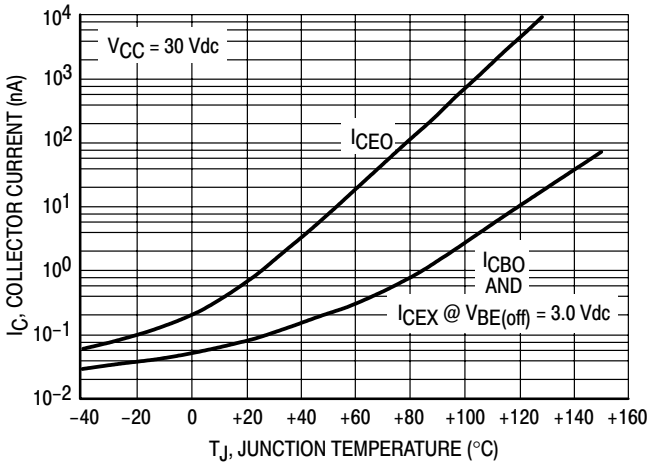



**Figure 21.**

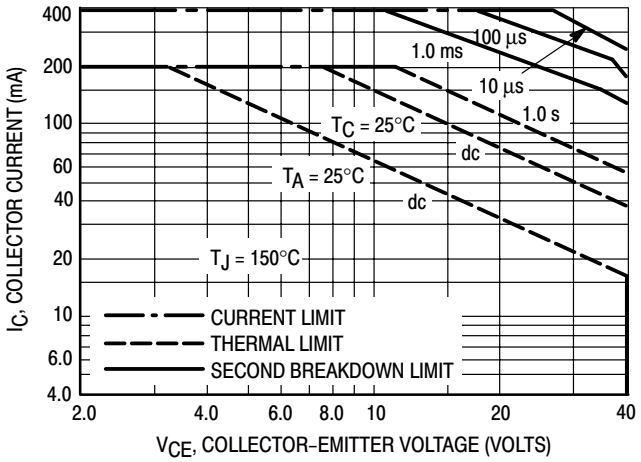



**Figure 22.**

**DESIGN NOTE: USE OF THERMAL RESPONSE DATA**

A train of periodical power pulses can be represented by the model as shown in Figure 20. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 19 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 19 by the steady state value $R_{\theta JA}$.

Example:

The MPS6521 is dissipating 2.0 watts peak under the following conditions:

$t_1$ = 1.0 ms, $t_2$ = 5.0 ms. (D = 0.2)

Using Figure 19 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore

$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88°C$.

For more information, see ON Semiconductor Application Note AN569/D, available from the Literature Distribution Center or on our website at **www.onsemi.com**.

The safe operating area curves indicate $I_C$–$V_{CE}$ limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 22 is based upon $T_{J(pk)}$ = 150°C; $T_C$ or $T_A$ is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 19. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

## PNP
## MPS6523
## TYPICAL NOISE CHARACTERISTICS

($V_{CE}$ = –5.0 Vdc, $T_A$ = 25°C)

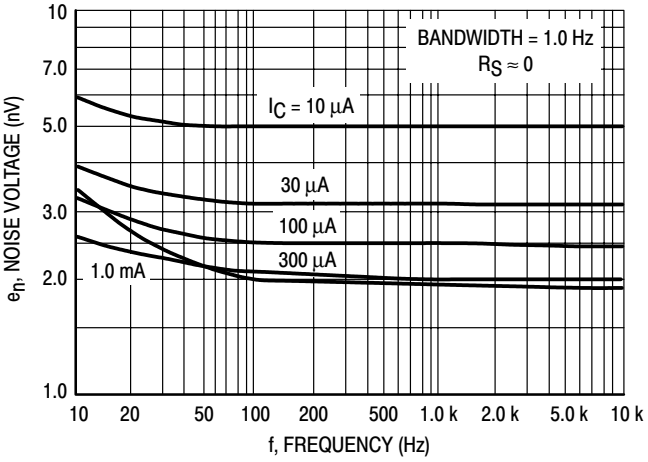



**Figure 23. Noise Voltage**

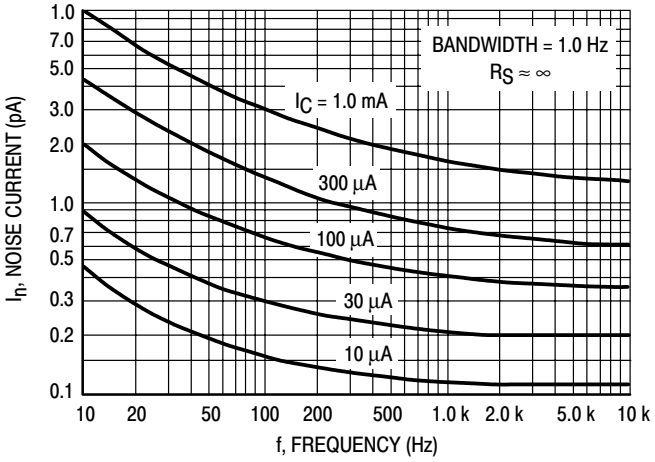



**Figure 24. Noise Current**

## NOISE FIGURE CONTOURS

($V_{CE}$ = –5.0 Vdc, $T_A$ = 25°C)

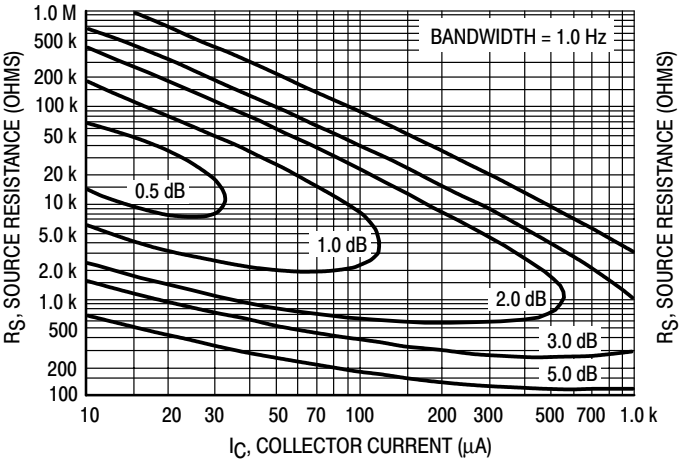



**Figure 25. Narrow Band, 100 Hz**

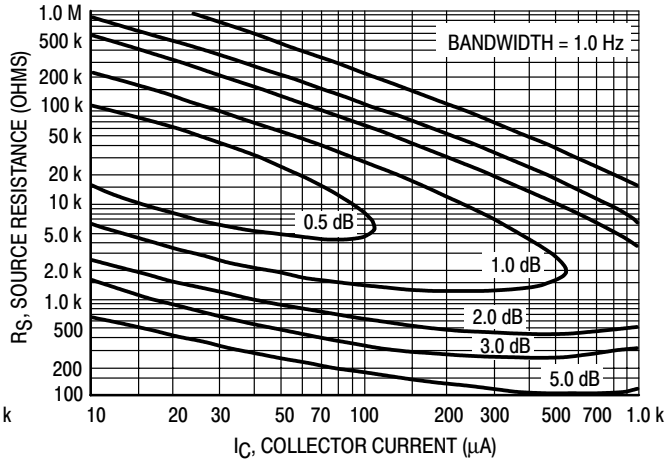



**Figure 26. Narrow Band, 1.0 kHz**

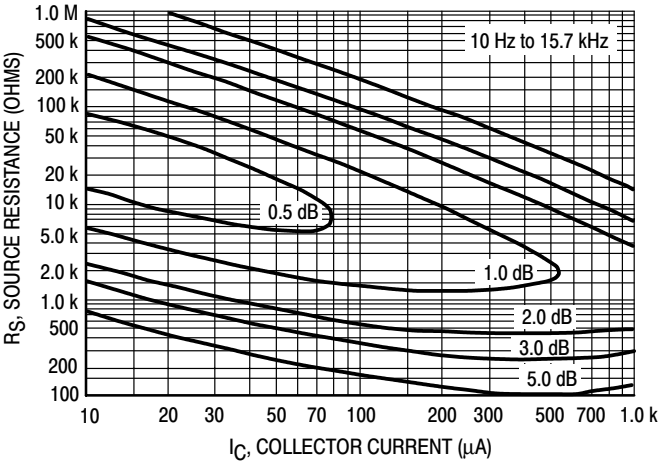



**Figure 27. Wideband**

Noise Figure is Defined as:

$$NF = 20 \log_{10}\left[\frac{e_n^2 + 4KTR_S + I_n{}^2R_S{}^2}{4KTR_S}\right]^{1/2}$$

$e_n$ = Noise Voltage of the Transistor referred to the input. (Figure 3)
$I_n$ = Noise Current of the Transistor referred to the input. (Figure 4)
K = Boltzman's Constant (1.38 x $10^{-23}$ j/°K)
T = Temperature of the Source Resistance (°K)
$R_S$ = Source Resistance (Ohms)

**PNP**
**MPS6523**
**TYPICAL STATIC CHARACTERISTICS**

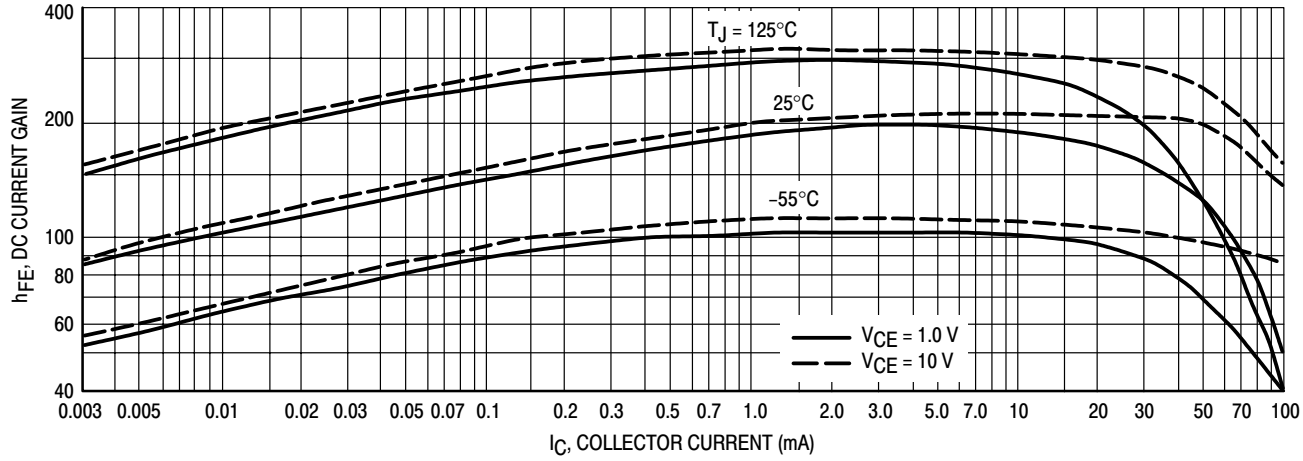



**Figure 28. DC Current Gain**

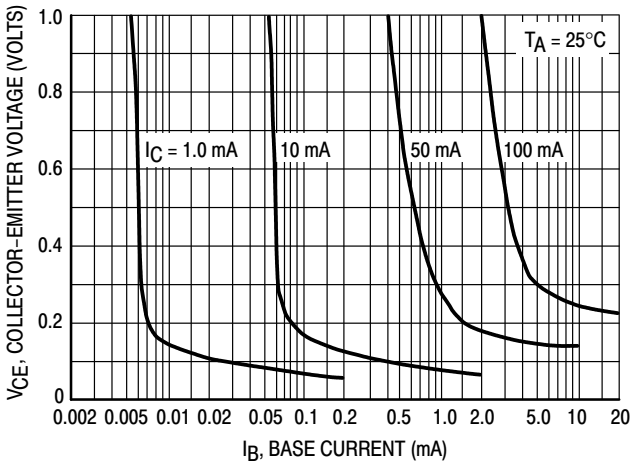



**Figure 29. Collector Saturation Region**

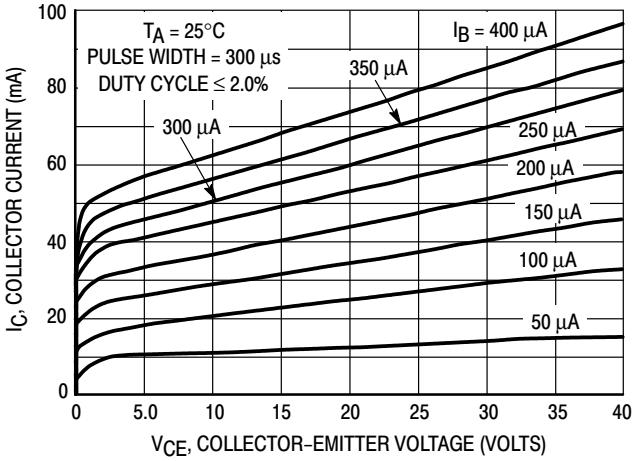



**Figure 30. Collector Characteristics**

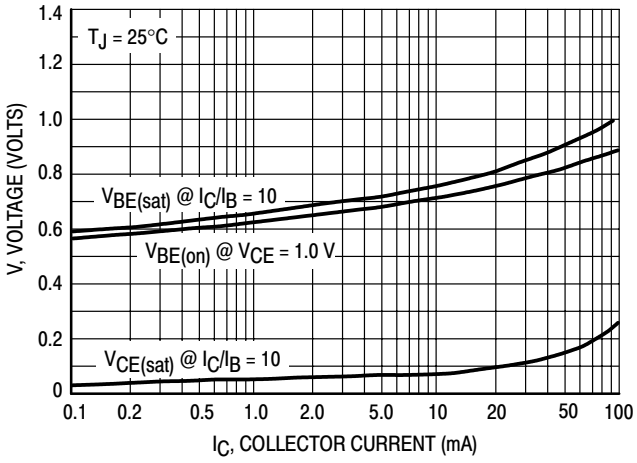



**Figure 31. “On” Voltages**

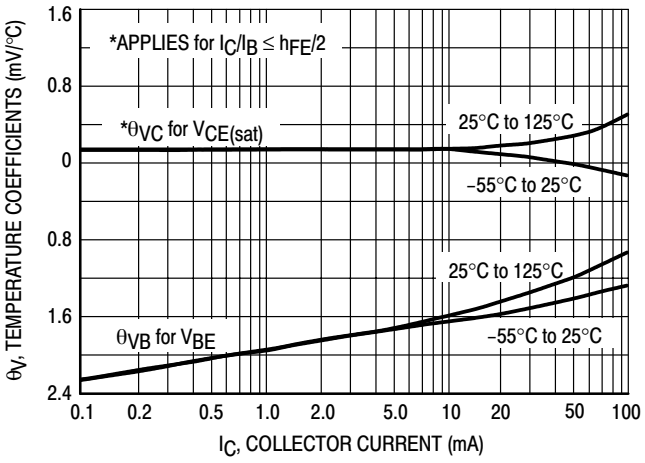



**Figure 32. Temperature Coefficients**

## PNP
## MPS6523
## TYPICAL DYNAMIC CHARACTERISTICS

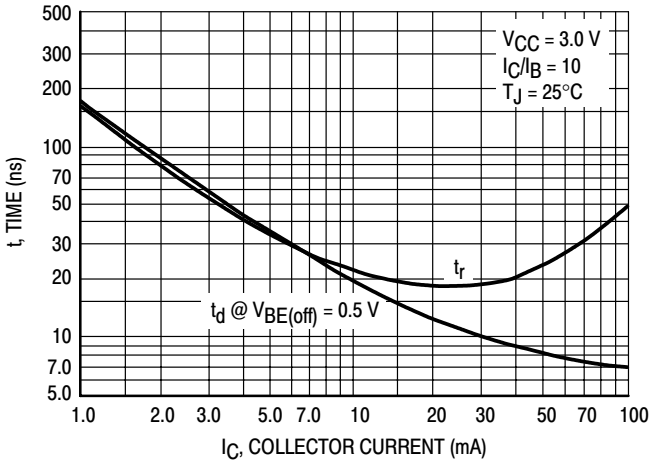



**Figure 33. Turn–On Time**

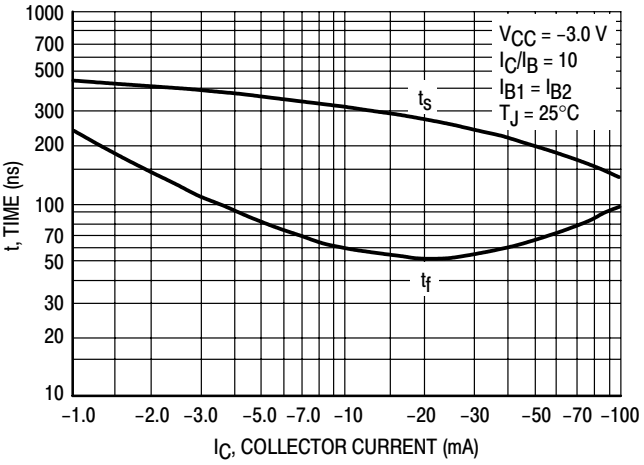



**Figure 34. Turn–Off Time**

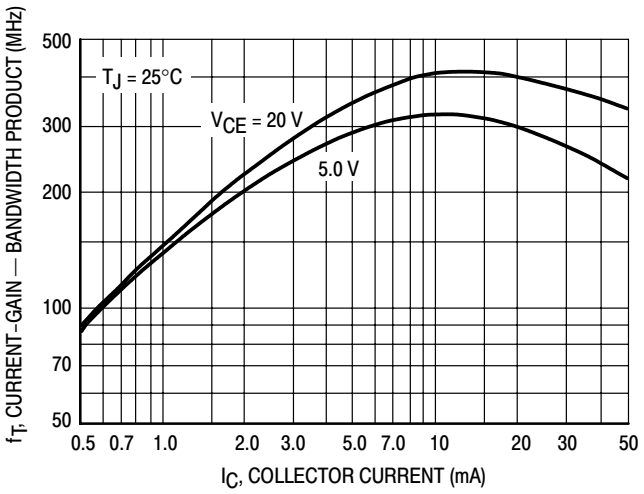



**Figure 35. Current–Gain — Bandwidth Product**

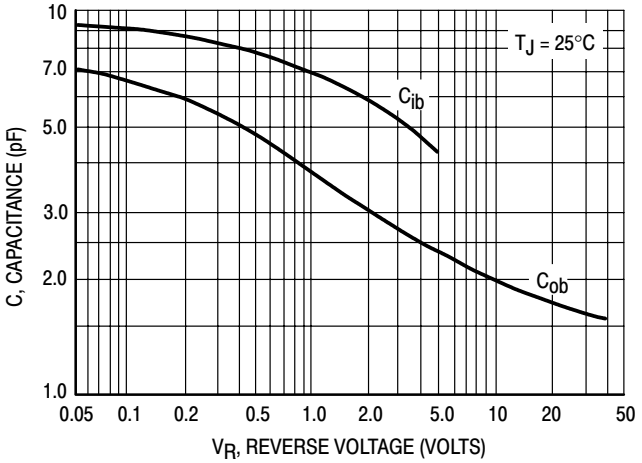



**Figure 36. Capacitance**

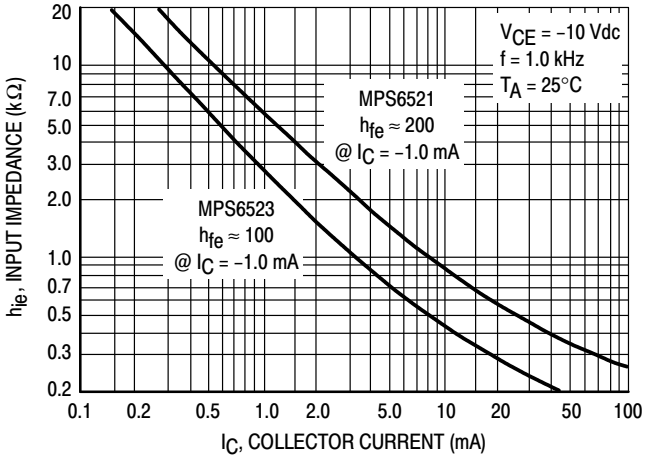



**Figure 37. Input Impedance**

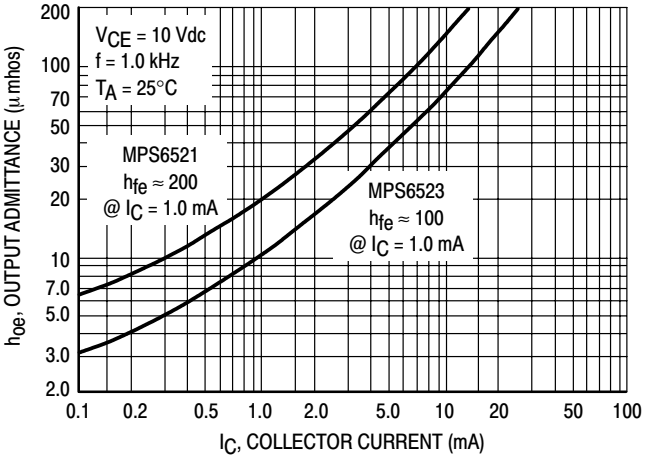



**Figure 38. Output Admittance**

**PNP**
**MPS6523**

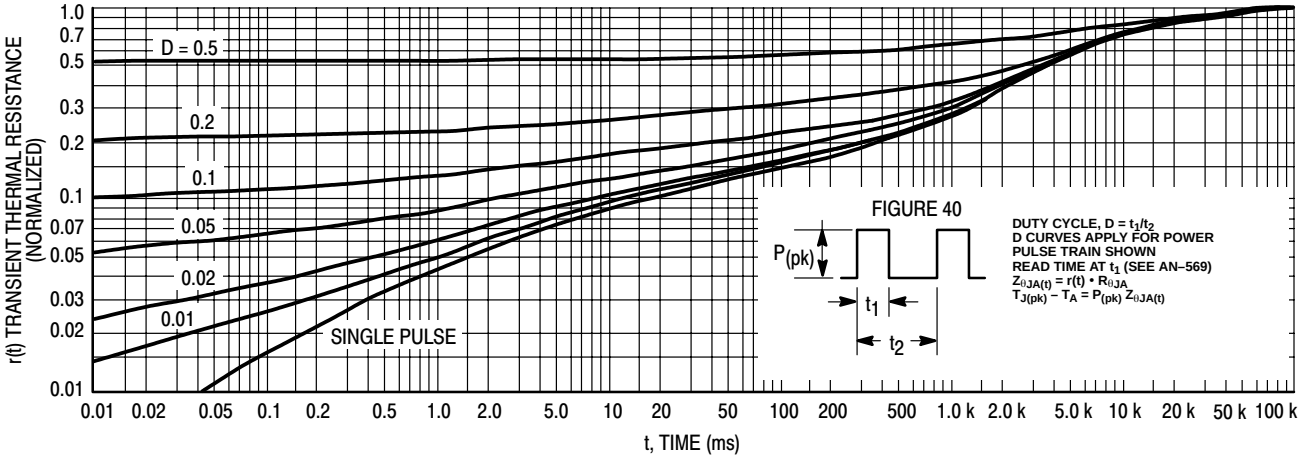



**Figure 39. Thermal Response**

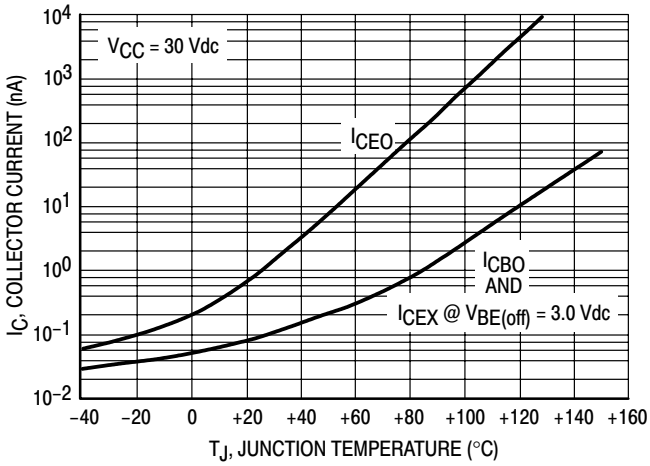



**Figure 41.**

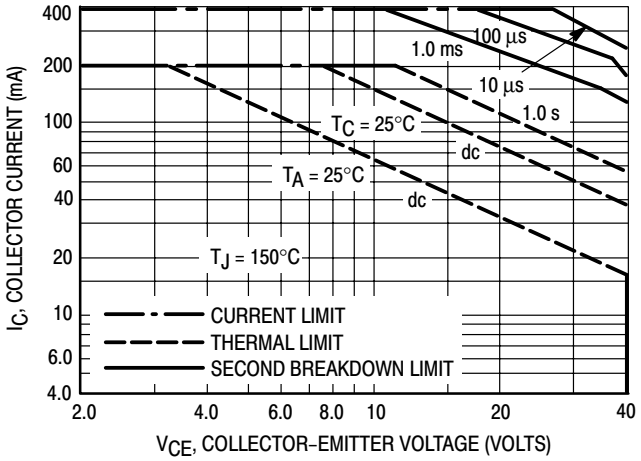



**Figure 42.**

**DESIGN NOTE: USE OF THERMAL RESPONSE DATA**

A train of periodical power pulses can be represented by the model as shown in Figure 40. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 39 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 39 by the steady state value $R_{\theta JA}$.

Example:

The MPS6523 is dissipating 2.0 watts peak under the following conditions:

$t_1$ = 1.0 ms, $t_2$ = 5.0 ms. (D = 0.2)

Using Figure 39 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore

$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88°C$.

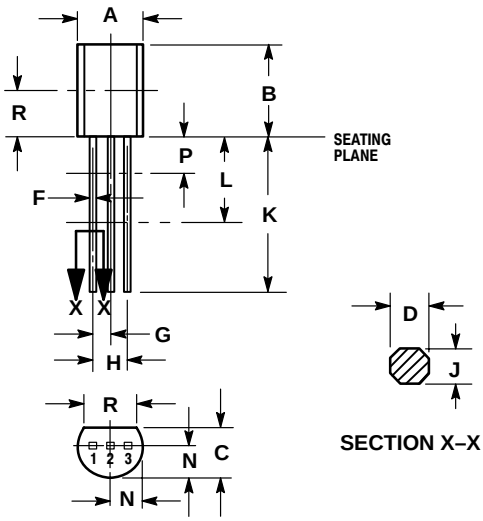
For more information, see ON Semiconductor Application Note AN569/D, available from the Literature Distribution Center or on our website at **www.onsemi.com**.

The safe operating area curves indicate $I_C–V_{CE}$ limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 42 is based upon $T_{J(pk)}$ = 150°C; $T_C$ or $T_A$ is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 39. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

## PACKAGE DIMENSIONS

**CASE 029–11**
**(TO–226AA)**
**ISSUE AD**




SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MIMIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.44 | 5.21 |
| B | 0.290 | 0.310 | 7.37 | 7.87 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.018 | 0.021 | 0.457 | 0.533 |
| F | 0.016 | 0.019 | 0.407 | 0.482 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.018 | 0.024 | 0.46 | 0.61 |
| K | 0.500 | --- | 12.70 | --- |
| L | 0.250 | --- | 6.35 | --- |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | --- | 0.100 | --- | 2.54 |
| R | 0.135 | --- | 3.43 | --- |

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

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