

NL17SZ02

2-Input NOR Gate

The NL17SZ02 is a single 2-input NOR Gate in two tiny footprint packages. The device performs much as LCX multi-gate products in speed and drive.

Features

- Tiny SOT-353 and SOT-553 Packages
- 2.4 ns T_{PD} at 5 V (typ)
- Source/Sink 24 mA at 3.0 V
- Over-Voltage Tolerant Inputs
- Pin For Pin with NC7SZ02P5X, TC7SZ02FU and TC7SZ02AFE
- Chip Complexity: FETs = 20
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Pb-Free Packages are Available

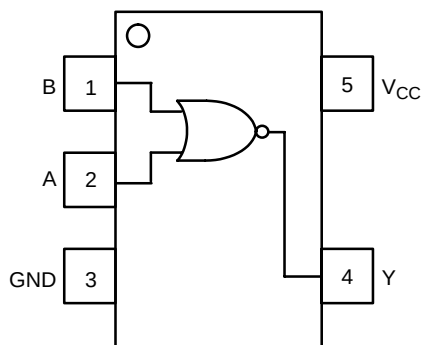


Figure 1. Pinout (Top View)

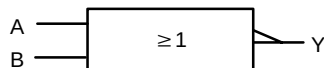


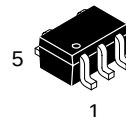
Figure 2. Logic Symbol



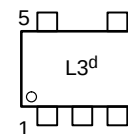
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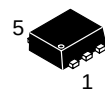
MARKING DIAGRAMS



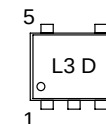
SOT-353/SC70-5/SC-88A
DF SUFFIX
CASE 419A



d = Date Code



SOT-553
XV5 SUFFIX
CASE 463B



L3 = Device Marking
D = One Digit Date Code

PIN ASSIGNMENT

Pin	Function
1	A
2	B
3	GND
4	Y
5	V_{CC}

FUNCTION TABLE

Input		Output $Y = \overline{A + B}$
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V _{IN}	DC Input Voltage	− 0.5 to + 7.0	V
V _{OUT}	DC Output Voltage	− 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	− 50	mA
I _{OK}	DC Output Diode Current	− 50	mA
I _{OUT}	DC Output Sink Current	± 50	mA
I _{CC}	DC Supply Current per Supply Pin	± 100	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+ 150	°C
θ _{JA}	Thermal Resistance	SOT-353 (Note 1) SOT-553 350 496	°C/W
P _D	Power Dissipation in Still Air at 85°C	SOT-353 SOT-553 186 135	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in	
ESD	ESD Classification	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) Class Z Class A N/A	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A, rated to EIA/JESD22-A114-B.
3. Tested to EIA/JESD22-A115-A, rated to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	1.65	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	V _{CC} + 0.5	V
T _A	Operating Temperature Range	− 40	+ 85	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 3.0 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V 0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			−40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 to 1.95 2.3 to 5.5	0.75 V _{CC} 0.7 V _{CC}			0.75 V _{CC} 0.7 V _{CC}		V
V _{IL}	Low-Level Input Voltage		1.65 to 1.95 2.3 to 5.5			0.25 V _{CC} 0.3 V _{CC}		0.25 V _{CC} 0.3 V _{CC}	V
V _{OH}	High-Level Output Voltage V _{IN} = V _{IL} or V _{IH}	I _{OH} = 100 μA I _{OH} = −3 mA I _{OH} = −8 mA I _{OH} = −12 mA I _{OH} = −16 mA I _{OH} = −24 mA I _{OH} = −32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V _{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V _{CC} 1.52 2.1 2.4 2.7 2.5 4.0		V _{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8		V
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH} or V _{OH}	I _{OL} = 100 μA I _{OL} = 3 mA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.08 0.20 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I _{IN}	Input Leakage Current	V _{IN} = V _{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 3.0 ns

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			−40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay (Figure 3 and 4)	R _L = 1 MΩ, C _L = 15 pF	1.65	2.0	5.3	11.5	2.0	12.0	ns
		R _L = 1 MΩ, C _L = 15 pF	1.8	2.0	4.4	9.5	2.0	10.0	
		R _L = 1 MΩ, C _L = 15 pF	2.5 ± 0.2	0.8	2.9	6.5	0.8	7.0	
		R _L = 1 MΩ, C _L = 15 pF	3.3 ± 0.3	0.5	2.3	4.5	0.5	4.7	
		R _L = 500 Ω, C _L = 50 pF		1.5	2.9	5.0	1.5	5.2	
		R _L = 1 MΩ, C _L = 15 pF	5.0 ± 0.5	0.5	1.9	3.9	0.5	4.1	
		R _L = 500 Ω, C _L = 50 pF		0.8	2.4	4.3	0.8	4.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	> 4	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC} 10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	25 30	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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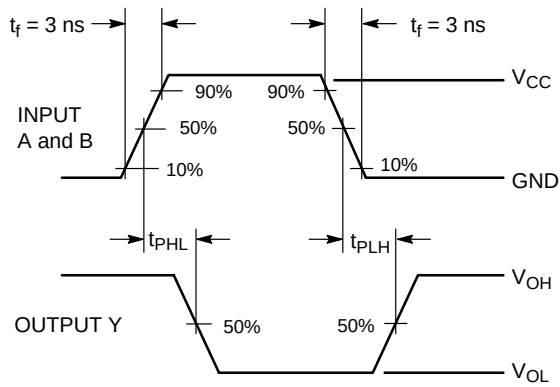
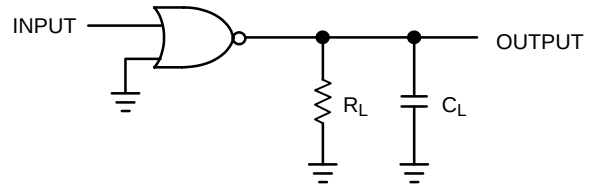


Figure 3. Switching Waveform



A 1-MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size [†]
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
NL17SZ02DFT2	NL	1	7	SZ	02	DF	T2	SOT-353/ SC70-5/ SC-88A	178 mm, 3000 Units
NL17SZ02DFT2G	NL	1	7	SZ	02	DF	T2	SOT-353/ SC70-5/ SC-88A (Pb-Free)	178 mm, 3000 Units
NL17SZ02XV5T2	NL	1	7	SZ	02	XV5	T2	SOT-553*	178 mm 4000 Units

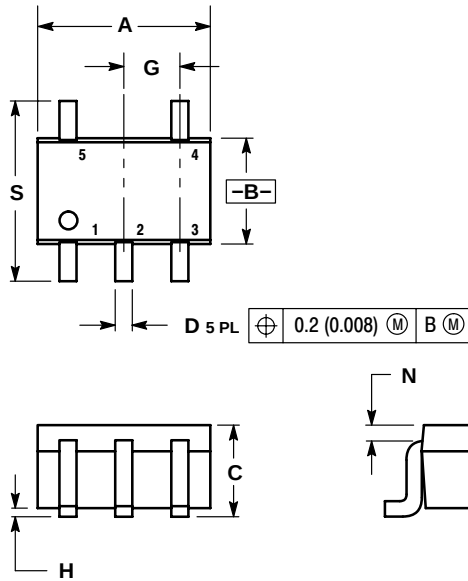
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*All Devices in Package SOT553 are Inherently Pb-Free.

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PACKAGE DIMENSIONS

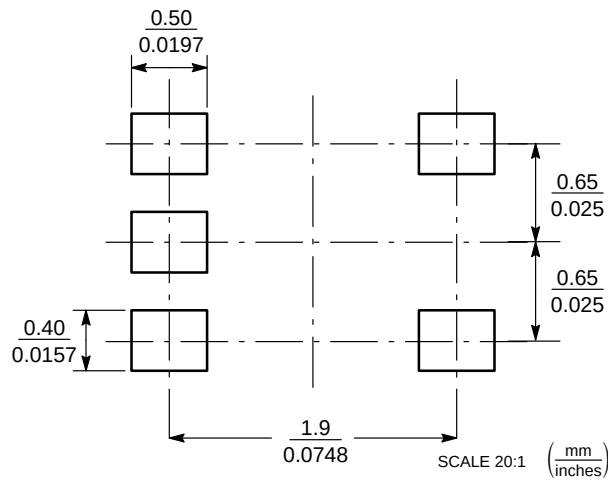
SOT-353
DF SUFFIX
5-LEAD PACKAGE
CASE 419A-02
ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*

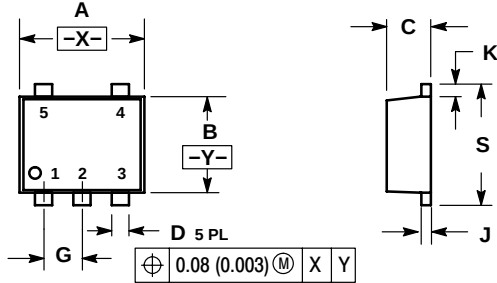


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ02

PACKAGE DIMENSIONS

SOT-553
XV5 SUFFIX
5-LEAD PACKAGE
CASE 463B-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

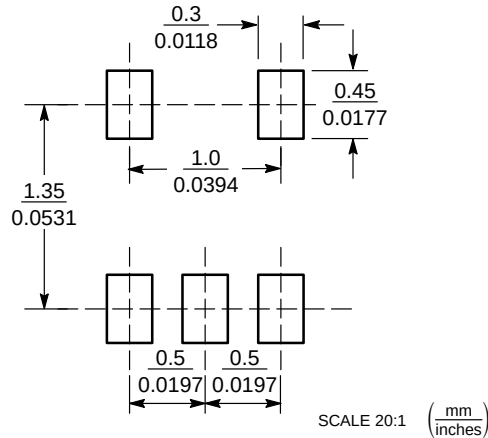
STYLE 1:

- PIN 1. BASE 1
- EMITTER 1/2
- BASE 2
- COLLECTOR 2
- COLLECTOR 1

STYLE 2:

- PIN 1. CATHODE
- ANODE
- CATHODE
- CATHODE
- CATHODE

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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