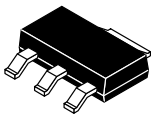
SOT-223 Triac
Silicon Bidirectional Thyristors

MAC08BT1 Series *
***Motorola preferred devices**

Designed for use in solid state relays, MPU interface, TTL logic and other light industrial or consumer applications. Supplied in surface mount package for use in automated manufacturing.

- Sensitive Gate Trigger Current in Four Trigger Modes
- Blocking Voltage to 600 Volts
- Glass Passivated Surface for Reliability and Uniformity
- Surface Mount Package
- Devices Supplied on 1 K Reel

TRIAC
0.8 AMPERE RMS
200 thru 600 Volts



CASE 318E-04
(SOT-223)
STYLE 11

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Blocking Voltage(1) (1/2 Sine Wave, Gate Open, T_J = 25 to 110°C) MAC08BT1 MAC08DT1 MAC08MT1	V_{DRM}	200 400 600	Volts
On-State Current RMS (T_C = 80°C)	$I_{T(RMS)}$	0.8	Amps
Peak Non-repetitive Surge Current (One Full Cycle, 60 Hz, T_C = 25°C)	I_{TSM}	10	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.4	A^2s
Peak Gate Power (t < 2.0 μs)	P_{GM}	5.0	Watts
Average Gate Power (T_C = 80°C, t = 8.3 ms)	$P_{G(AV)}$	0.1	Watts
Operating Junction Temperature Range	T_J	–40 to +110	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C
Maximum Device Temperature for Soldering Purposes (for 5 Seconds Maximum)	T_L	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient PCB Mounted per Figure 1	$R_{\theta JA}$	156	°C/W
Thermal Resistance, Junction to Tab Measured on Anode Tab Adjacent to Epoxy	$R_{\theta JT}$	25	°C/W

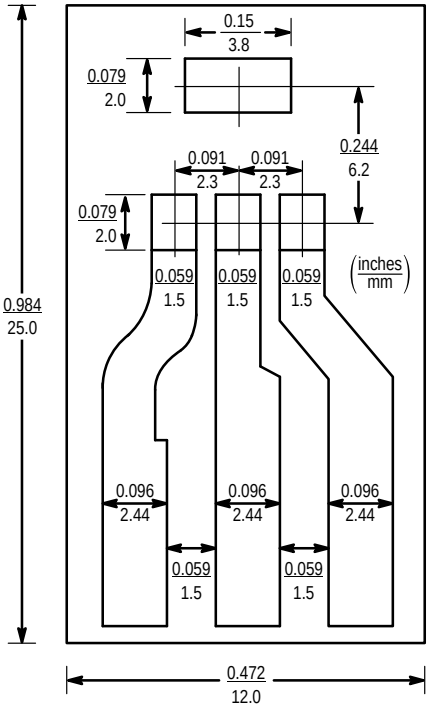
1. V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Repetitive Blocking Current (V_D = Rated V_{DRM} Gate Open) T_J = 25°C T_J = 110°C	I_{DRM}	 — —	 — —	 10 200	 μA μA
Maximum On-State Voltage (Either Direction) (I_T = 1.1 A Peak, T_A = 25°C)	V_{TM}	—	—	1.9	Volts
Gate Trigger Current (Continuous dc) All Quadrants (V_D = 7.0 Vdc, R_L = 100 Ω)	I_{GT}	—	—	10	mA
Holding Current (Either Direction) (V_D = 7.0 Vdc, Gate Open, Initiating Current = 20 mA, Gate Open)	I_H	—	—	5.0	mA
Gate Trigger Voltage (Continuous dc) All Quadrants (V_D = 7.0 Vdc, R_L = 100 Ω)	V_{GT}	—	—	2.0	Volts
Critical Rate of Rise of Commutation Voltage (f = 250 Hz, I_{TM} = 1.0 A, Commutating di/dt = 1.5 A/mS On-State Current Duration = 2.0 mS, V_{DRM} = 200 V, Gate Unenergized, T_C = 110°C, Gate Source Resistance = 150 Ω, See Figure 10)	dv/dt_c	1.5	—	—	V/μs
Critical Rate-of-Rise of Off State Voltage (V_{pk} = Rated V_{DRM}, T_C = 110°C, Gate Open, Exponential Method)	dv/dt	10	—	—	V/μs



BOARD MOUNTED VERTICALLY IN CINCH 8840 EDGE CONNECTOR.
BOARD THICKNESS = 65 MIL., FOIL THICKNESS = 2.5 MIL.
MATERIAL: G10 FIBERGLASS BASE EPOXY

Figure 1. PCB for Thermal Impedance and Power Testing of SOT-223

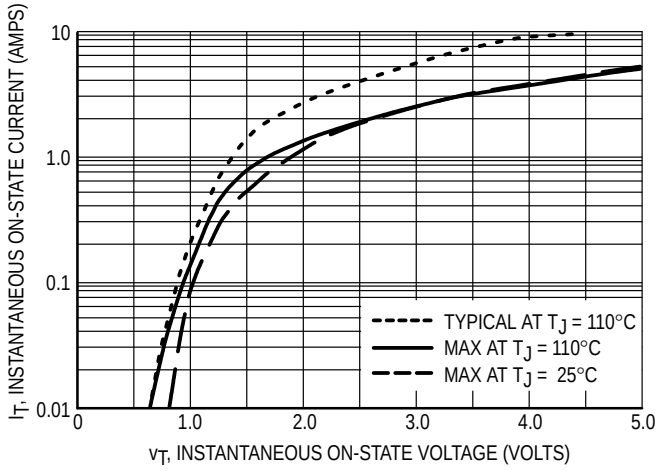


Figure 2. On-State Characteristics

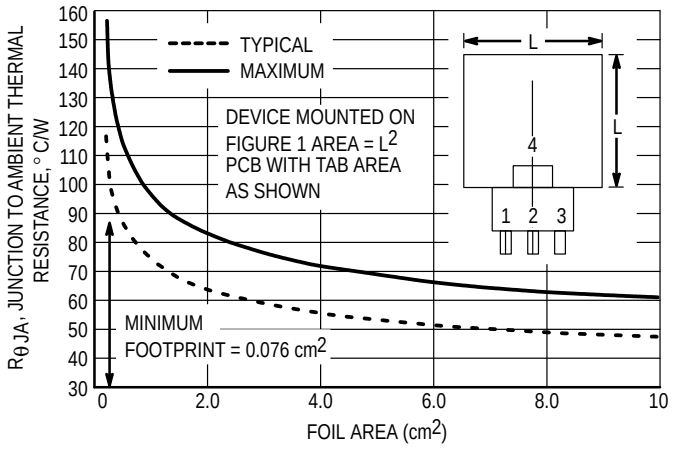


Figure 3. Junction to Ambient Thermal Resistance versus Copper Tab Area

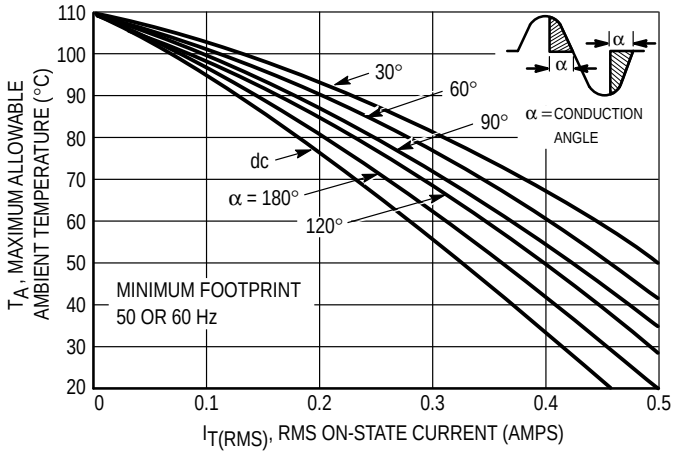


Figure 4. Current Derating, Minimum Pad Size Reference: Ambient Temperature

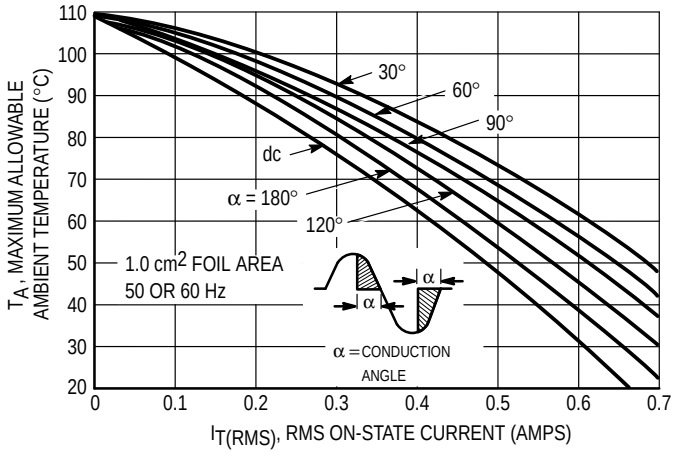


Figure 5. Current Derating, 1.0 cm Square Pad Reference: Ambient Temperature

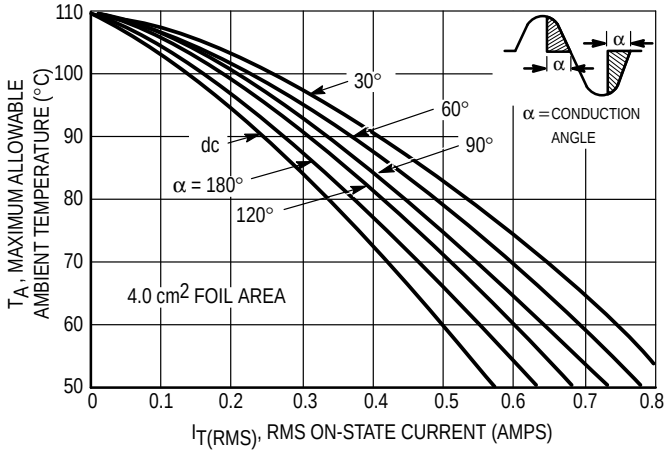


Figure 6. Current Derating, 2.0 cm Square Pad Reference: Ambient Temperature

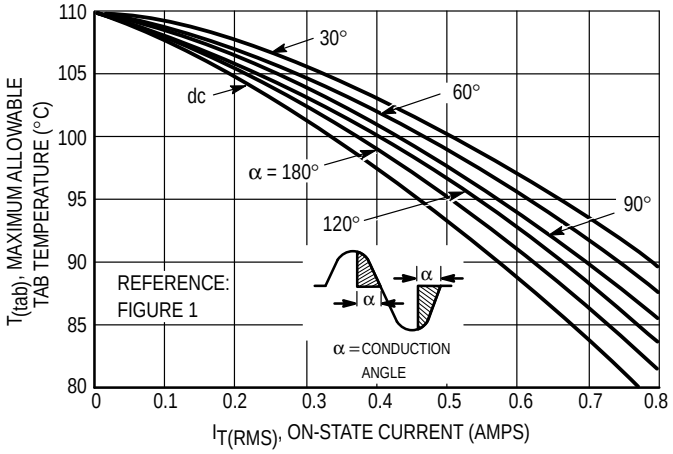


Figure 7. Current Derating Reference: MT2 Tab

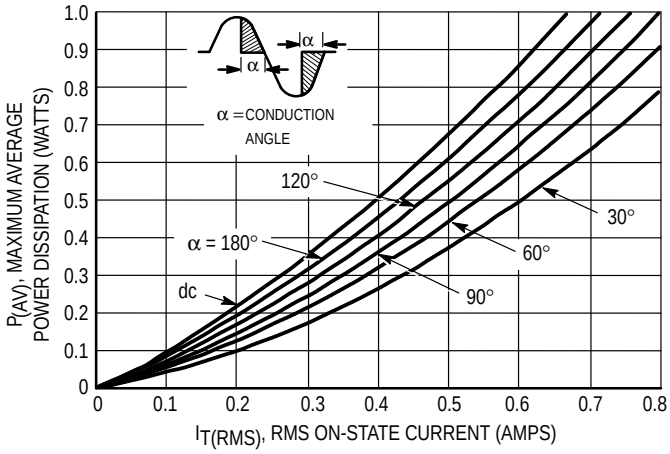


Figure 8. Power Dissipation

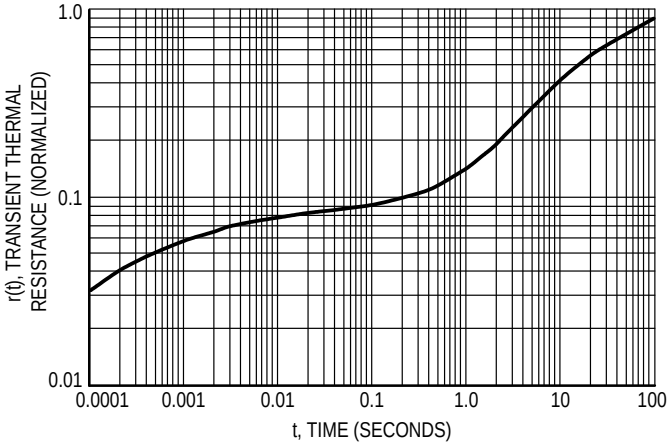
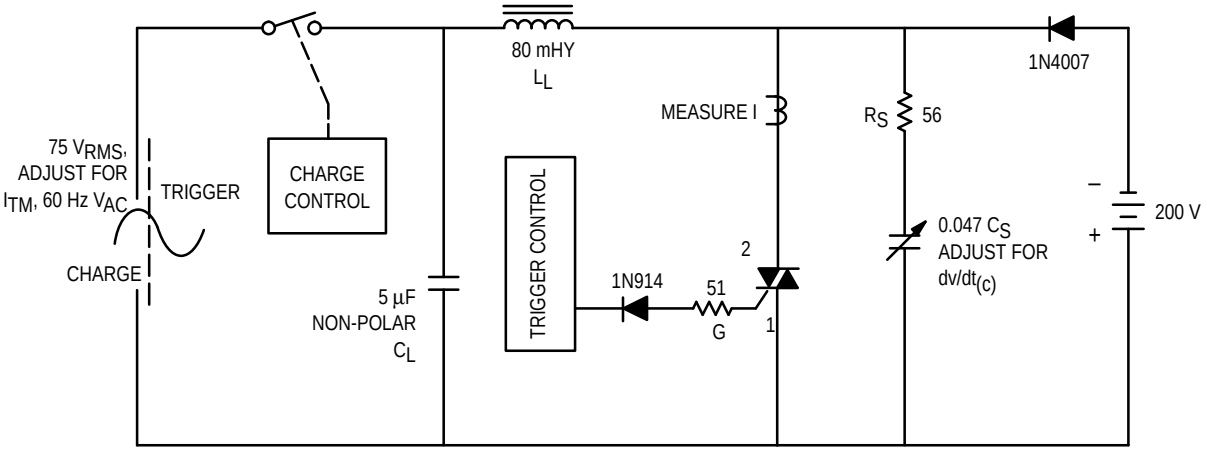


Figure 9. Thermal Response, Device Mounted on Figure 1 Printed Circuit Board



Component values are for verification of rated $(dv/dt)_C$. See AN1048 for additional information.

Figure 10. Simplified Q_1 $(dv/dt)_C$ Test Circuit

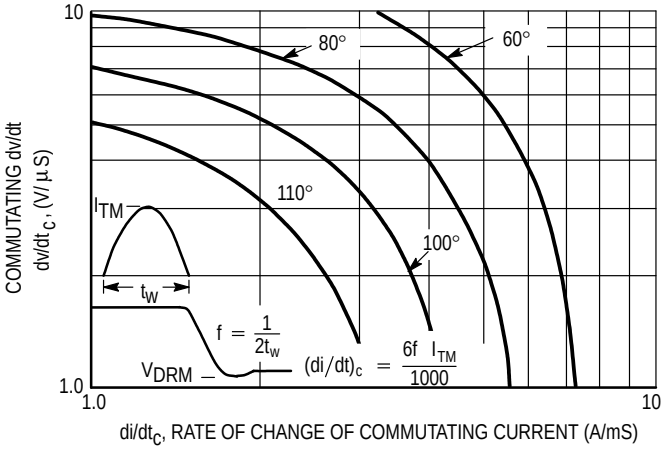


Figure 11. Typical Commutating dv/dt versus Current Crossing Rate and Junction Temperature

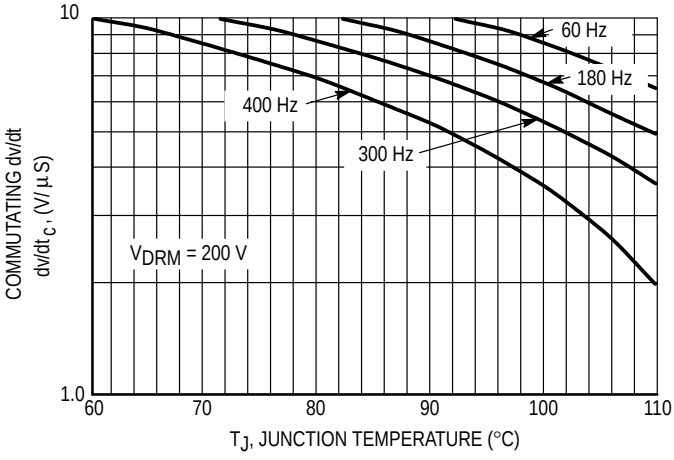


Figure 12. Typical Commutating dv/dt versus Junction Temperature at 0.8 Amps RMS

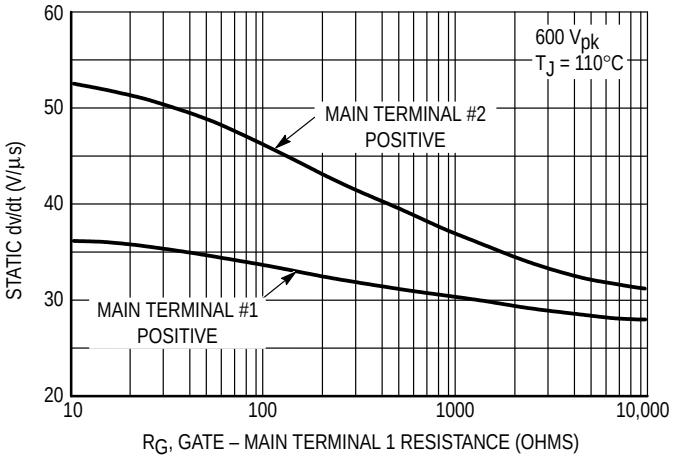


Figure 13. Exponential Static dv/dt versus Gate – Main Terminal 1 Resistance

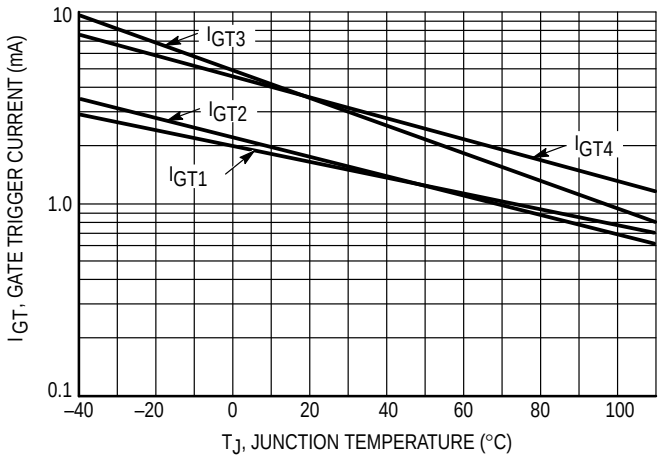


Figure 14. Typical Gate Trigger Current Variation

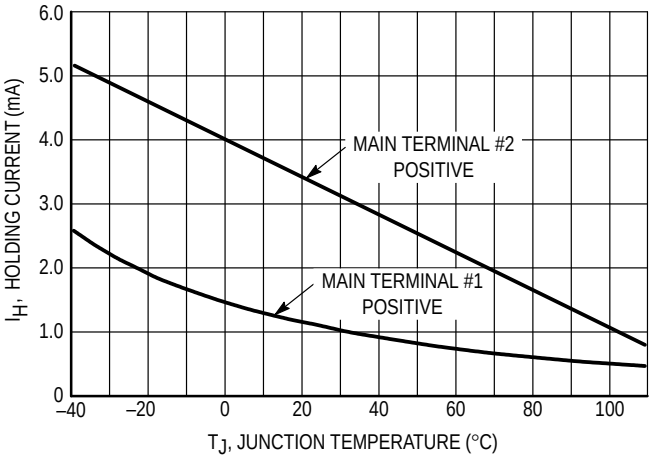


Figure 15. Typical Holding Current Variation

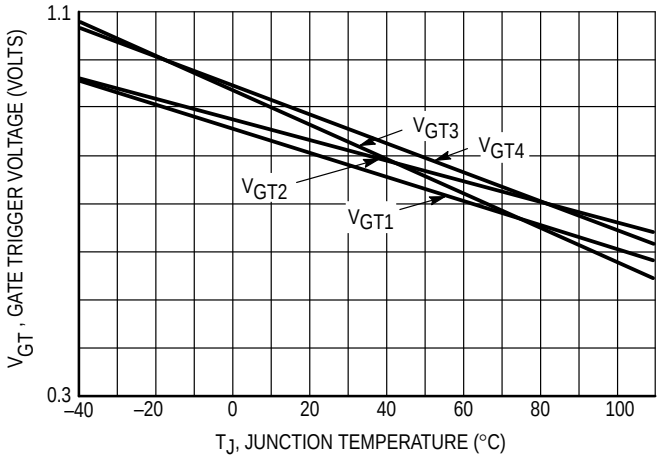


Figure 16. Gate Trigger Voltage Variation