

BALANCED MODULATOR/ DEMODULATOR

These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN531 for additional design information.

- Excellent Carrier Suppression — 65 dB typ @ 0.5 MHz
— 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection — 85 dB typ

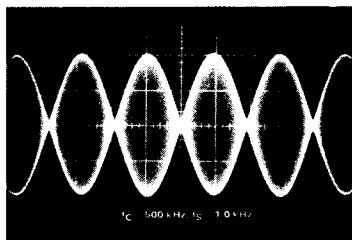


FIGURE 1 —
SUPPRESSED CARRIER
OUTPUT WAVEFORM

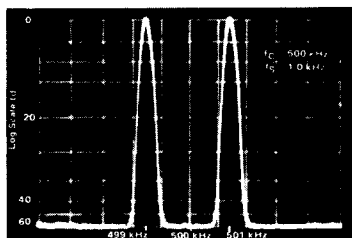


FIGURE 2 —
SUPPRESSED CARRIER
SPECTRUM

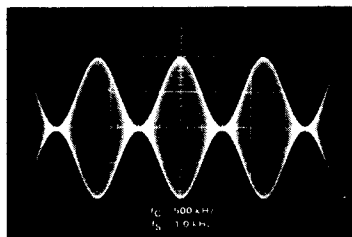
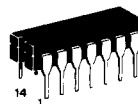


FIGURE 3 —
AMPLITUDE MODULATION
OUTPUT WAVEFORM

MC1496
MC1596

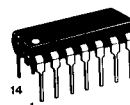
BALANCED MODULATOR/DEMODULATOR



L SUFFIX
CERAMIC PACKAGE
CASE 632



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



P SUFFIX
PLASTIC PACKAGE
CASE 646

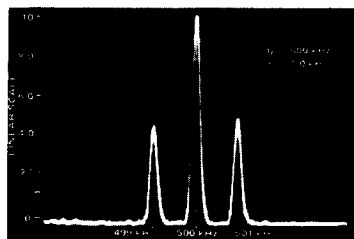
PIN ASSIGNMENTS

Signal Input	1	14	VEE
Gain Adjust	2	13	NC
Gain Adjust	3	12	Output
Signal Input	4	11	NC
Bias	5	10	Carrier Input
Output	6	9	NC
NC	7	8	Input Carrier

ORDERING INFORMATION

Device	Temperature Range	Package
MC1496D	0°C to +70°C	SO-14
MC1496L		Ceramic DIP
MC1496P		Plastic DIP
MC1596L	-55°C to +125°C	Ceramic DIP

FIGURE 4 — AMPLITUDE-MODULATION SPECTRUM



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MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V ₆ - V ₈ , V ₁₀ - V ₁ , V ₁₂ - V ₈ , V ₁₂ - V ₁₀ , V ₈ - V ₄ , V ₈ - V ₁ , V ₁₀ - V ₄ , V ₆ - V ₁₀ , V ₂ - V ₅ , V ₃ - V ₅)	ΔV	30	Vdc
Differential Input Signal	V ₈ - V ₁₀ V ₄ - V ₁	+5.0 ± (5 + I ₅ R _θ)	Vdc
Maximum Bias Current	I ₅	10	mA
Thermal Resistance, Junction to Air Ceramic Dual In-Line Package Plastic Dual In-Line Package Metal Package	R _{θJA}	100 100 160	°C/W
Operating Temperature Range	T _A	0 to +70 -55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = -8.0 Vdc, I₅ = 1.0 mAdc, R_L = 3.9 kΩ, R_θ = 1.0 kΩ, T_A = +25°C, all input and output characteristics are single-ended, unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	MC1596			MC1496			Unit
				Min	Typ	Max	Min	Typ	Max	
Carrier Feedthrough V _C = 60 mV(rms) sine wave and offset adjusted to zero V _C = 300 mVp-p square wave: offset adjusted to zero offset not adjusted	5	1	V _{CFT}	—	40 140	—	—	40 140	—	μV(rms) mV(rms)
Carrier Suppression f _S = 10 kHz, 300 mV(rms) f _C = 500 kHz, 60 mV(rms) sine wave f _C = 10 MHz, 60 mV(rms) sine wave	5	2	V _{CS}	50 —	65 50	—	40 —	65 50	—	dB k
Transadmittance Bandwidth (Magnitude) (R _L = 50 ohms) Carrier Input Port, V _C = 60 mV(rms) sine wave f _S = 1.0 kHz, 300 mV(rms) sine wave Signal Input Port, V _S = 300 mV(rms) sine wave V _C = 0.5 Vdc	8	8	BW _{3dB}	—	300 80	—	—	300 80	—	MHz
Signal Gain V _S = 100 mV(rms), f = 1.0 kHz; V _C = 0.5 Vdc	10	3	A _{VS}	2.5	3.5	—	2.5	3.5	—	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz Parallel Input Resistance Parallel Input Capacitance	6	—	r _{ip} c _{ip}	—	200 2.0	—	—	200 2.0	—	kΩ pF
Single-Ended Output Impedance, f = 10 MHz Parallel Output Resistance Parallel Output Capacitance	6	—	r _{op} c _{oo}	—	40 5.0	—	—	40 5.0	—	kΩ pF
Input Bias Current I _{BS} = $\frac{I_1 + I_4}{2}$, I _{BC} = $\frac{I_8 + I_{10}}{2}$	7	—	I _{BS} I _{BC}	—	12 12	25 25	—	12 12	30 30	μA
Input Offset Current I _{IOS} = I ₁ - I ₄ ; I _{IOC} = I ₈ - I ₁₀	7	—	I _{IOS} I _{IOC}	—	0.7 0.7	5.0 5.0	—	0.7 0.7	7.0 7.0	μA
Average Temperature Coefficient of Input Offset Current (T _A = -55°C to +125°C)	7	—	TC _{IOS}	—	2.0	—	—	2.0	—	nA/°C
Output Offset Current (I ₆ - I ₉)	7	—	I _{ool}	—	14	50	—	14	80	μA
Average Temperature Coefficient of Output Offset Current (T _A = -55°C to +125°C)	7	—	TC _{IOol}	—	90	—	—	90	—	nA/°C
Common-Mode Input Swing, Signal Port, f _S = 1.0 kHz	9	4	CMV	—	5.0	—	—	5.0	—	Vp-p
Common-Mode Gain, Signal Port, f _S = 1.0 kHz, V _C = 0.5 Vdc	9	—	ACM	—	-85	—	—	-85	—	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	—	V _{out}	—	8.0	—	—	8.0	—	Vp-p
Differential Output Voltage Swing Capability	10	—	V _{out}	—	8.0	—	—	8.0	—	Vp-p
Power Supply Current I ₆ + I ₁₂ I ₁₄	7	6	I _{CC} I _{EE}	—	2.0 3.0	3.0 4.0	—	2.0 3.0	4.0 5.0	mAdc
DC Power Dissipation	7	5	P _D	—	33	—	—	33	—	mW

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GENERAL OPERATING INFORMATION

Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R₁ of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair — or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_O}{V_S} = \frac{R_L}{R_E + 2r_e} \quad \text{where } r_e = \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I₅.

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1 volt peak.

Common Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming V₁₂ = V₆, I₅ = I₆ = I₁₂ and ignoring base current, P_D = 2 I₅ (V₆ - V₁₄) + I₅ V₅ - V₁₄ where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_{12},$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V - \phi}{I_5} - 500 \Omega \quad \text{where: } R_5 \text{ is the resistor between pin 5 and ground}$$

$$\phi = 0.75 \text{ V at } T_A = +25^\circ\text{C}$$

The MC1596 has been characterized for the condition I₅ = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_{12} = V^+ - I_5 R_L$$

Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30 \text{ Vdc} \geq [(V_6, V_{12}) - (V_8, V_{10})] \geq 2 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_8, V_{10}) - (V_1, V_4)] \geq 2.7 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7 \text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_{12}, V_8 = V_{10}, V_1 = V_4$$

Bias currents flowing into pins 1, 4, 8, and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma_{21C} = \frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}} \bigg|_{V_O = 0}$$

Signal transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma_{21S} = \frac{i_o \text{ (signal)}}{v_s \text{ (signal)}} \bigg|_{V_C = 0.5 \text{ Vdc}, V_O = 0}$$

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Coupling and Bypass Capacitors

Capacitors C_1 and C_2 (Figure 5) should be selected for a reactance of less than $5.0\ \Omega$ at the carrier frequency.

Output Signal

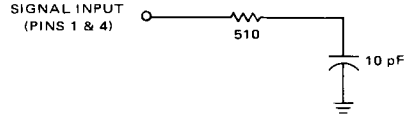
The output signal is taken from Pins 6 and 12 either balanced or single-ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Negative Supply

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Signal Port Stability

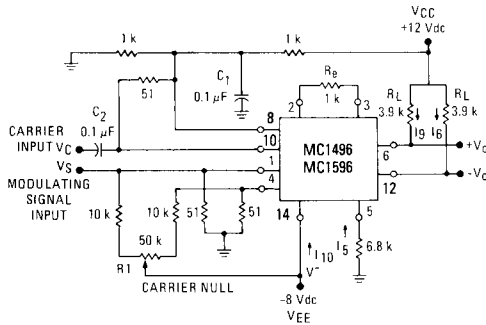
Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a $1.0\ k\Omega$ resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 5 — CARRIER REJECTION AND SUPPRESSION



NOTE: Shielding of input and output leads may be needed to properly perform these tests.

FIGURE 6 — INPUT-OUTPUT IMPEDANCE

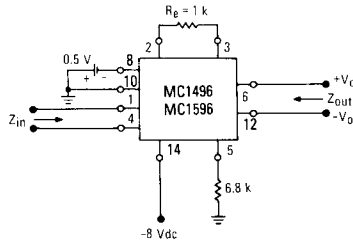


FIGURE 7 — BIAS AND OFFSET CURRENTS

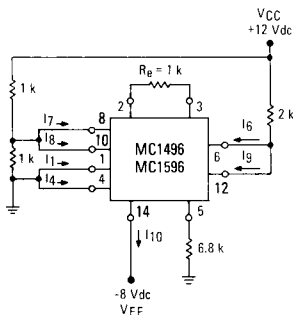
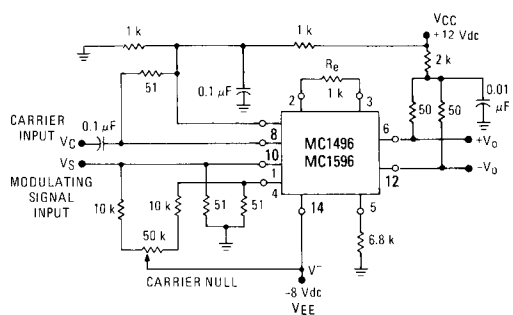


FIGURE 8 — TRANSCONDUCTANCE BANDWIDTH



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FIGURE 9 – COMMON MODE GAIN

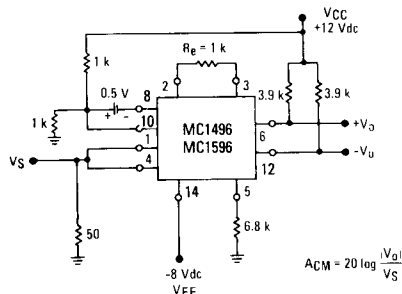
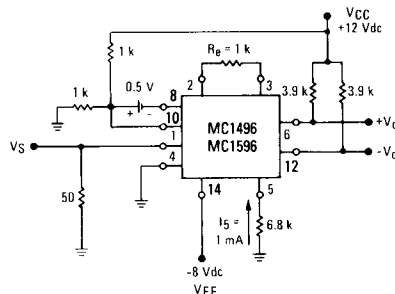


FIGURE 10 – SIGNAL GAIN AND OUTPUT SWING



TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, $f_C = 500$ kHz (sine wave), $V_C = 60$ mV(rms), $f_S = 1$ kHz, $V_S = 300$ mV(rms), $T_A = +25^\circ\text{C}$ unless otherwise noted.

FIGURE 11 – SIDEBAND OUTPUT versus CARRIER LEVELS

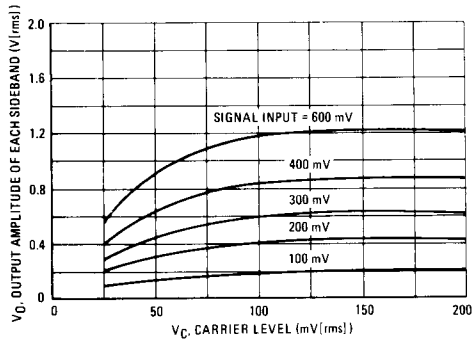


FIGURE 12 – SIGNAL PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

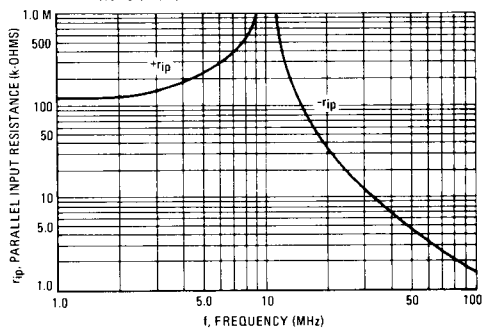


FIGURE 13 – SIGNAL PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

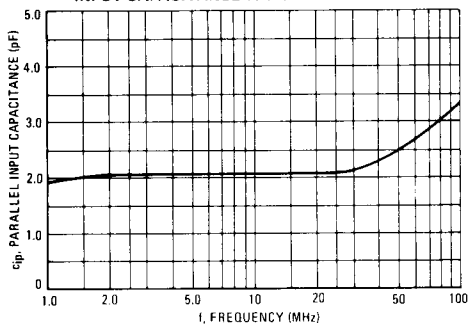
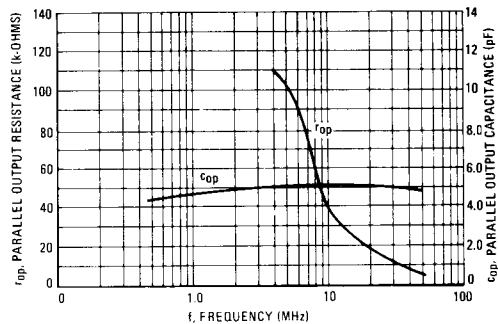


FIGURE 14 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



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TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, $f_C = 500$ kHz (sine wave),
 $V_C = 60$ mV(rms), $f_S = 1$ kHz, $V_S = 300$ mV(rms), $T_A = +25^\circ\text{C}$ unless otherwise noted.

FIGURE 15 – SIDE BAND AND SIGNAL PORT TRANSAMITTANCES versus FREQUENCY

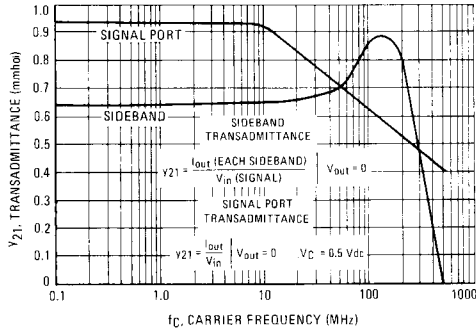


FIGURE 16 – CARRIER SUPPRESSION versus TEMPERATURE

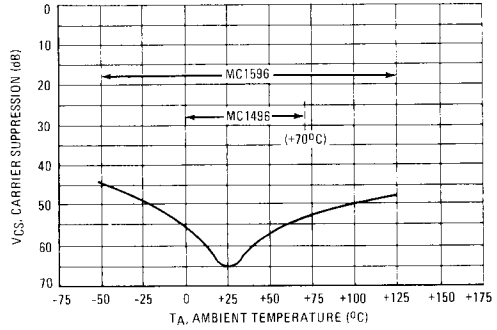


FIGURE 17 – SIGNAL-PORT FREQUENCY RESPONSE

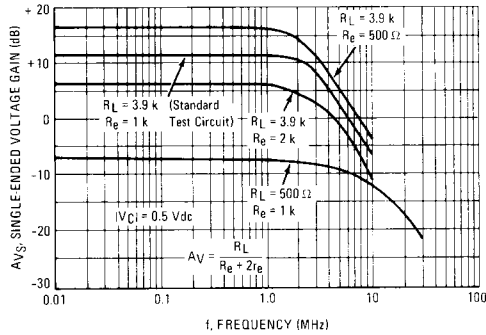


FIGURE 18 – CARRIER SUPPRESSION versus FREQUENCY

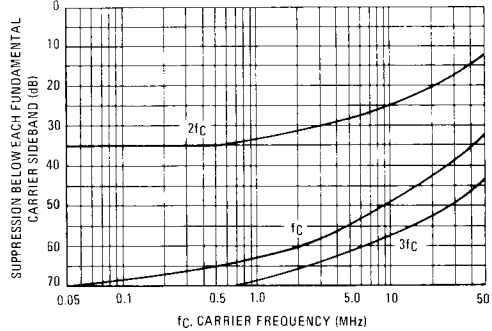


FIGURE 19 – CARRIER FEEDTHROUGH versus FREQUENCY

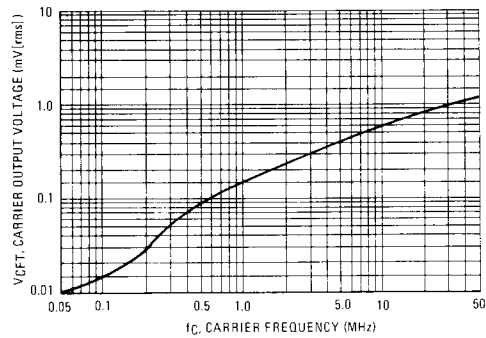
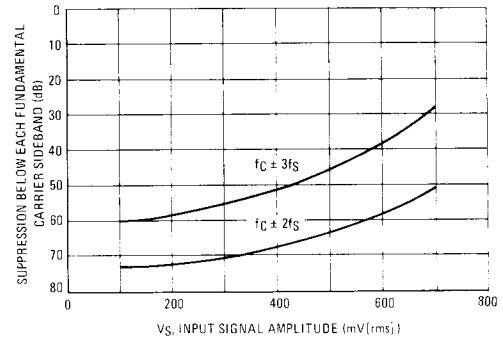


FIGURE 20 – SIDE BAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



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FIGURE 21 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

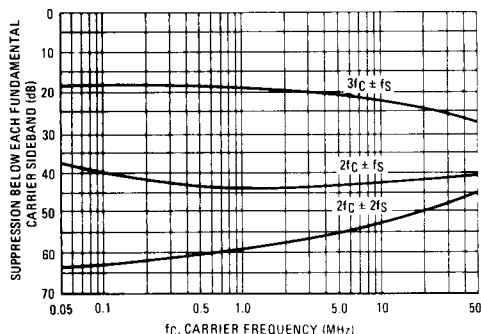
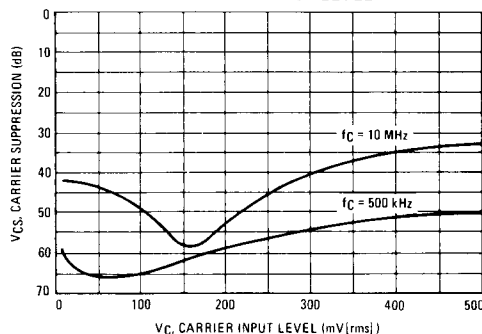


FIGURE 22 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

FIGURE 23 – CIRCUIT SCHEMATIC

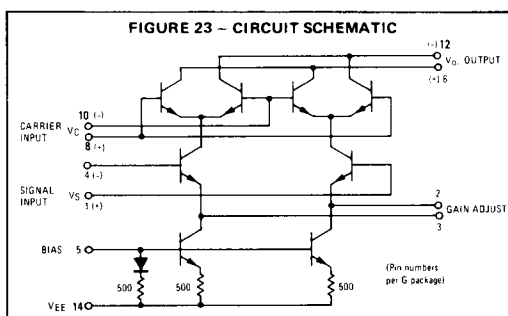
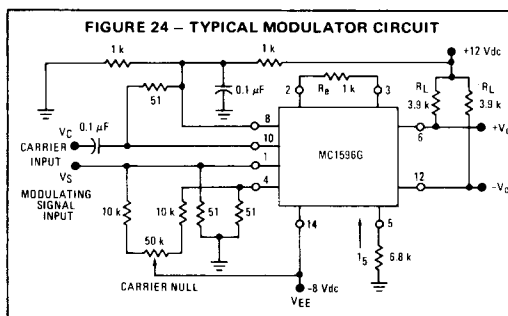


FIGURE 24 – TYPICAL MODULATOR CIRCUIT



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The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5) (R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

**FIGURE 25 — TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES**

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e) \left(\frac{KT}{q} \right)}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(\text{rms})}{2\sqrt{2} \left(\frac{KT}{q} \right) (R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637 R_L}{R_E + 2r_e}$	$f_C \pm f_M, 3f_C \pm f_M, 5f_C \pm f_M, \dots$

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

- 1) Low-level dc
- 2) High-level dc
- 3) Low-level ac
- 4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

NOTES:

1. Low-level Modulating Signal, V_M , assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at $+25^\circ\text{C}$;

$$r_e \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature}$$

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 8 and 10 should be increased to 1.0 μF . Also, the output filter at pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

MC1496, MC1596

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

TYPICAL APPLICATIONS

FIGURE 26 — BALANCED MODULATOR
(+12 Vdc SINGLE SUPPLY)

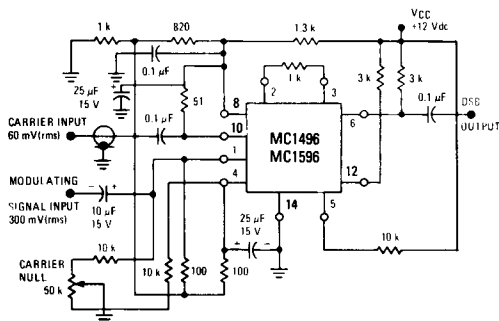


FIGURE 27 — BALANCED MODULATOR-DEMODULATOR

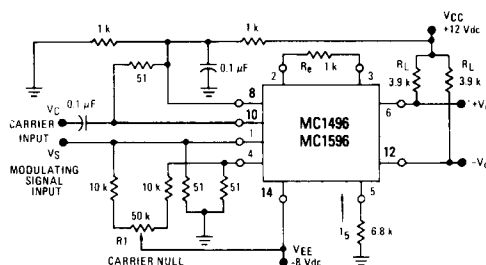


FIGURE 28 — AM MODULATOR CIRCUIT

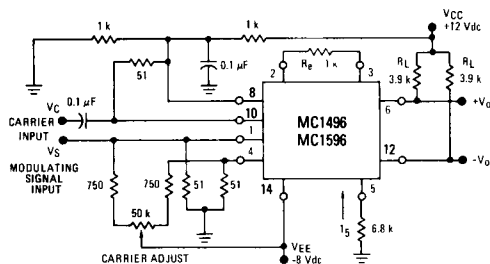
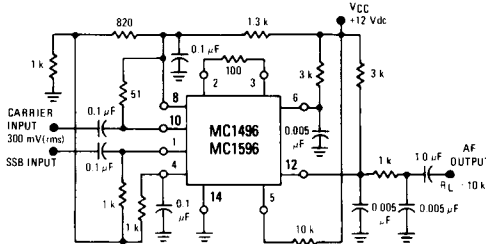
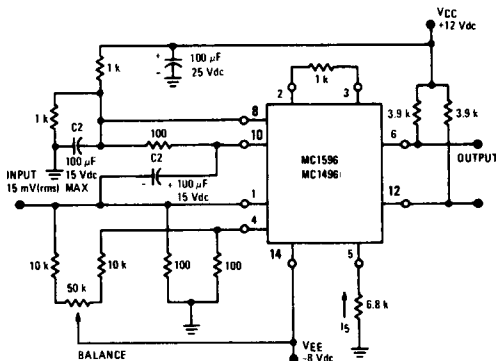


FIGURE 29 — PRODUCT DETECTOR
(+12 Vdc SINGLE SUPPLY)



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FIGURE 31 – LOW-FREQUENCY DOUBLER



The circuit diagram shows an MC1596 phase-locked loop (PLL) and an MC1496 double-balanced mixer. The PLL is configured with a 150 MHz input, a 100k feedback resistor, and a 1k divider. The mixer is driven by the PLL's output and a 300 MHz input. The output is taken from the mixer's output terminals and is a 300 MHz signal. The circuit is powered by a +8 Vdc supply and a -8 Vdc supply. Component values include resistors of 1k, 100, 10k, 50k, 100, and 1k, capacitors of 0.001 μF, 0.001 μF, 18 pF, 0.68 μH, 1-10 pF, and 1-10 pF, and an inductor L1 (18 nH). The output is labeled 300 MHz OUTPUT with $R_L = 50\Omega$. A note specifies L1 = 1 TURN AWG NO. 18 WIRE 7/32" ID.

