

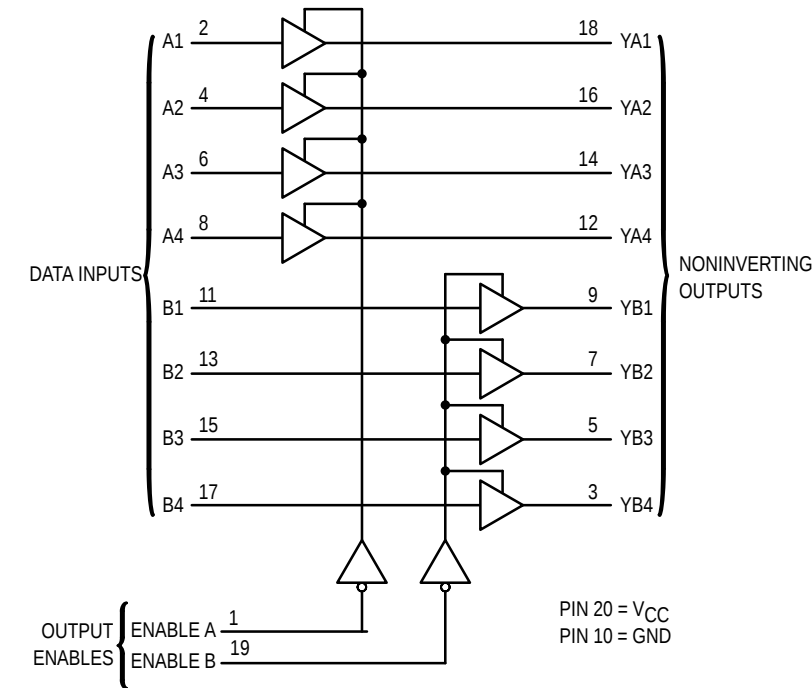
# Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT244A is identical in pinout to the LS244. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT244A is an octal noninverting buffer line driver line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two active-low output enables.

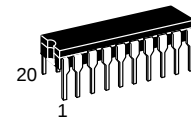
The HCT244A is the noninverting version of the HCT240. See also HCT241.

- Output Drive Capability: 15 LSTTL Loads
- TTL NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 112 FETs or 28 Equivalent Gates

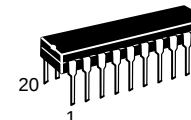
LOGIC DIAGRAM



## MC54/74HCT244A



**J SUFFIX**  
CERAMIC PACKAGE  
CASE 732-03



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 738-03



**DW SUFFIX**  
SOIC PACKAGE  
CASE 751D-04



**SD SUFFIX**  
SSOP PACKAGE  
CASE 940C-03



**DT SUFFIX**  
TSSOP PACKAGE  
CASE 948E-02

### ORDERING INFORMATION

|               |         |
|---------------|---------|
| MC54HCTXXXAJ  | Ceramic |
| MC74HCTXXXAN  | Plastic |
| MC74HCTXXXADW | SOIC    |
| MC74HCTXXXASD | SSOP    |
| MC74HCTXXXADT | TSSOP   |

### PIN ASSIGNMENT

|          |    |    |          |
|----------|----|----|----------|
| ENABLE A | 1  | 20 | VCC      |
| A1       | 2  | 19 | ENABLE B |
| YB4      | 3  | 18 | YA1      |
| A2       | 4  | 17 | B4       |
| YB3      | 5  | 16 | YA2      |
| A3       | 6  | 15 | B3       |
| YB2      | 7  | 14 | YA3      |
| A4       | 8  | 13 | B2       |
| YB1      | 9  | 12 | YA4      |
| GND      | 10 | 11 | B1       |

### FUNCTION TABLE

| Inputs                |      | Outputs |
|-----------------------|------|---------|
| Enable A,<br>Enable B | A, B | YA, YB  |
| L                     | L    | L       |
| L                     | H    | H       |
| H                     | X    | Z       |

Z = high impedance  
X = don't care



## MAXIMUM RATINGS\*

| Symbol    | Parameter                                                                                                      | Value                   | Unit |
|-----------|----------------------------------------------------------------------------------------------------------------|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                                                          | – 0.5 to + 7            | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                                                           | – 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                                                          | – 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin                                                                                      | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin                                                                                     | $\pm 35$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                                                       | $\pm 75$                | mA   |
| $P_D$     | Power Dissipation in Still Air, Plastic or Ceramic DIP†<br>SOIC Package†<br>SSOP or TSSOP Package†             | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature                                                                                            | – 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, SOIC, SSOP or TSSOP Package)<br>(Ceramic DIP) | 260<br>300              | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C  
Ceramic DIP: – 10 mW/°C from 100° to 125°C  
SOIC Package: – 7 mW/°C from 65° to 125°C  
SSOP or TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter                                            | Min  | Max      | Unit |
|-------------------|------------------------------------------------------|------|----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 4.5  | 5.5      | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | $V_{CC}$ | V    |
| $T_A$             | Operating Temperature, All Package Types             | – 55 | + 125    | °C   |
| $t_r, t_f$        | Input Rise and Fall Time (Figure 1)                  | 0    | 500      | ns   |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol   | Parameter                         | Test Conditions                                                                         | $V_{CC}$<br>V | Guaranteed Limit |            |            | Unit          |
|----------|-----------------------------------|-----------------------------------------------------------------------------------------|---------------|------------------|------------|------------|---------------|
|          |                                   |                                                                                         |               | – 55 to<br>25°C  | ≤ 85°C     | ≤ 125°C    |               |
| $V_{IH}$ | Minimum High-Level Input Voltage  | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$ | 4.5<br>5.5    | 2<br>2           | 2<br>2     | 2<br>2     | V             |
| $V_{IL}$ | Maximum Low-Level Input Voltage   | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$ | 4.5<br>5.5    | 0.8<br>0.8       | 0.8<br>0.8 | 0.8<br>0.8 | V             |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$                 | 4.5<br>5.5    | 4.4<br>5.4       | 4.4<br>5.4 | 4.4<br>5.4 | V             |
|          |                                   | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 6 \text{ mA}$                   | 4.5           | 3.98             | 3.84       | 3.7        |               |
| $V_{OL}$ | Maximum Low-Level Output Voltage  | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$                 | 4.5<br>5.5    | 0.1<br>0.1       | 0.1<br>0.1 | 0.1<br>0.1 | V             |
|          |                                   | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \leq 6 \text{ mA}$                   | 4.5           | 0.26             | 0.33       | 0.4        |               |
| $I_{in}$ | Maximum Input Leakage Current     | $V_{in} = V_{CC} \text{ or } GND$                                                       | 5.5           | $\pm 0.1$        | $\pm 1.0$  | $\pm 1.0$  | $\mu\text{A}$ |

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol           | Parameter                                      | Test Conditions                                                                                                                     | V <sub>CC</sub><br>V | Guaranteed Limit |               |         | Unit |
|------------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------|---------------|---------|------|
|                  |                                                |                                                                                                                                     |                      | – 55 to 25°C     | ≤ 85°C        | ≤ 125°C |      |
| I <sub>OZ</sub>  | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND | 5.5                  | ± 0.5            | ± 5.0         | ± 10    | μA   |
| I <sub>CC</sub>  | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                                                                 | 5.5                  | 4                | 40            | 160     | μA   |
| ΔI <sub>CC</sub> | Additional Quiescent Supply Current            | V <sub>in</sub> = 2.4 V, Any One Input<br>V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs<br>I <sub>out</sub> = 0 μA         | 5.5                  | ≥ –55°C          | 25°C to 125°C |         | mA   |
|                  |                                                |                                                                                                                                     |                      | 2.9              | 2.4           |         |      |

**NOTES:**

- Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

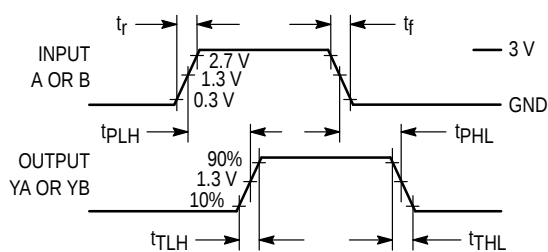
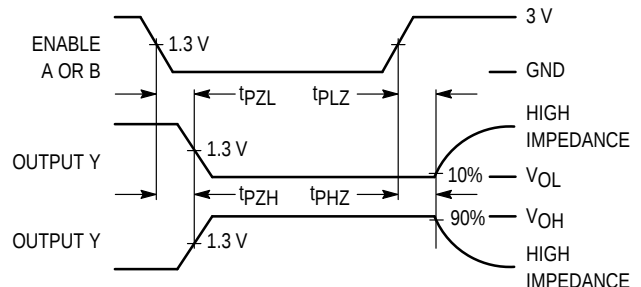
**AC ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 5.0 V ± 10%, C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter                                                                 | Guaranteed Limit |        |         | Unit |
|----------------------------------------|---------------------------------------------------------------------------|------------------|--------|---------|------|
|                                        |                                                                           | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, A to YA or B to YB<br>(Figures 1 and 3)        | 20               | 25     | 30      | ns   |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to YA or YB<br>(Figures 2 and 4) | 26               | 33     | 39      | ns   |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to YA or YB<br>(Figures 2 and 4) | 22               | 28     | 33      | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 3)           | 12               | 15     | 18      | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance                                                 | 10               | 10     | 10      | pF   |
| C <sub>out</sub>                       | Maximum Three-State Output Capacitance (Output in High-Impedance State)   | 15               | 15     | 15      | pF   |

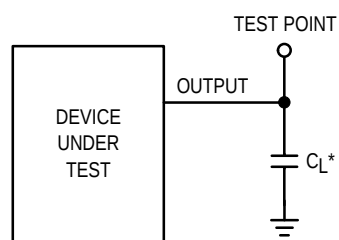
NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|-----------------|-----------------------------------------------------|-----------------------------------------|----|
|                 |                                                     | 55                                      |    |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

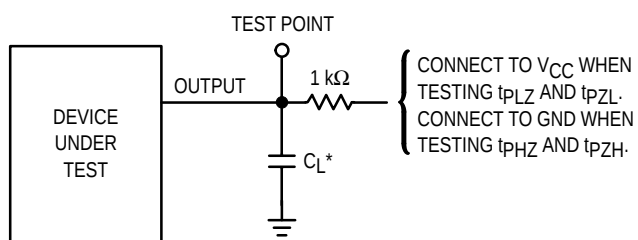
**SWITCHING WAVEFORMS****Figure 1.****Figure 2.**

## TEST CIRCUITS



\* Includes all probe and jig capacitance

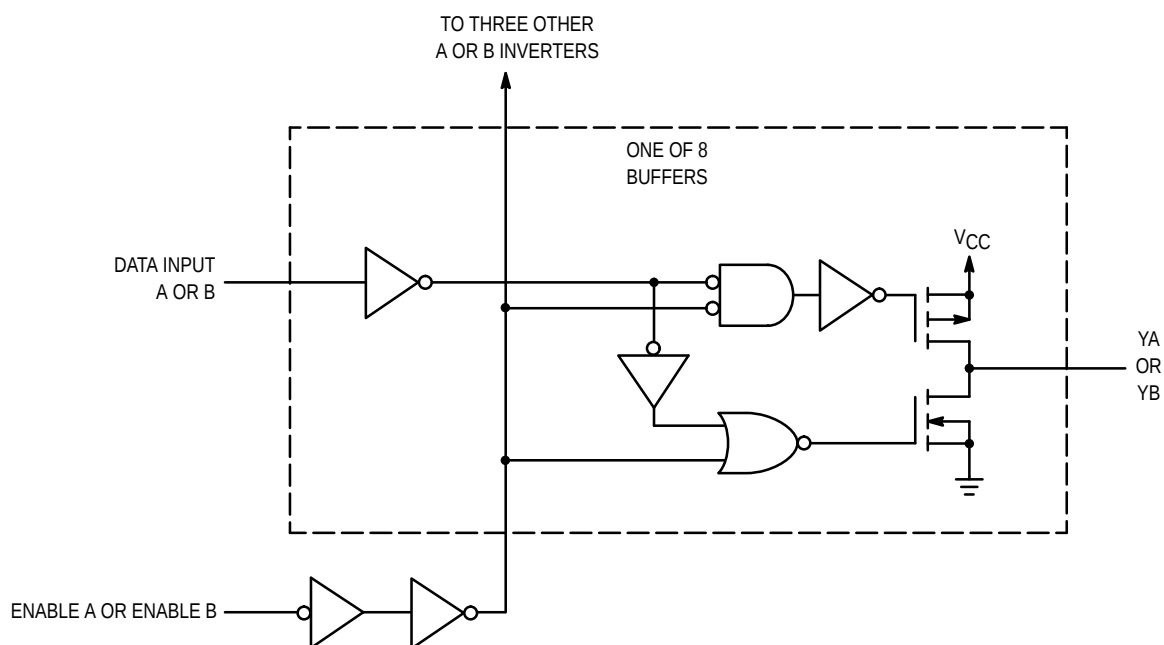
Figure 3.



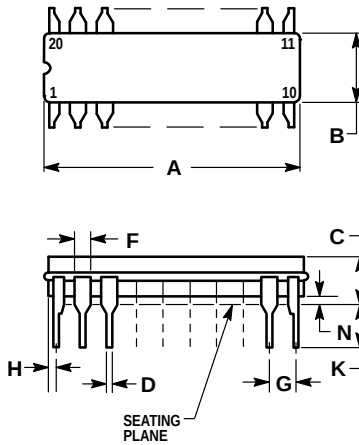
\* Includes all probe and jig capacitance

Figure 4.

## LOGIC DETAIL



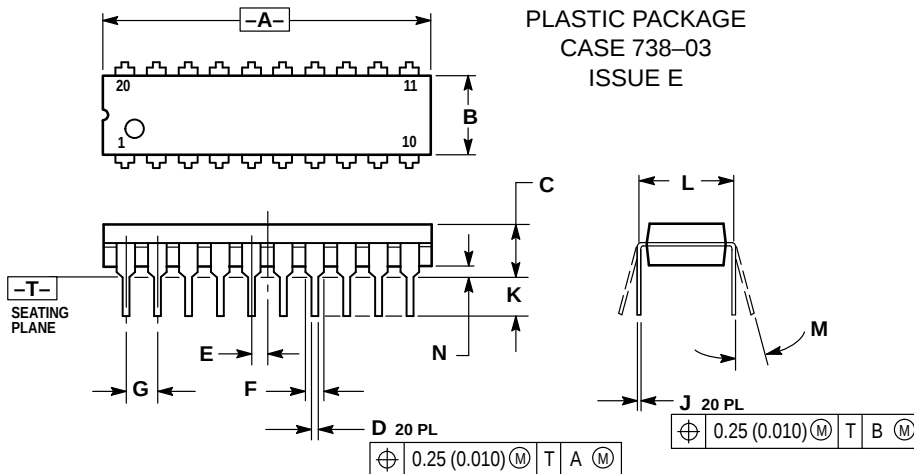
## OUTLINE DIMENSIONS

**J SUFFIX**  
 CERAMIC PACKAGE  
 CASE 732-03  
 ISSUE E


## NOTES:

- LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSIONS A AND B INCLUDE MENISCUS.

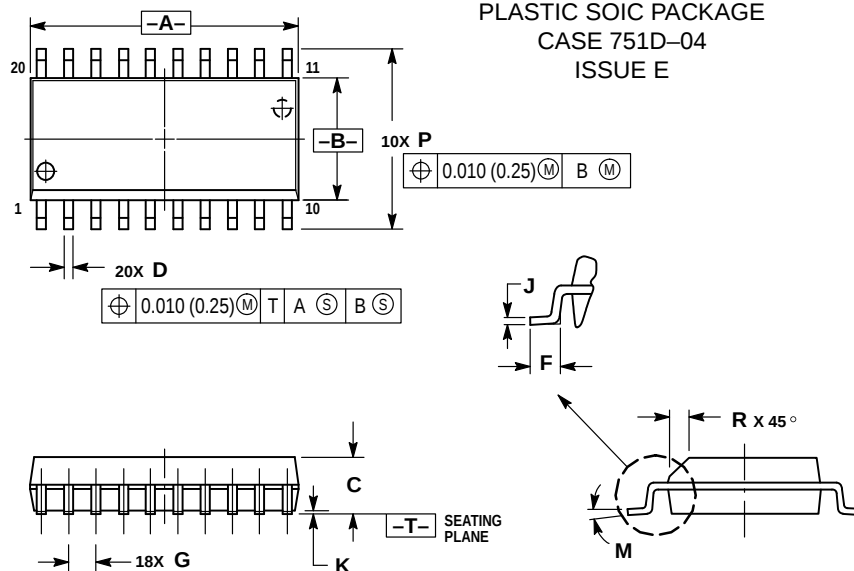
| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 23.88       | 25.15 | 0.940     | 0.990 |
| B   | 6.60        | 7.49  | 0.260     | 0.295 |
| C   | 3.81        | 5.08  | 0.150     | 0.200 |
| D   | 0.38        | 0.56  | 0.015     | 0.022 |
| F   | 1.40        | 1.65  | 0.055     | 0.065 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| H   | 0.51        | 1.27  | 0.020     | 0.050 |
| J   | 0.20        | 0.30  | 0.008     | 0.012 |
| K   | 3.18        | 4.06  | 0.125     | 0.160 |
| L   | 7.62 BSC    |       | 0.300 BSC |       |
| M   | 0°          | 15°   | 0°        | 15°   |
| N   | 0.25        | 1.02  | 0.010     | 0.040 |

**N SUFFIX**  
 PLASTIC PACKAGE  
 CASE 738-03  
 ISSUE E


## NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 1.010     | 1.070 | 25.66       | 27.17 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.150     | 0.180 | 3.81        | 4.57  |
| D   | 0.015     | 0.022 | 0.39        | 0.55  |
| E   | 0.050 BSC |       | 1.27 BSC    |       |
| F   | 0.050     | 0.070 | 1.27        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.140 | 2.80        | 3.55  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 15°   | 0°          | 15°   |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |

**DW SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751D-04  
 ISSUE E


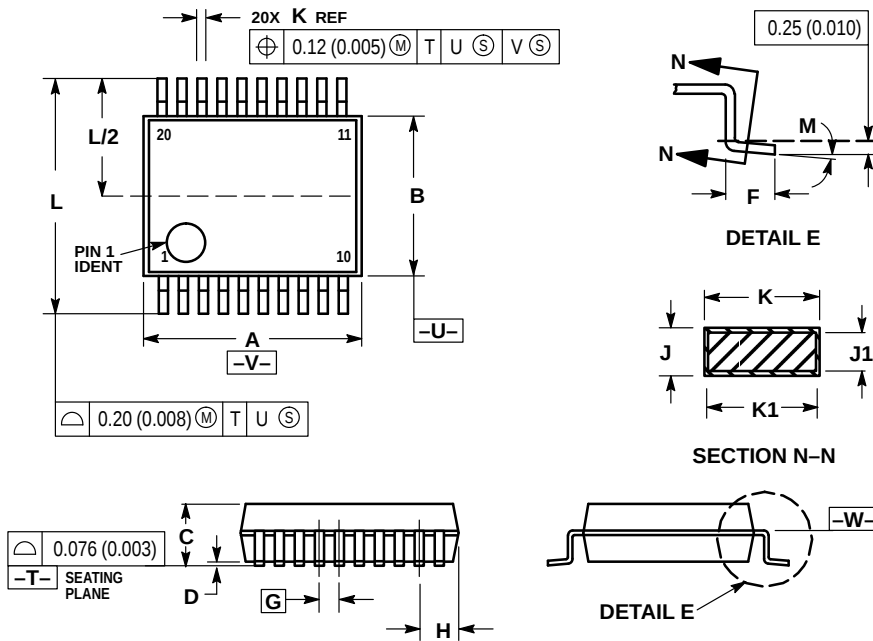
## NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 12.65       | 12.95 | 0.499     | 0.510 |
| B   | 7.40        | 7.60  | 0.292     | 0.299 |
| C   | 2.35        | 2.65  | 0.093     | 0.104 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.50        | 0.90  | 0.020     | 0.035 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.25        | 0.32  | 0.010     | 0.012 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 10.05       | 10.55 | 0.395     | 0.415 |
| R   | 0.25        | 0.75  | 0.010     | 0.029 |

## OUTLINE DIMENSIONS

**SD SUFFIX**  
**PLASTIC SSOP PACKAGE**  
**CASE 940C-03**  
**ISSUE B**

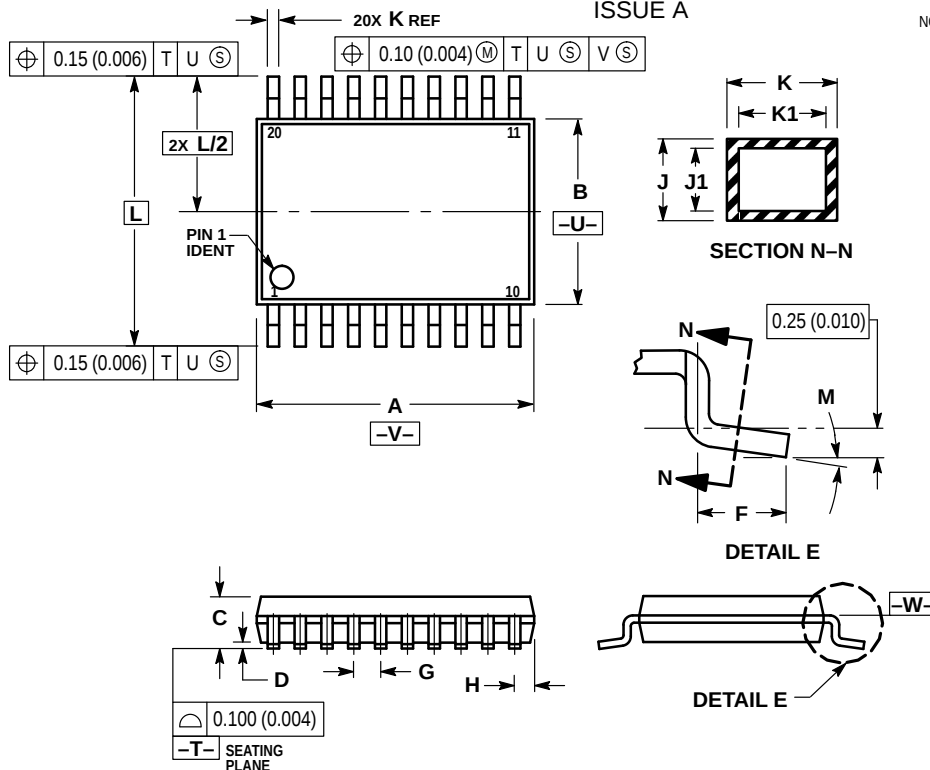


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 7.07        | 7.33 | 0.278     | 0.288 |
| B   | 5.20        | 5.38 | 0.205     | 0.212 |
| C   | 1.73        | 1.99 | 0.068     | 0.078 |
| D   | 0.05        | 0.21 | 0.002     | 0.008 |
| F   | 0.63        | 0.95 | 0.024     | 0.037 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.59        | 0.75 | 0.023     | 0.030 |
| J   | 0.09        | 0.20 | 0.003     | 0.008 |
| J1  | 0.09        | 0.16 | 0.003     | 0.006 |
| K   | 0.25        | 0.38 | 0.010     | 0.015 |
| K1  | 0.25        | 0.33 | 0.010     | 0.013 |
| L   | 7.65        | 7.90 | 0.301     | 0.311 |
| M   | 0°          | 8°   | 0°        | 8°    |

**DT SUFFIX**  
**PLASTIC TSSOP PACKAGE**  
**CASE 948E-02**  
**ISSUE A**



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 6.40        | 6.60 | 0.252     | 0.260 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | —           | 1.20 | —         | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.27        | 0.37 | 0.011     | 0.015 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

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