

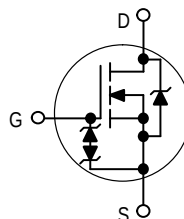
Advance Information

TMOS E-FET™

Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate

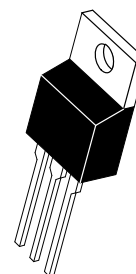
This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor—Absorbs High Energy in the Avalanche Mode
- ESD Protected. Designed to Typically Withstand 400 V Machine Model and 4000 V Human Body Model.



MTP55N06Z

TMOS POWER FET
55 AMPERES
60 VOLTS
 $R_{DS(on)} = 18 \text{ m}\Omega$



CASE 221A-06, Style 5
TO-220AB

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-to-Source Voltage — Continuous	V_{GS}	± 20	Vdc
— Non-Repetitive ($t_p \leq 10 \text{ ms}$)	V_{GSM}	± 40	Vpk
Drain Current — Continuous @ $T_C = 25^\circ\text{C}$	I_D	55	Adc
— Continuous @ $T_C = 100^\circ\text{C}$	I_D	35.5	
— Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	165	Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	113	Watts
Derate above 25°C		0.91	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25 \text{ Vdc}$, $V_{DS} = 60 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, Peak $I_L = 55 \text{ Apk}$, $L = 0.3 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	454	mJ
Thermal Resistance — Junction-to-Case	$R_{\theta JC}$	1.1	$^\circ\text{C/W}$
— Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

This document contains information on a new product. Specifications and information herein are subject to change without notice.
E-FET is a trademark of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.



MTP55N06Z

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 250\text{ }\mu\text{Adc}$) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	60 —	— 53	— —	Vdc mV/°C	
Zero Gate Voltage Drain Current ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	— —	— —	1.0 10	μAdc	
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	100	nAdc	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{Adc}$) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 —	3.0 6.0	4.0 —	Vdc mV/°C	
Static Drain-to-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 27.5\text{ Adc}$)	$R_{DS(on)}$	—	14	16	m Ω	
Drain-to-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$) ($I_D = 55\text{ Adc}$) ($I_D = 27.5\text{ Adc}$, $T_J = 125^\circ\text{C}$)	$V_{DS(on)}$	— —	0.825 0.74	1.2 1.0	Vdc	
Forward Transconductance ($V_{DS} = 4.0\text{ Vdc}$, $I_D = 27.5\text{ Adc}$)	g_{FS}	12	15	—	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	$(V_{DS} = 25\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{iss}	—	1390	pF	
Output Capacitance		C_{oss}	—	520		
Transfer Capacitance		C_{rss}	—	119		
SWITCHING CHARACTERISTICS (2)						
Turn-On Delay Time	$(V_{DD} = 30\text{ Vdc}$, $I_D = 55\text{ Adc}$, $V_{GS(on)} = 10\text{ Vdc}$, $R_G = 9.1\text{ }\Omega$)	$t_{d(on)}$	—	27	ns	
Rise Time		t_r	—	157		
Turn-Off Delay Time		$t_{d(off)}$	—	116		
Fall Time		t_f	—	126		
Gate Charge (See Figure 8)	$(V_{DS} = 48\text{ Vdc}$, $I_D = 55\text{ Adc}$, $V_{GS} = 10\text{ Vdc}$)	Q_T	—	40	nC	
		Q_1	—	7.0		
		Q_2	—	18		
		Q_3	—	15		
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	$(I_S = 55\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$) $(I_S = 55\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	V_{SD}	— —	0.93 0.82	1.1 —	Vdc
Reverse Recovery Time	$(I_S = 55\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$)	t_{rr}	—	57	ns	
		t_a	—	32		
		t_b	—	25		
Reverse Recovery Stored Charge		Q_{RR}	—	0.11	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from drain lead 0.25" from package to center of die)	L_D	— —	3.5 4.5	— —	nH	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L_S	—	7.5	—		

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

(2) Switching characteristics are independent of operating junction temperature.

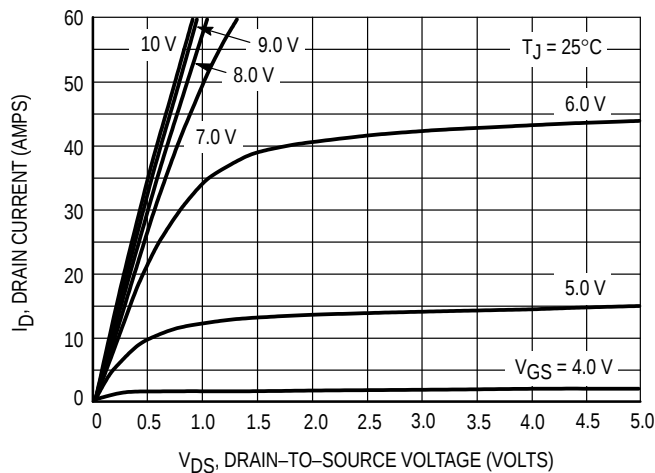


Figure 1. On-Region Characteristics

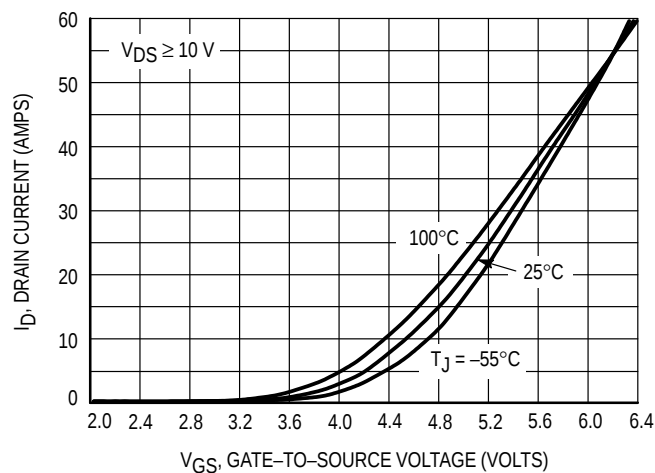


Figure 2. Transfer Characteristics

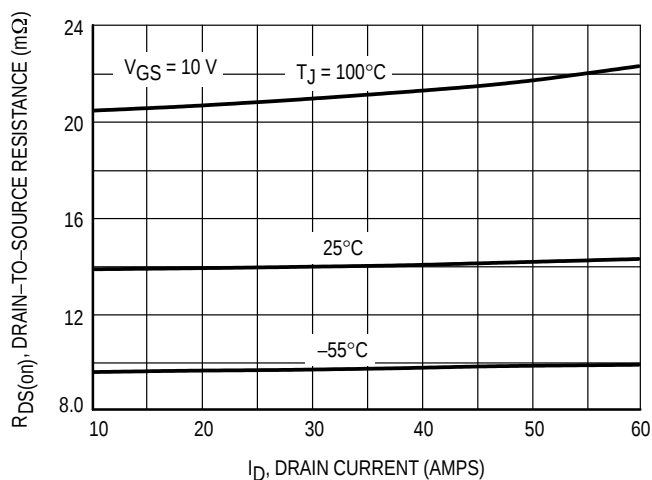


Figure 3. On-Resistance versus Drain Current and Temperature

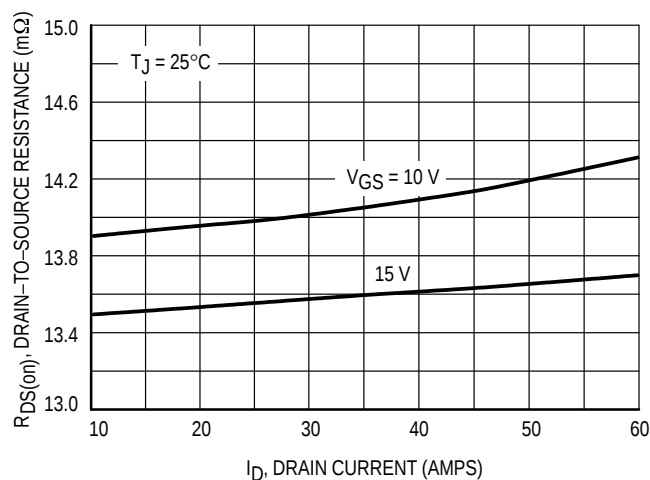


Figure 4. On-Resistance versus Drain Current and Gate Voltage

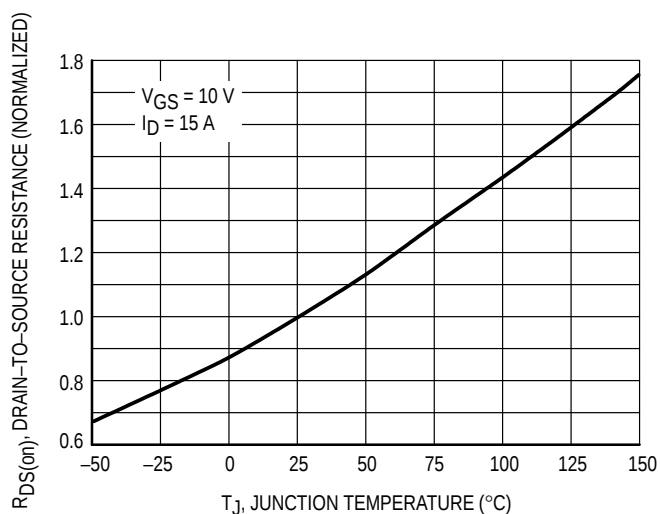


Figure 5. On-Resistance Variation with Temperature

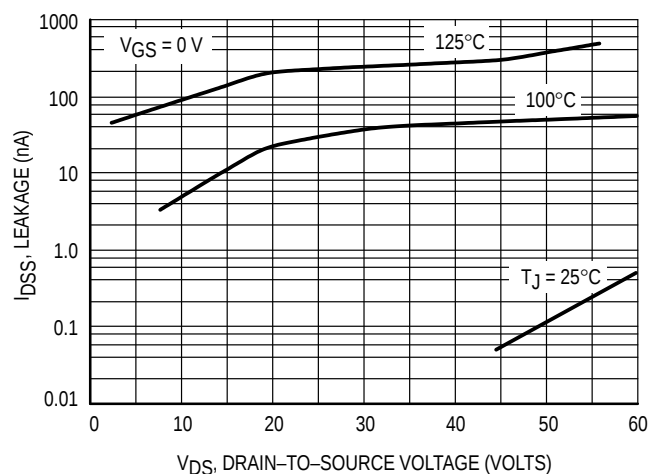


Figure 6. Drain-to-Source Leakage Current versus Voltage

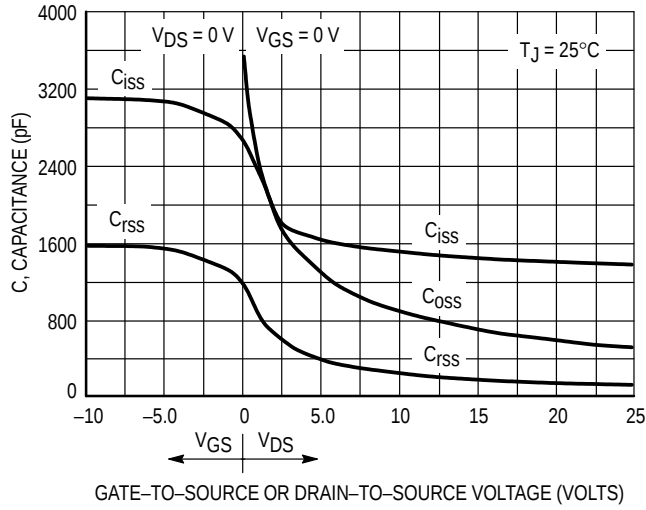


Figure 7. Capacitance Variation

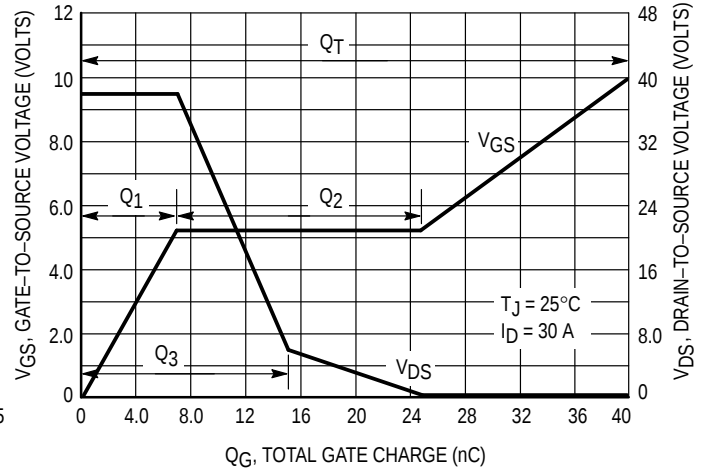


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

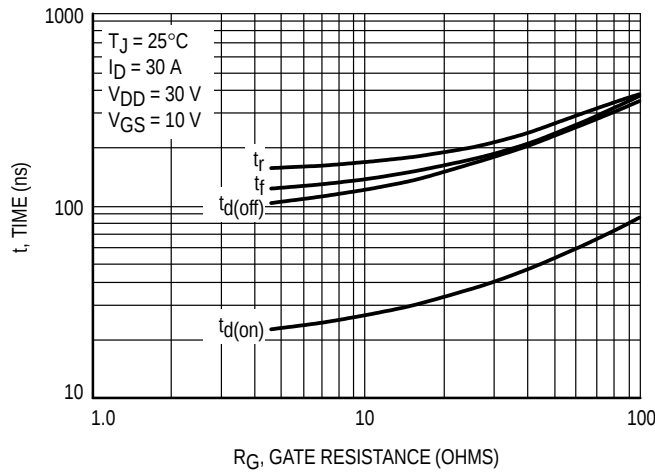


Figure 9. Resistive Switching Time Variation versus Gate Resistance

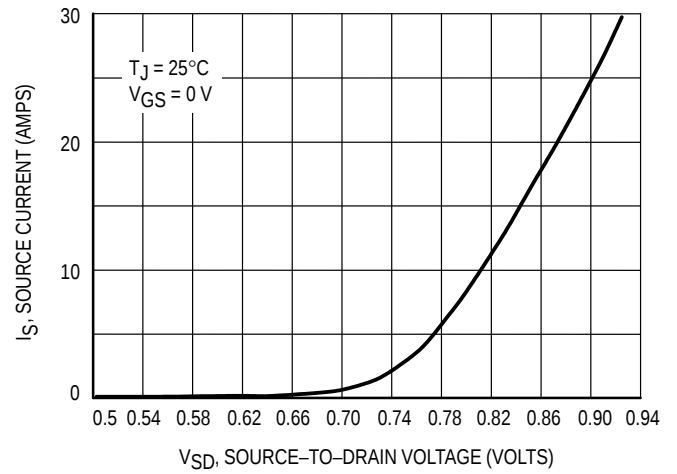


Figure 10. Diode Forward Voltage versus Current

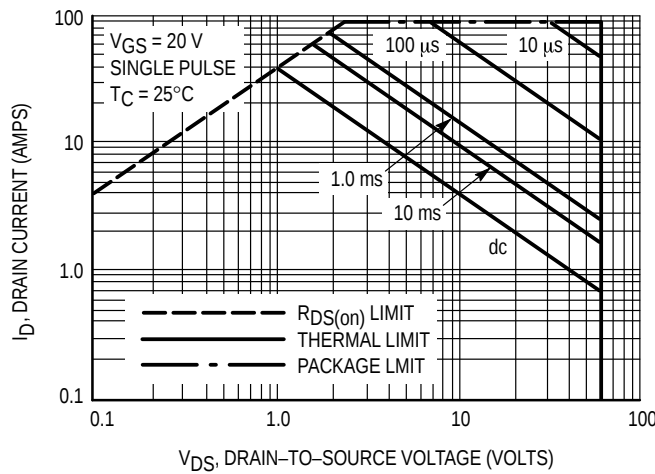


Figure 11. Maximum Rated Forward Biased Safe Operating Area

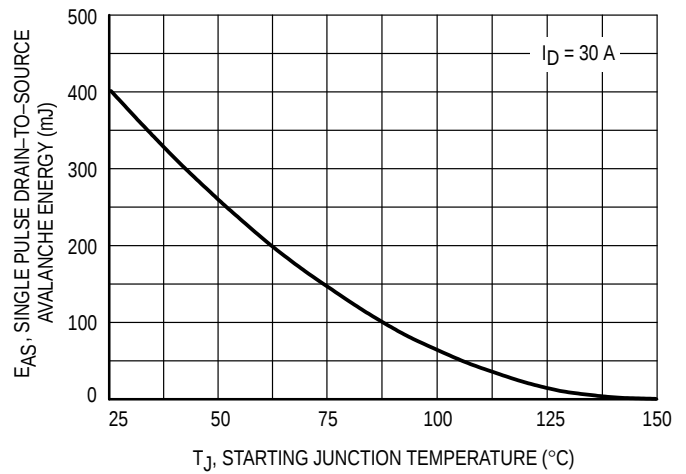


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

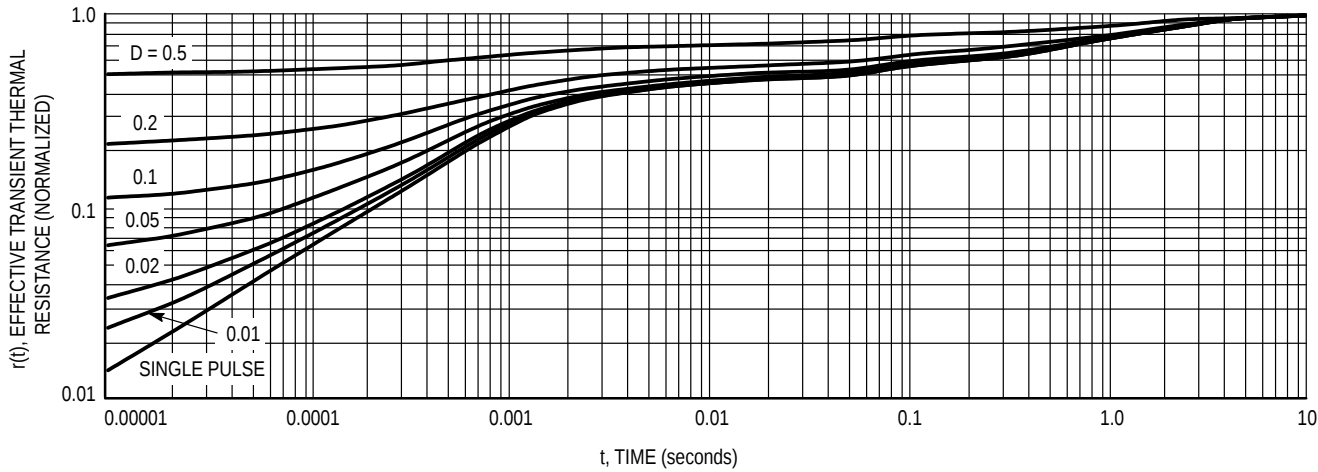
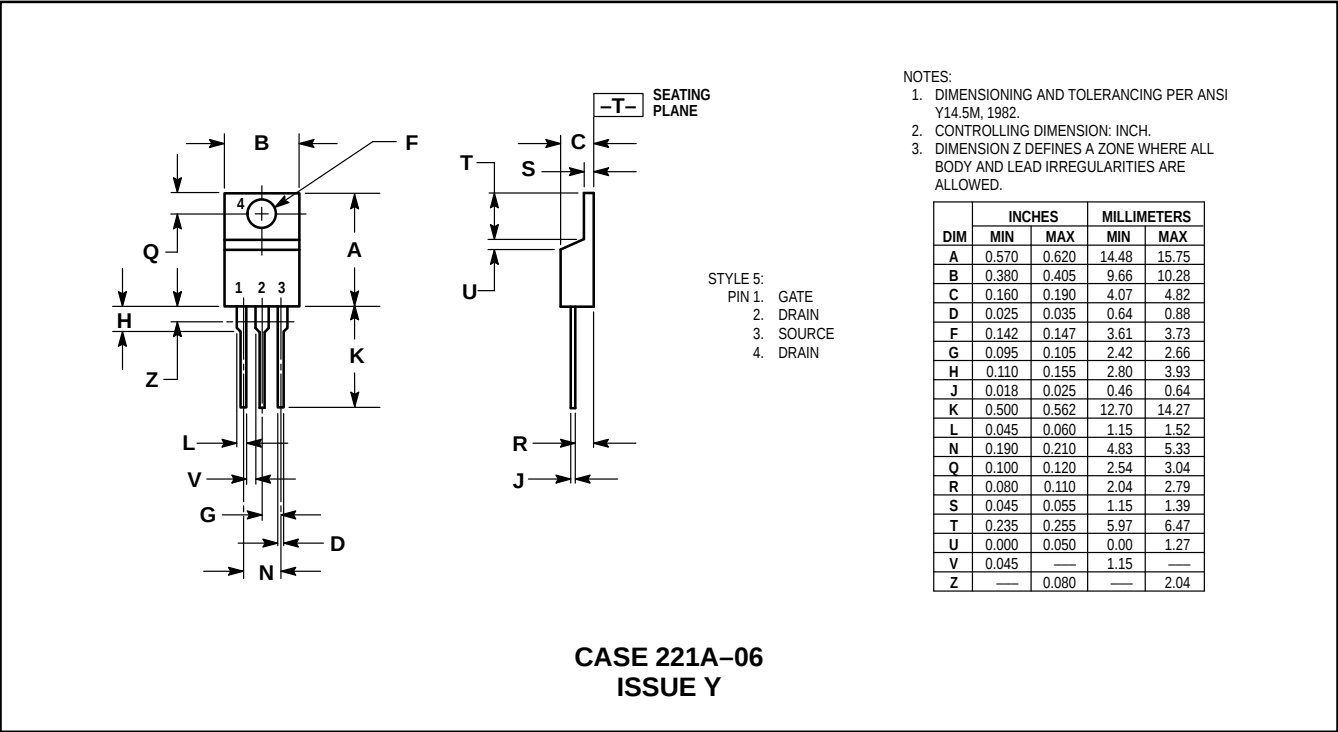


Figure 13. Thermal Response

PACKAGE DIMENSIONS



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