

MNDS90LV032A-X REV 0D0

 Original Creation Date: 2/21/00
 Last Update Date: 11/10/03
 Last Major Revision Date: 2/21/00

Low Voltage LVDS Quad CMOS Differential Line Receiver

General Description

The DS90LV032A is a quad differential line receiver designed for applications requiring low power dissipation and high data rates.

The DS90LV032A accepts low voltage differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE function that may be used to multiplex outputs.

The DS90LV032A and companion LVDS line driver (DS90LV031A) provide a new alternative to high power pseudo-ECL devices for high speed point to point interface applications.

In addition, the DS90LV032A provides power-off high impedance LVDS inputs. This feature assures minimal loading effect on the LVDS bus lines when VCC is not present.

Industry Part Number

DS90LV032A

Prime Die

DS90LV032A

NS Part Numbers

 DS90LV032AW-MLS
 DS90LV032AW-QML
 DS90LV032AWGMLS
 DS90LV032AWGQML

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+85
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+85
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+85
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+85
11	Switching tests at	-55

Features

- High impedance LVDS inputs with power-off
- Accepts small swing (330 mV) differential signal levels.
- Low power dissipation.
- Low differential skew.
- Low chip to chip skew
- +85C thru -55C operating temperature range
- Pin compatible with DS90C032A and DS26C32A.
- Compatible with ANSI/TIA/EIA-644
- Typical Rise/Fall time is 350 ps

CONTROLLING DOCUMENT:

DS90LV032AW-QML	5962-9865201QFA
DS90LV032AWGQML	5962-9865201QXA

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vcc)	-0.3 to +4V
Input Voltage (RIN+, RIN-)	-0.3 to 3.9V
Enable Input Voltage (EN, EN*)	-0.3 to (Vcc+0.3V)
Output Voltage (ROUT)	-0.3 to (Vcc+0.3V)
Storage Temperature Range (Tstg)	-65C to + 150C
Lead Temperature Soldering 4 seconds	260 C
Maximum Package Power Dissipation @ +25C (Note 2)	
16 PIN CERPAK (W Pkg)	845mW
16 PIN CERAMIC SOIC (WG Pkg)	845mW
Thermal Resistance. (Theta JA)	
16 PIN CERPAK (W Pkg)	148 C/W
16 PIN CERAMIC SOIC (WG Pkg)	148 C/W
Thermal Resistance. (Theta JC)	
16 PIN CERPAK (W Pkg)	21 C/W
16 PIN CERAMIC SOIC (WG Pkg)	21 C/W
ESD Rating.	4500 Volts.
Maximum Junction Temperature	+150C

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Derate (W & WG Pkgs) @ 6.8 mW/C above +25C.

Recommended Operating Conditions

Operating Voltage (Vcc)	3.15V to 3.45V
Operating Temperature Range (Ta)	-55C to +85C
Receiver Input Voltage	GND to 3.0V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: Over supply voltage range of 3.15V to 3.45V and operating temperature of -55C to +85C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VTL	Differential Input Low Threshold	V _{cm} = +1.2V	1	RIN+, RIN-	-100		mV	1, 2, 3
VTH	Differential Input High Threshold	V _{cm} = +1.2V	1	RIN+, RIN-		100	mV	1, 2, 3
VCMR	Common Mode Voltage Range	VID = 200mV peak to peak	1, 4	RIN+, RIN-	0.1	2.3	V	1, 2, 3
IIN	Input Current	V _{cc} = 3.45V or 0V, V _{in} = 2.8V or 0V		RIN+, RIN-		±10	uA	1, 2, 3
		V _{cc} = 0V, V _{in} = 3.45V		RIN+, RIN-		±20	uA	1, 2, 3
VOH	Output High Voltage	I _{oh} = -0.4 mA, V _{id} = 200mV		ROUT	2.7		V	1, 2, 3
		I _{oh} = -0.4 mA, Inputs Open		ROUT	2.7		V	1, 2, 3
VOL	Output Low Voltage	I _{ol} = 2 mA, V _{id} = -200mV		ROUT		0.25	V	1, 2, 3
IOS	Output Short Circuit Current	Enabled, V _{out} = 0V	5	ROUT	-15	-120	mA	1, 2, 3
IOZ	Output TRI-STATE Current	Disabled, V _{out} = 0V or V _{cc}		ROUT		±10	uA	1, 2, 3
VIH	Input High Voltage		6	EN, EN*	2.0	V _{cc}	V	1, 2, 3
VIL	Input Low Voltage		6	EN, EN*	GND	0.8	V	1, 2, 3
II	Input Current	V _{in} = V _{cc} or 0V, Other Input = V _{cc} or GND		EN, EN*		±10	uA	1, 2, 3
VCL	Input Clamp Voltage	I _{cl} = -18mA		EN, EN*		-1.5	V	1, 2, 3
Icc	No Load Supply Current Receivers Enabled	EN, EN* = V _{cc} or GND, Inputs Open		V _{cc}		15	mA	1, 2, 3
		EN, EN* = 2.4 or 0.5, Inputs Open		V _{cc}		15	mA	1, 2, 3
IccZ	No Load Supply Current Receivers Disabled	EN = GND, EN* = V _{cc} , Inputs Open		V _{cc}		5	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: VCC = 3.15/3.30/3.45V, CL = 20pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPHLD	Differential Propagation Delay High to Low	Vid = 200mV, Input pulse = 1.1V to 1.3V, Vin = 1.2V (0 differential) to Vout = 1/2 Vcc			0.5	3.5	ns	9, 10, 11
tPLHD	Differential Propagation Delay Low to High	Vid = 200mV, Input pulse = 1.1V to 1.3V, Vin = 1.2V (0V differential) to Vout = 1/2 Vcc			0.5	3.5	ns	9, 10, 11
tSKD	Differential Skew tPHLD-tPLHD	CL = 20pF, Vid = 200mV				1.5	ns	9, 10, 11
tSK1	Channel to Channel Skew	CL = 20pF, Vid = 200mV	2			1.75	ns	9, 10, 11
tSK2	Chip to Chip Skew	CL = 20pF, Vid = 200mV	3			3.0	ns	9, 10, 11
tPLZ	Disable Time Low to Z	Input pulse = 0V to 3.0V, Vin = 1.5V, Vout = Vol+0.5V, RL = 1K Ohm.				12	ns	9, 10, 11
tPHZ	Disable Time High to Z	Input pulse = 0V to 3.0V, Vin = 1.5V, Vout = Voh-0.5V, RL = 1K Ohm.				12	ns	9, 10, 11
tPZH	Enable Time Z to High	Input pulse = 0V to 3.0V, Vin = 1.5V, Vout = 50%, RL = 1K Ohm.				20	ns	9, 10, 11
tPZL	Enable Time Z to Low	Input pulse = 0V to 3.0V, Vin = 1.5V, Vout = 50%, RL = 1K Ohm.				20	ns	9, 10, 11

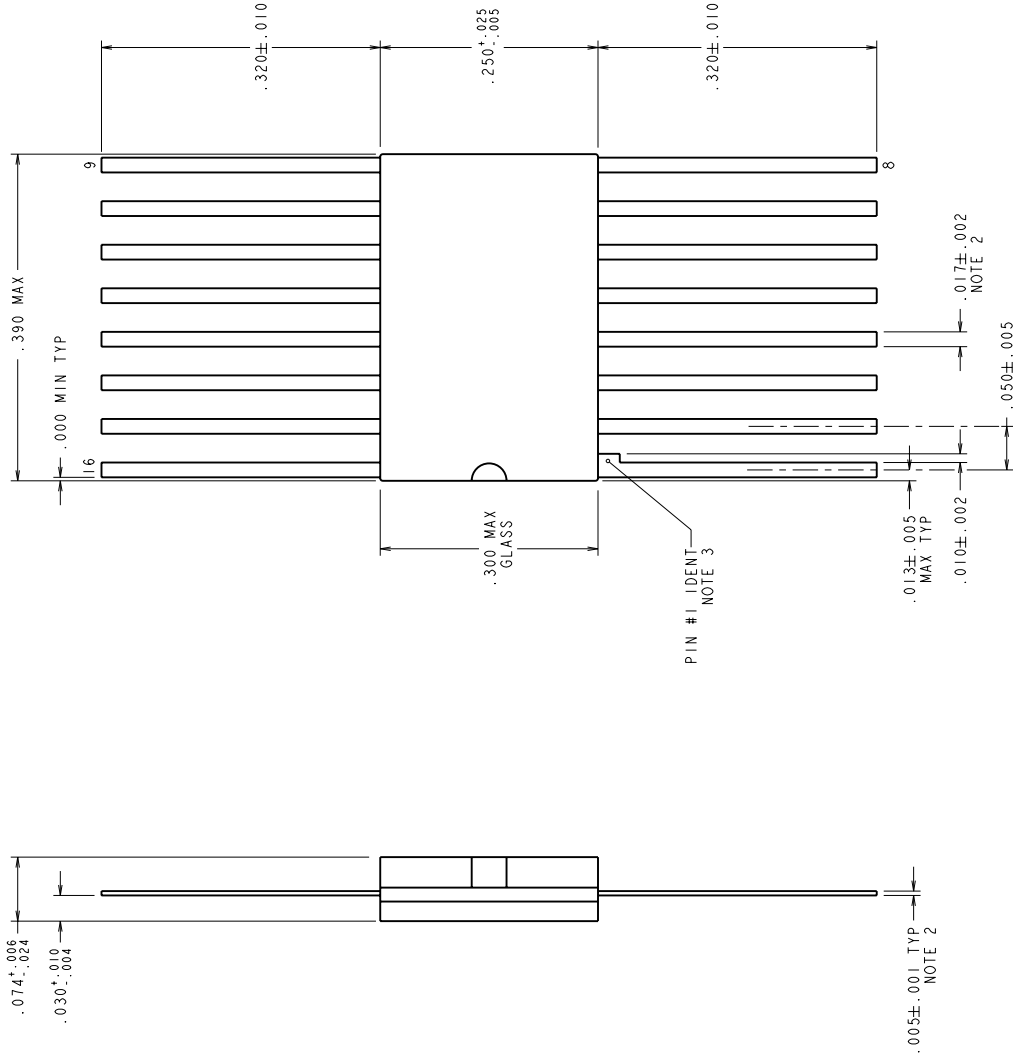
- Note 1: Tested during VOH/VOL tests by applying appropriate voltage levels to the input pins of the device under test.
- Note 2: Channel to Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
- Note 3: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
- Note 4: The VCMR range is reduced for larger input differential voltage (VID). Example: If VID = 400mV, the VCMR is 0.2V to 2.2V. A VID up to Vcc- 0V may be applied to the Rin+/Rin- inputs with the Common-Mode voltage set to Vcc/2.
- Note 5: Output short circuit current (Ios) is specified as magnitude only, minus sign indicates direction of current. Only one output should be shorted at a time, do not exceed maximum junction temperature.
- Note 6: Tested during IOZ tests by applying appropriate threshold voltage levels to the EN and EN* pins.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
W16ARL	CERPACK (W), 16 LEAD (P/P DWG)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94
L	.017±.002 WAS .017±.020.	10656	10/21/94
			DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
 - a) A NOTCH OR OTHER MARK WITHIN THIS AREA
 - b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION M0-092, VARIATION AC, DATED 04/89.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS		DATE	
DRN	<i>D.F. Grady</i>	07/28/94	
DFTG. CHK.			
ENGR. CHK.			
PROJECTION			
SCALE	N/A	SIZE	C
DRAWING NUMBER	MKT-W16A		
REV	L		
DO NOT SCALE DRAWING		SHEET 1 of 1	

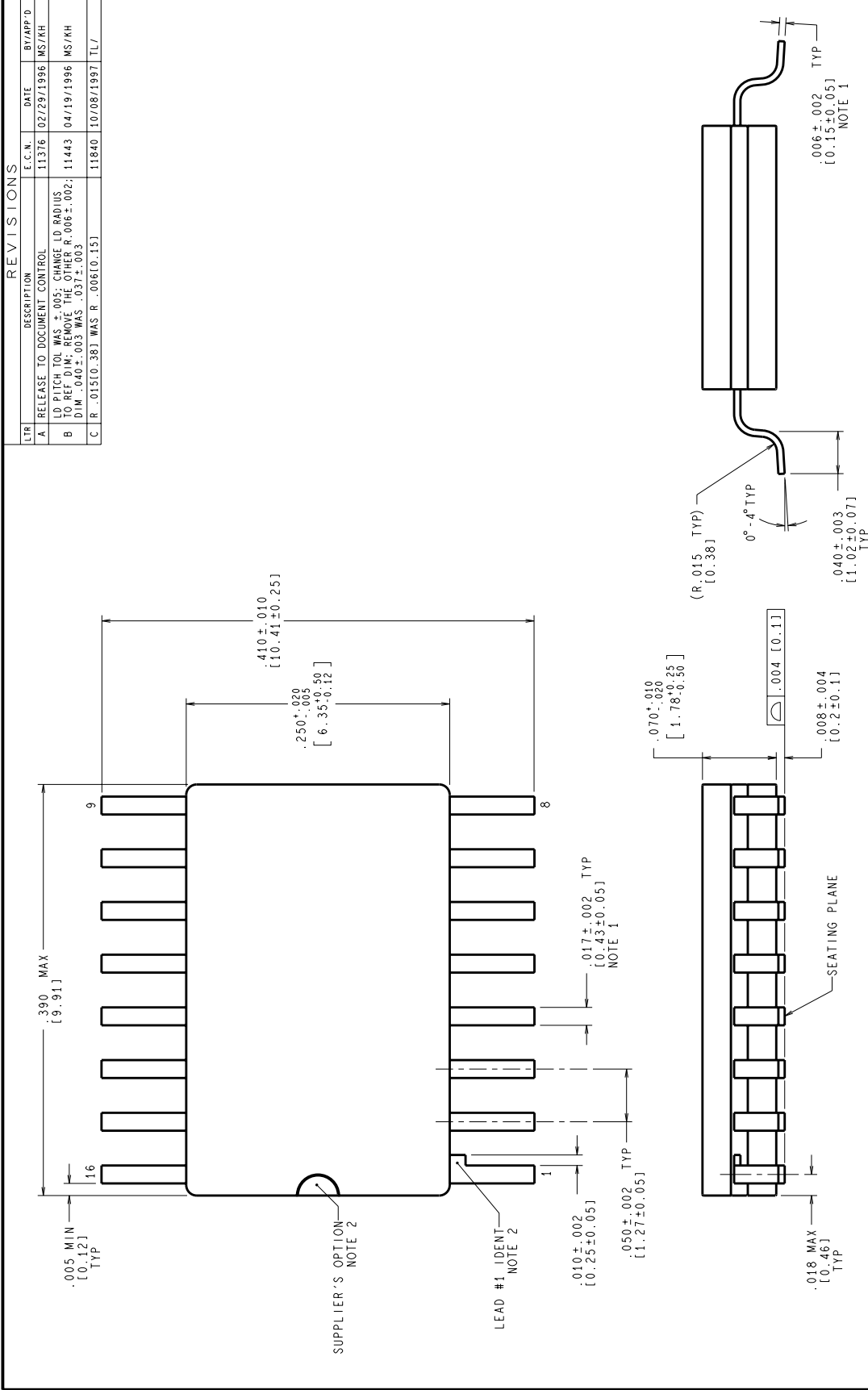
	<i>National Semiconductor</i>
2900 Semiconductor dr., Santa Clara, CA 95052-8090	

CERPACK, 16 LEAD

National Semiconductor
2000 Semiconductor dr., Santa Clara, CA 95052-8090

CERPACK, I6 LEAD

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996
B	LD PITCH TOL WAS $\pm .005$; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R .006 $\pm .002$; DIM .040 $\pm .003$ WAS .037 $\pm .003$	11443	04/19/1996
C	R .015(0.38) WAS R .006(0.15)	11840	10/08/1997



NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASE METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
- NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

MIL-PRF-38535 CONFIGURATION CONTROL

APPROVALS	DATE	SCALE	SIZE	DRAWING NUMBER	REV
DESIGN MARTY SUCHY	02/29/96	N/A	C	(SC)MKT-WG16A	C
ENGINEER CHK.					
PROJECTION					
National Semiconductor 2000 Semiconductor Dr., Santa Clara, CA 95052-8000 CERPACK, 16 LEAD, GULL WING					
DO NOT SCALE DRAWING					
SHEET 1 of 1					

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003631	08/16/02	Mike Fitzgerald	Initial MDS Release
0B0	M0004035	08/15/03	Rose Malone	Update MDS: MNDS90LV032A-X, Rev. 0A0 to MNDS90LV031A-X, Rev. 0B0. Added to Main Table NS Part Number DS90LV032AW-MLS. Moved reference to SMD number from Main Table to Features Section.
0C0	M0004184	11/10/03	Rose Malone	Update MDS: MNDS90LV032A-X, Rev. 0B0 to 0C0. MDS enhancements: Additional verbage to the general discription, Main Table and Added new bullet to the Features Section.
0D0	M0004345	11/10/03	Rose Malone	Update MDS: MNDS90LV032A-X, Rev. 0C0 to MNDS90LV032A-X, Rev. 0D0. Updated Features Section Typical Rise/Fall time.