

LM27222

High-Speed 4.5A Synchronous MOSFET Driver

General Description

The LM27222 is a dual N-channel MOSFET driver designed to drive MOSFETs in push-pull configurations as typically used in synchronous buck regulators. The LM27222 takes the PWM output from a controller and provides the proper timing and drive levels to the power stage MOSFETs. Adaptive shoot-through protection prevents damaging and efficiency reducing shoot-through currents, thus ensuring a robust design capable of using nearly any MOSFET. The adaptive shoot-through protection circuitry also reduces the dead time down to as low as 10ns ensuring the highest operating efficiency. The peak sourcing and sinking current for each driver of the LM27222 is about 3A and 4.5Amps respectively with a Vgs of 5V. System performance is also enhanced by keeping propagation delay down to 8ns. Efficiency is once again improved at all load currents by supporting synchronous, non-synchronous, and diode emulation modes through the LEN pin. The minimum output pulse width realized at the output of the MOSFETs is as low as 30ns. This enables high operating frequencies at very high conversion ratios in buck regulator designs. The LM27222 simplifies sequencing requirements by keeping gate drives low until Vin and Vcc are stable and the switching controller starts operating. To support low power states in notebook

systems, LM27222 draws only 5µA from the 5V rail when the IN and LEN inputs are low or floating.

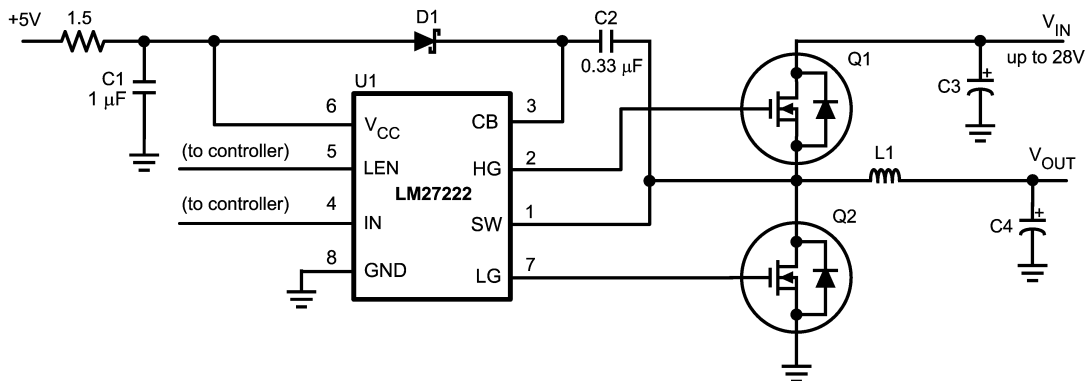
Features

- Adaptive shoot-through protection
- 10ns dead time
- 8ns propagation delay
- 30ns minimum on-time
- 0.4Ω pull-down and 0.9Ω pull-up drivers
- 4.5A peak driving current
- MOSFET tolerant design
- 5µA quiescent current
- 28V input voltage in buck configuration
- SO-8 and LLP packages

Applications

- High Current DC/DC Power Supplies
- High Input Voltage Switching Regulators
- Fast Transient DC/DC Power Supplies
- Single ended forward output rectification
- Notebook Computer core regulators

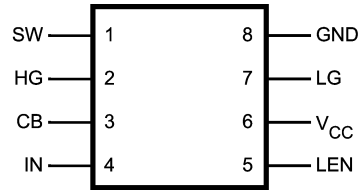
Typical Application



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FIGURE 1.

Connection Diagram



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Top View
SO-8 (NS Package # M08A) $\theta_{JA} = 172^{\circ}\text{C/W}$
or
LLP-8 (NS Package # SDC08A) $\theta_{JA} = 39^{\circ}\text{C/W}$

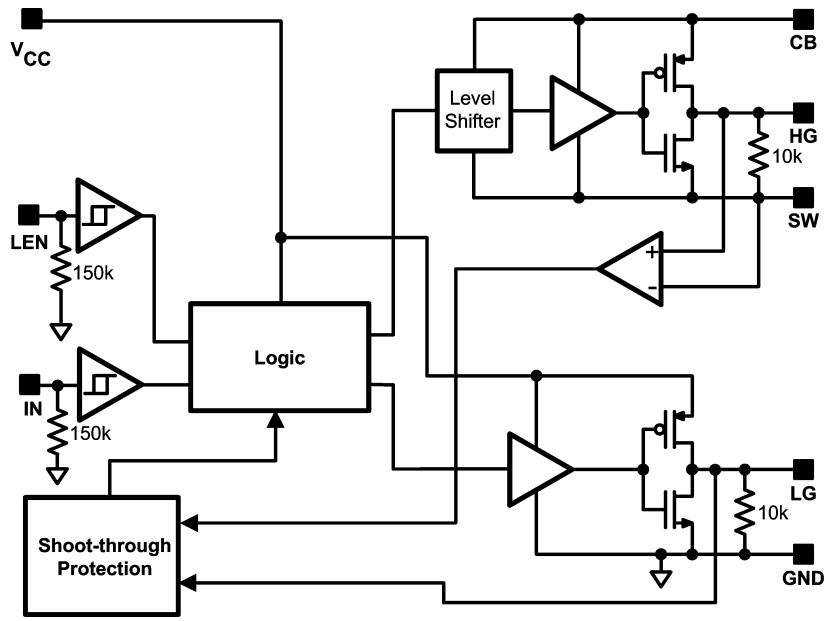
Ordering Information

| Order Number | Size | NSC Drawing # | Package Type | Supplied As |
|--------------|-------|---------------|---------------|-----------------|
| LM27222M | SO-8 | M08A | Rail | 95 Units/Rail |
| LM27222MX | | | Tape and Reel | 2500 Units/Reel |
| LM27222SD | LLP-8 | SDC08A | Tape and Reel | 1000 Units/Reel |
| LM27222SDX | | | Tape and Reel | 4500 Units/Reel |

Pin Description

| Pin # | Pin Name | Pin Function |
|-------|-----------------|---|
| 1 | SW | High-side driver return. Should be connected to the common node of high and low-side MOSFETs. |
| 2 | HG | High-side gate drive output. Should be connected to the high-side MOSFET gate. Pulled down internally to SW with a 10K resistor to prevent spurious turn on of the high-side MOSFET when the driver is off. |
| 3 | CB | Bootstrap. Accepts a bootstrap voltage for powering the high-side driver. |
| 4 | IN | Accepts a logic control signal from a controller. Pulled down internally to GND with a 150K resistor to prevent spurious turn on of the high-side MOSFET when the controller is inactive. |
| 5 | LEN | Low-side gate enable. Pulled down internally to GND with a 150K resistor to prevent spurious turn-on of the low-side MOSFET when the controller is inactive. |
| 6 | V _{CC} | Connect to +5V supply. |
| 7 | LG | Low-side gate drive output. Should be connected to low-side MOSFET gate. Pulled down internally to GND with a 10K resistor to prevent spurious turn on of the low-side MOSFET when the driver is off. |
| 8 | GND | Ground. |

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|------------------------|--------------|
| V _{CC} to GND | -0.3V to 7V |
| CB to GND | -0.3V to 36V |
| CB to SW | -0.3V to 7V |
| SW to GND (Note 2) | -0.2V to 36V |
| LEN to GND | -0.3V to 7V |
| IN to GND | -0.3V to 7V |
| LG to GND | -0.3V to 7V |
| HG to GND | -0.3V to 36V |

| | |
|----------------------------|---------------|
| Junction Temperature | +150°C |
| Power Dissipation (Note 3) | 720mW |
| Storage Temperature | -65° to 150°C |
| ESD Susceptibility | |
| Human Body Model | 2kV |

Operating Ratings (Note 1)

| | |
|----------------------------|---------------|
| VCC | 4V to 7V |
| Junction Temperature Range | -40° to 125°C |
| CB (max) | 33V |

Electrical Characteristics (Note 4)

VCC = CB = 5V, SW = GND = 0V, unless otherwise specified. Typical and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over the entire operating temperature range (-40°C ≤ T_J ≤ 125°C).

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------------|-------------------------------------|---|-----|------|------------|-------|
| POWER SUPPLY | | | | | | |
| I _{q_op} | Operating Quiescent Current | IN = 0V, LEN = 0V | | 5 | 15 | μA |
| | | | | | 30 | |
| | | IN = 0V, LEN = 5V | 500 | 540 | 650 | μA |
| | | | | | 825 | |
| HIGH-SIDE DRIVER | | | | | | |
| | Peak Pull-up Current | | | 3 | | A |
| R _{H-pu} | Pull-up Rds_on | I _{CB} = I _{HG} = 0.3A | | 0.9 | 2.5 | Ω |
| | Peak Pull-down Current | | | 4.5 | | A |
| R _{H-pd} | Pull-down Rds_on | I _{SW} = I _{HG} = 0.3A | | 0.4 | 1.5 | Ω |
| t ₄ | Rise Time | Timing Diagram, C _{LOAD} = 3.3nF | | 17 | | ns |
| t ₆ | Fall Time | Timing Diagram, C _{LOAD} = 3.3nF | | 12 | | ns |
| t ₃ | Pull-up Dead Time | Timing Diagram | | 9.5 | | ns |
| t ₅ | Pull-down Delay | Timing Diagram | | 16.5 | | ns |
| t _{on_min} | Minimum Positive Output Pulse Width | | | 30 | | ns |
| LOW-SIDE DRIVER | | | | | | |
| | Peak Pull-up Current | | | 3.2 | | A |
| R _{L-pu} | Pull-up Rds_on | I _{VCC} = I _{LG} = 0.3A | | 0.9 | 2.5 | Ω |
| | Peak Pull-down Current | | | 4.5 | | A |
| R _{L-pd} | Pull-down Rds_on | I _{GND} = I _{LG} = 0.3A | | 0.4 | 1.5 | Ω |
| t ₈ | Rise Time | Timing Diagram, C _{LOAD} = 3.3nF | | 17 | | ns |
| t ₂ | Fall Time | Timing Diagram, C _{LOAD} = 3.3nF | | 14 | | ns |
| t ₇ | Pull-up Dead Time | Timing Diagram | | 11.5 | | ns |
| t ₁ | Pull-down Delay | Timing Diagram | | 7.7 | | ns |
| PULL-DOWN RESISTANCES | | | | | | |
| | HG-SW Pull-down Resistance | | | 10k | | Ω |
| | LG-GND Pull-down Resistance | | | 10k | | Ω |
| | LEN-GND Pull-down Resistance | | | 150K | | Ω |
| | IN-GND Pull-down Resistance | | | 150K | | Ω |
| LEAKAGE CURRENTS | | | | | | |
| I _{leak_IN} | IN pin Leakage Current | IN = 0V, Source Current | | 50 | | nA |
| | | IN = 5V, Sink Current | | 33 | | μA |

Electrical Characteristics (Note 4) (Continued)

VCC = CB = 5V, SW = GND = 0V, unless otherwise specified. Typical and limits appearing in plain type apply for $T_A = T_J = +25^\circ\text{C}$. Limits appearing in **boldface** type apply over the entire operating temperature range ($-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$).

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------|-------------------------|--------------------------|-----|-----|-----|---------------|
| $I_{\text{leak_LEN}}$ | LEN pin Leakage Current | LEN = 0V, Source Current | | 200 | | nA |
| | | LEN = 5V, Sink Current | | 33 | | μA |

LOGIC

| | | | | | | |
|----------------------|-----------------------------|--------------------------------|-----------|--|-----------|----------------------|
| $V_{\text{IH_LEN}}$ | LEN Pin High Input | When LEN pin goes high from 0V | | | 65 | % of V_{CC} |
| $V_{\text{IL_LEN}}$ | LEN Pin Low Input | When LEN pin goes low from 5V | 30 | | | % of V_{CC} |
| $V_{\text{IH_IN}}$ | IN High Level Input Voltage | When IN pin goes high from 0V | | | 65 | % of V_{CC} |
| $V_{\text{IL_IN}}$ | IN Low Level Input Voltage | When IN pin goes low from 5V | 30 | | | % of V_{CC} |

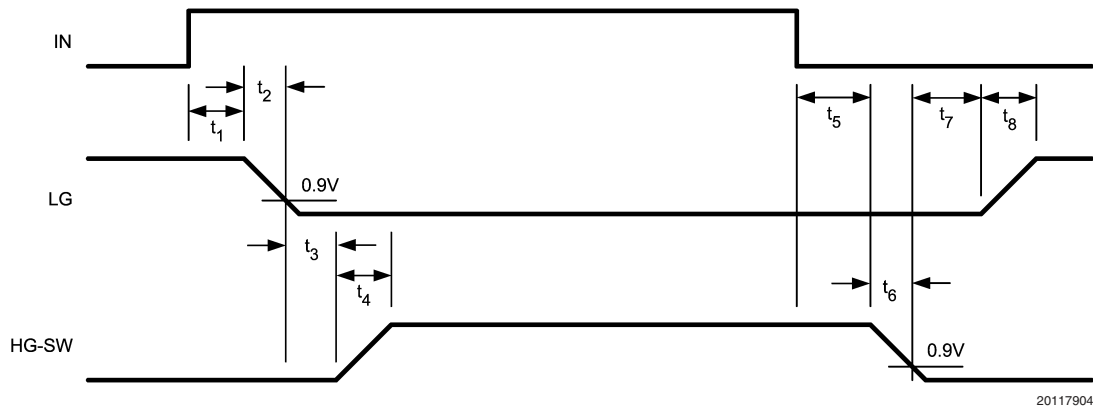
Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. Operating Ratings do not imply guaranteed performance limits.

Note 2: The SW pin can have -2V to -0.5V volts applied for a maximum duty cycle of 10% with a maximum period of 1 second. There is no duty cycle or maximum period limitation for a SW pin voltage range of -0.5V to 30 Volts.

Note 3: Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX} , the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{\text{MAX}} = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}}$. The junction-to-ambient thermal resistance, θ_{JA} , for the LM2722, it is 172°C/W . For a T_{JMAX} of 150°C and T_A of 25°C , the maximum allowable power dissipation is 0.7W. The θ_{JA} for the LM2724 LLP-8 package is 39°C/W . For a T_{JMAX} of 150°C and T_A of 25°C , the maximum allowable power dissipation is 3.2W.

Note 4: Min and Max limits are 100% production tested at 25°C . Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Timing Diagram



Typical Waveforms

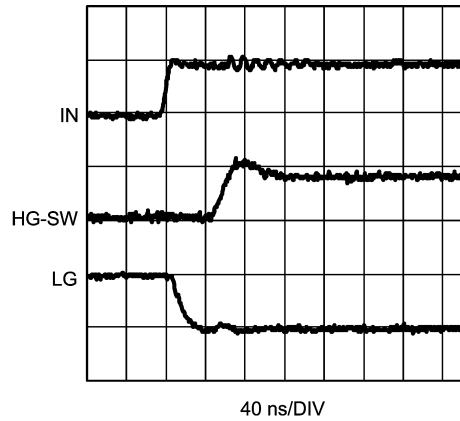


FIGURE 2. IN Rising

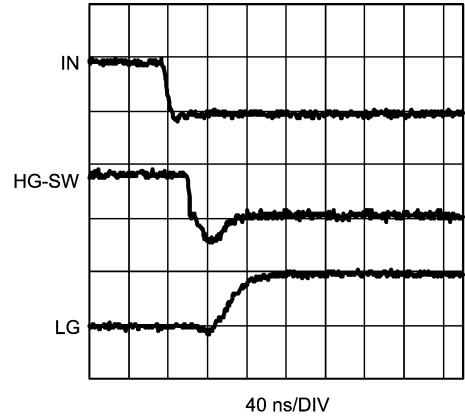


FIGURE 3. IN Falling

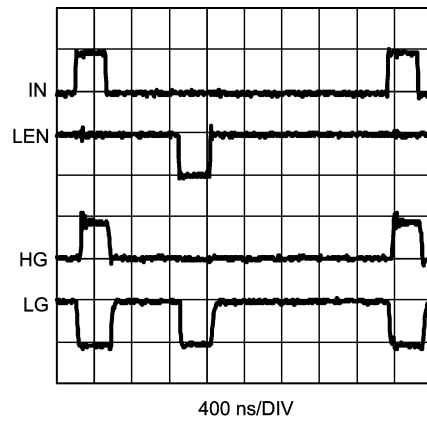


FIGURE 4. LEN Operation

The typical waveforms are from a circuit similar to *Figure 1* with:

Q1: 2 x Si7390DP

Q2: 2 x Si7356DP

L1: 0.4 μ H

V_{IN} : 12V

Application Information

MINIMUM PULSE WIDTH

As the input pulse width to the IN pin is decreased, the pulse width of the high-side gate drive (HG-SW) also decreases. However, for input pulse widths 60ns and smaller, the HG-SW remains constant at 30ns. Thus the minimum pulse width of the driver output is 30ns. *Figure 5* shows an input pulse at the IN pin 20ns wide, and the output of the driver, as measured between the nodes HG and SW is a 30ns wide pulse. *Figure 6* shows the variation of the SW node pulse width vs IN pulse width. At the IN pin, if a falling edge is followed by a rising edge within 5ns, the HG may ignore the rising edge and remain low until the IN pin toggles again. If a rising edge is followed by a falling edge within 5ns, the pulse may be completely ignored.

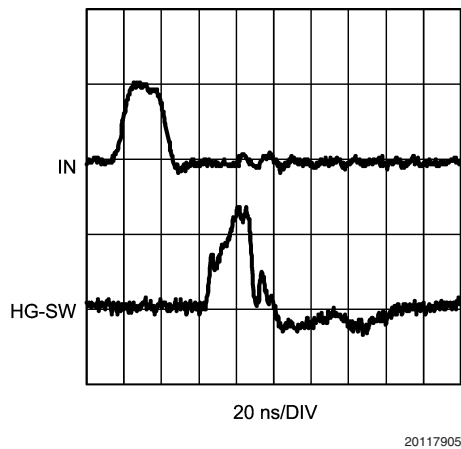


FIGURE 5. Min On Time

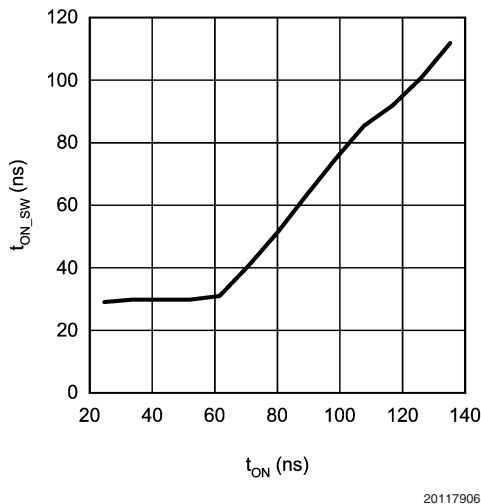


FIGURE 6.

ADAPTIVE SHOOT-THROUGH PROTECTION

The LM27222 prevents shoot-through power loss by ensuring that both the high- and low-side MOSFETs are not conducting at the same time. When the IN signal rises, LG is first pulled down. The adaptive shoot-through protection circuit waits for LG to reach 0.9V before turning on HG. Similarly,

when IN goes low, HG is pulled down first, and the circuit turns LG on only after the voltage difference between the high-side gate and the switch node, ie HG-SW, has fallen to 0.9V. The dead-time between the high and low-side pulses is kept as small as possible to minimize conduction through the body diode of the low-side MOSFET(s).

POWER DISSIPATION

The power dissipated in the driver IC when switching synchronously can be calculated as follows:

$$P = \frac{f_{SW} \times V_{CC}}{2} \left[Q_{G-H} \left(\frac{R_{H-pu}}{R_{H-pu} + R_{G-H}} \right) + \left(\frac{R_{H-pd}}{R_{H-pd} + R_{G-H}} \right) + Q_{G-L} \left(\frac{R_{L-pu}}{R_{L-pu} + R_{G-L}} \right) + \left(\frac{R_{L-pd}}{R_{L-pd} + R_{G-L}} \right) \right]$$

where f_{SW} = switching frequency

V_{CC} = voltage at the V_{CC} pin,

Q_{G-H} = total gate charge of the (parallel combination of the) high-side MOSFET(s)

Q_{G-L} = total gate charge of the (parallel combination of the) low-side MOSFET(s)

R_{G-H} = gate resistance of the (parallel combination of the) high-side MOSFET(s)

R_{G-L} = gate resistance of the (parallel combination of the) low-side MOSFET(s)

R_{H-pu} = pull-up R_{DS_ON} of the high-side driver

R_{H-pd} = pull-down R_{DS_ON} of the high-side driver

R_{L-pu} = pull-up R_{DS_ON} of the low-side driver

R_{L-pd} = pull-down R_{DS_ON} of the low-side driver

PC BOARD LAYOUT GUIDELINES

1. Place the driver as close to the MOSFETs as possible
2. HG, SW, LG, GND: Run short, thick traces between the driver and the MOSFETs. To minimize parasitics, the traces for HG and SW should run parallel and close to each other. The same is true for LG and GND
3. Driver V_{CC} : Place the coupling capacitor close to the V_{CC} and GND pins
4. The high-current loop between the high-side and low-side MOSFETs and the input capacitors should be as small as possible
5. There should be enough copper area near the MOSFETs and the inductor for heat dissipation. Vias may also be added to carry the heat to other layers

TYPICAL APPLICATION CIRCUIT DESCRIPTION

The Typical Application Circuit shown on the following page shows the LM27222 being used with National's LM27212 2-Phase Hysteretic Current mode controller. Although this circuit is capable of operating from 5V to 28V, the components are optimized for a input voltage range of 9V to 28V. The high-side FET is selected for low gate charge to reduce switching losses. For low duty cycles, the average current is relatively small and thus we trade off higher conduction losses for lower switching losses. The low side FET is selected solely on R_{DS_ON} to minimize conduction losses. If the input voltage range were 4V to 6V, the MOSFET selection should be changed. First, much lower voltage FETs can be

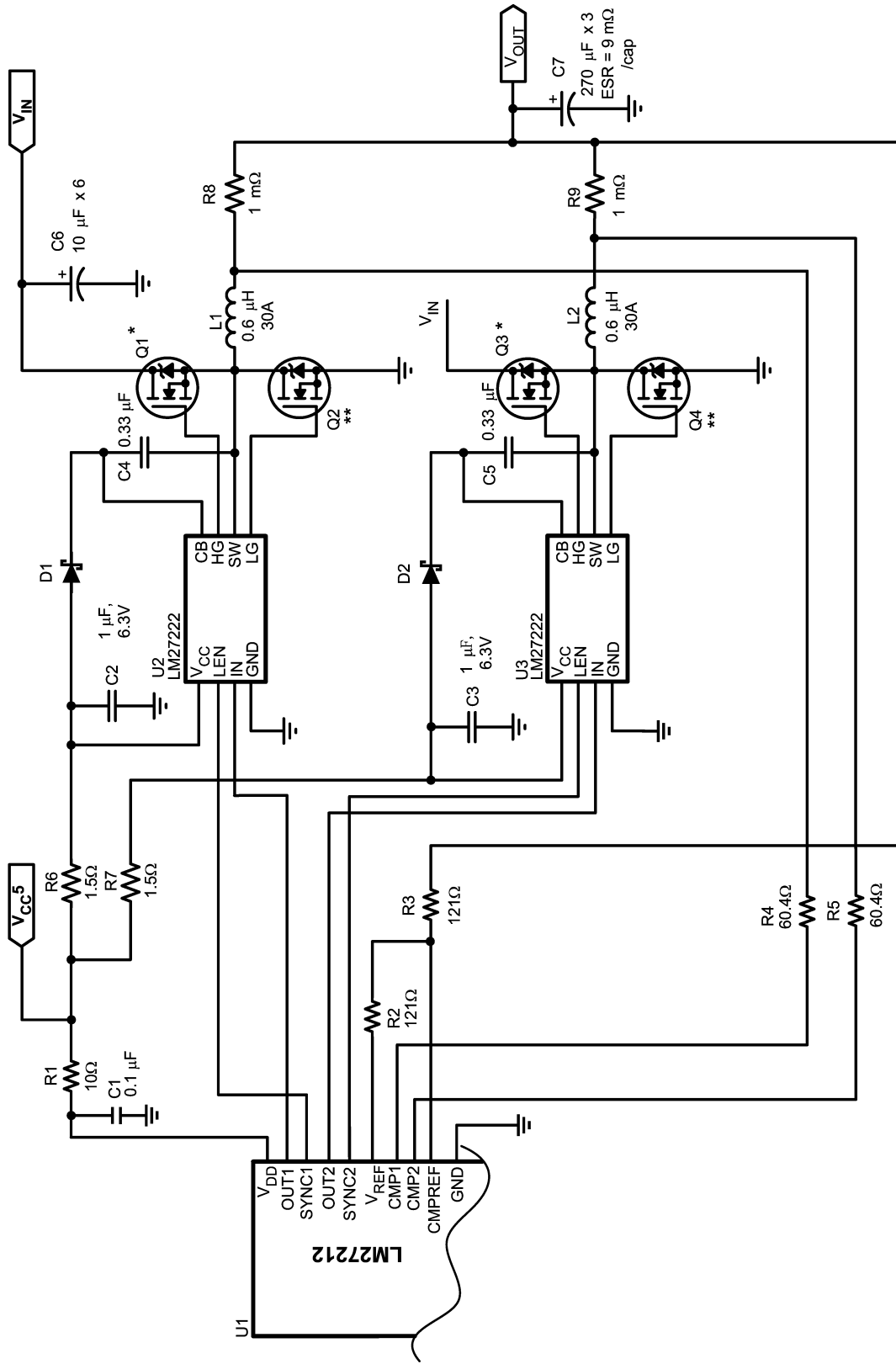
Application Information (Continued)

used, and secondly, high-side switch resistance becomes a larger loss factor than the switching losses. Of course with a lower input voltage, the input capacitor voltage rating can be reduced and the inductor value can be reduced as well. For a 4V to 6V application, the inductor can be reduced to 200nH to 300nH. The switching frequency of the LM27212 is determined by the allowed ripple current in the inductor. This

circuit is set for approximately 300kHz. At lower input voltages, higher frequencies are possible without suffering significant efficiency loss. Although the LM27222 can support operating frequencies up to 2MHz in many applications, the LM27212 should be limited to about 1MHz. The control architecture of the LM27212 and the low propagation times of the LM27222 potentially gives this solution the fastest transient response in the industry.

Application Information (Continued)

Typical Application Circuit

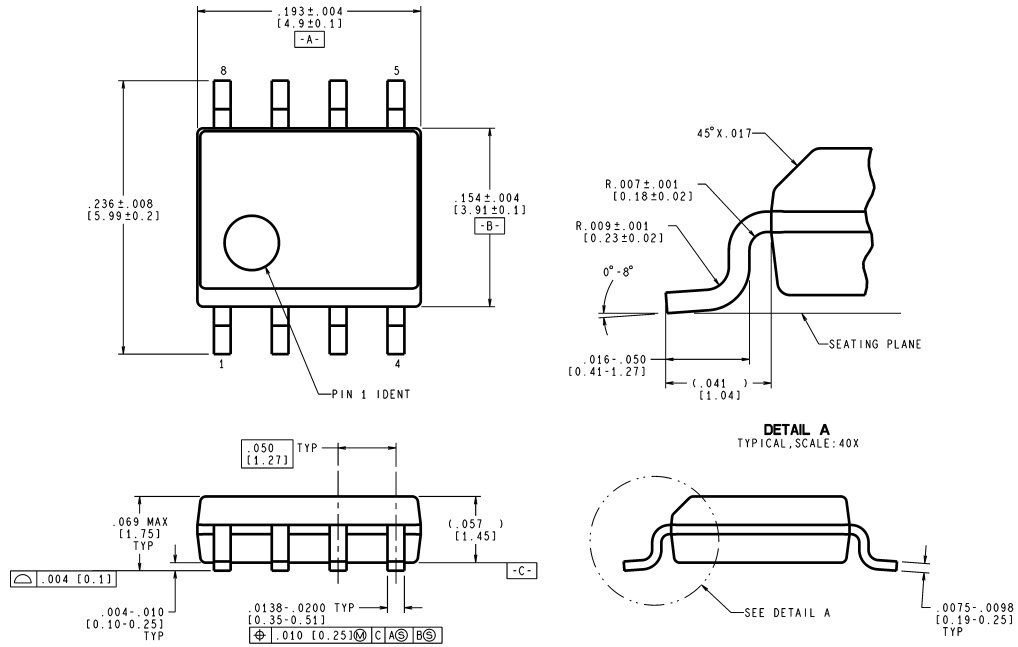


* Q1, Q3: 2 x S17390DP
 ** Q2, Q4: 2 x S17356DP

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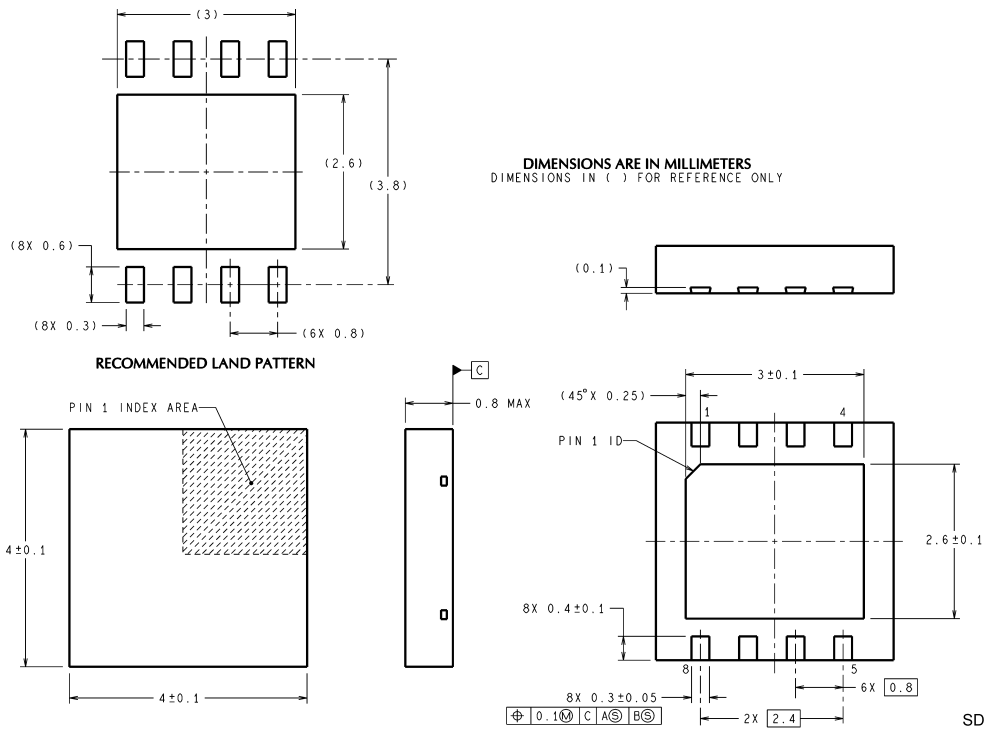
Physical Dimensions inches (millimeters)

unless otherwise noted



M08A (Rev J)

8-Lead Small Outline Package
Order Number: LM27222M, LM27222MX
NS Package Number M08A



SDC08A (Rev A)

8-Lead LLP Package
Order Number: LM27222SD, LM27222SDX
NS Package Number SDC08A

Notes

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Support Center
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