

MM54C905/MM74C905 12-Bit Successive Approximation Register

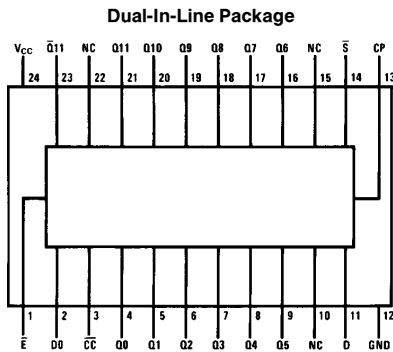
General Description

The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45V_{CC} typ
- Low power TTL fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

Connection Diagram



Order Number MM74C905N
See NS Package Number N24C

See the CMOS Logic Databook
for Complete Specifications

Top View

TL/F/5712-1

Truth Table

TIME	INPUTS			OUTPUTS														
	t _n	D	\bar{S}	\bar{E}	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	\bar{C}
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L	H
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L	H
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

MM54C905/MM74C905 12-Bit Successive Approximation Register

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	-0.3 to V_{CC} + 0.3V
Operating Temperature Range	
MM74C905	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

ESD Susceptibility (Note 4)

Package Dissipation	400V
Operating V_{CC} Range	500 mW
Absolute Maximum V_{CC}	3.0V to 15V
Lead Temperature (Soldering, 10 seconds)	16V
	260°C

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5.0V$	3.5			V
	$V_{CC} = 10V$	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5.0V$			1.5	V
	$V_{CC} = 10V$			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5.0V, I_O = -10\mu A$	4.5			V
	$V_{CC} = 10V, I_O = -10\mu A$	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5.0V, I_O = 10\mu A$			0.5	V
	$V_{CC} = 10V, I_O = 10\mu A$			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
Supply Current (I_{CC})	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) MM54C905 MM74C905	$V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$) MM54C905 MM74C905	$V_{CC} = 4.5V$			0.8	V
	$V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$) MM54C905 MM74C905	$V_{CC} = 4.5V, I_O = -360\mu A$	2.4			V
	$V_{CC} = 4.75V, I_O = -360\mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$) MM54C905 MM74C905	$V_{CC} = 4.5V, I_O = 360\mu A$			0.4	V
	$V_{CC} = 4.75V, I_O = 360\mu A$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-1.75	-3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-8.0	-15		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	8.0	16		mA
Q11-Q0 Outputs R_{SOURCE}	$V_{CC} = 10V \pm 5\%$ $V_{OUT} = V_{CC} - 0.3V$ $T_A = 25^\circ C$	150		350	Ω
R_{SINK}	$V_{CC} = 10V \pm 5\%$ $V_{OUT} = 0.3V$ $T_A = 25^\circ C$	80		230	Ω

AC Electrical Characteristics $T_A = 25^\circ\text{C}, C_L = 50\text{pF}$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Propagation Delay Time From Clock	$V_{CC} = 5.0\text{V}$		200	350	ns
Input To Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 10\text{V}$		80	150	ns
Propagation Delay Time From Clock	$V_{CC} = 5.0\text{V}$		180	325	ns
Input To D_O ($t_{pd(D_O)}$)	$V_{CC} = 10\text{V}$		70	125	ns
Propagation Delay Time From Register	$V_{CC} = 5.0\text{V}$		190	350	ns
Enable (\bar{E}) To Output (Q11) ($t_{pd(\bar{E})}$)	$V_{CC} = 10\text{V}$		75	150	ns
Propagation Delay Time From Clock	$V_{CC} = 5.0\text{V}$		190	350	ns
To $\bar{C}\bar{C}$ ($t_{pd(\bar{C}\bar{C})}$)	$V_{CC} = 10\text{V}$		75	0.50	ns
Data Input Set-Up Time (t_{DS})	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	80 30			ns ns
Start Input Set-Up Time (t_{SS})	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	80 30			ns ns
Minimum Clock Pulse Width (t_{PWL}, t_{PWH})	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	250 100	125 40		ns ns
Maximum Clock Rise and Fall Time (t_r, t_f)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$			15 5	μs μs
Maximum Clock Frequency (f_{MAX})	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	2 5	4 10		MHz MHz
Clock Input Capacitance (C_{CLK})	Clock Input (Note 2)		10		pF
Input Capacitance (C_{IN})	Any Other Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	(Note 3)		100		pF

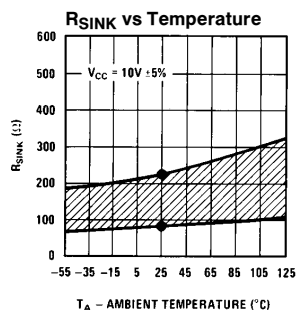
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

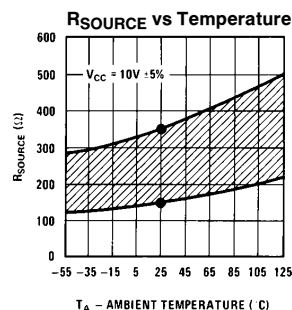
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Typical Performance Characteristics



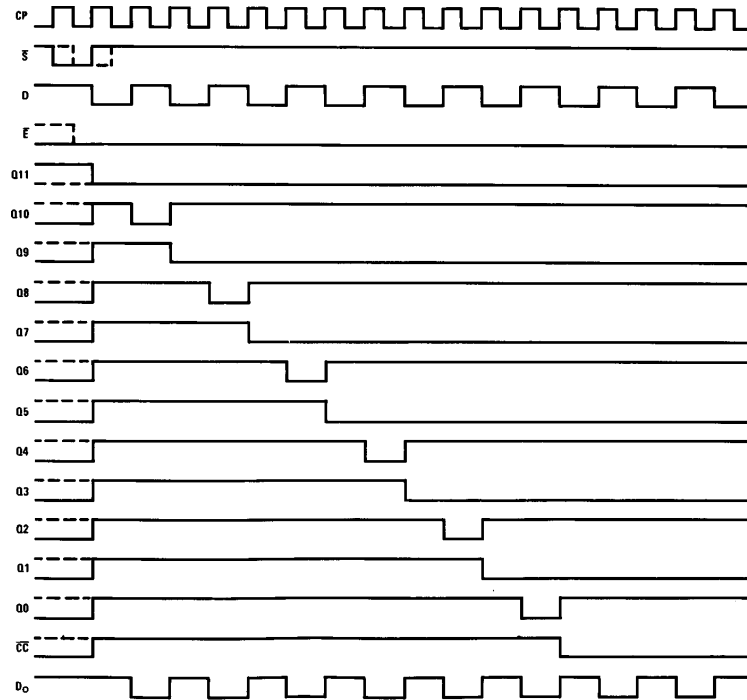
•These points are guaranteed by automatic testing



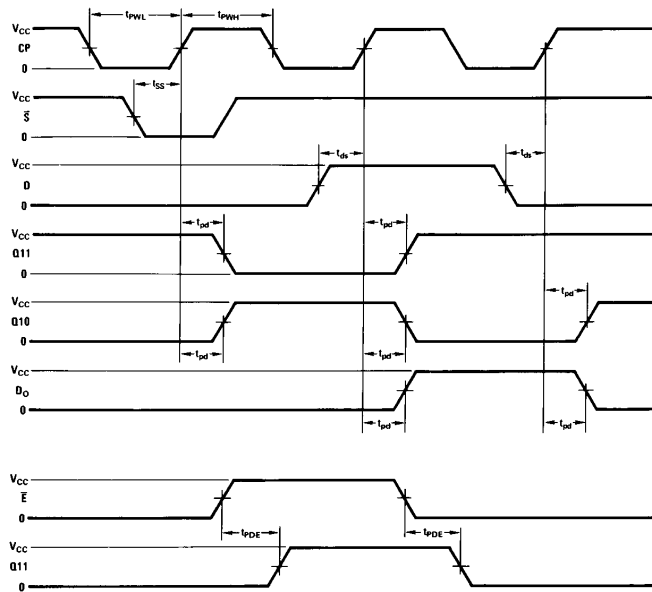
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TL/F/5712-2

Timing Diagram

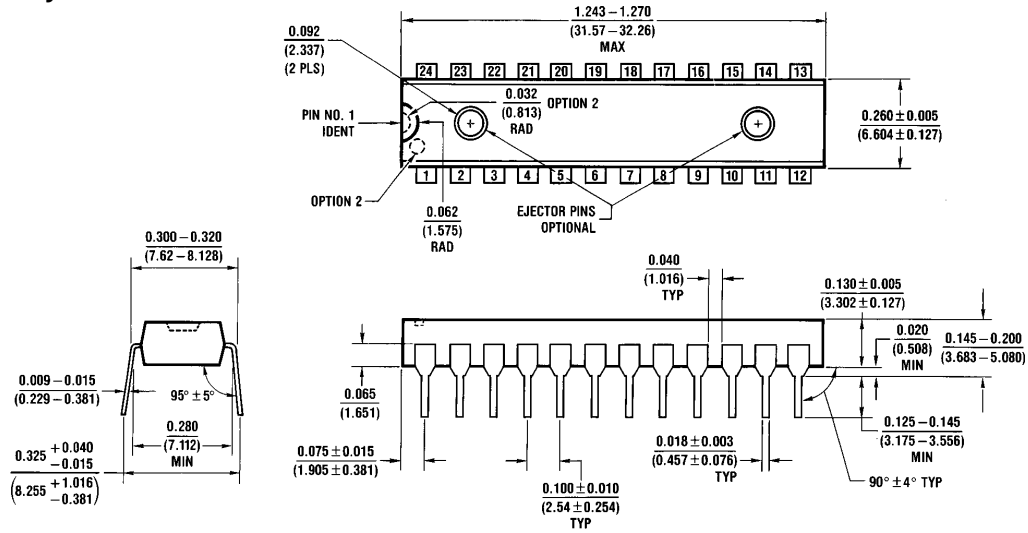


Switching Time Waveforms



TL/F/5712-3

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number MM74C905N
NS Package Number N24C

N24C (REV F)

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