

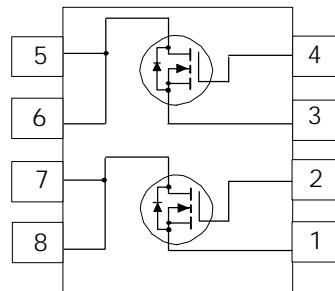
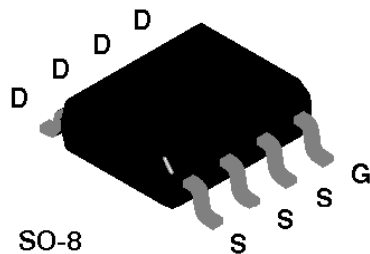
N

**NDS8936****Dual N-Channel Enhancement Mode Field Effect Transistor****General Description**

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

**Features**

- 5.3A, 30V.  $R_{DS(ON)} = 0.035\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} = 0.05\Omega @ V_{GS} = 4.5V$
- High density cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.

**Absolute Maximum Ratings**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	NDS8936	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	$\pm 5.3$	A
	- Pulsed	$\pm 20$	
$P_D$	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$			1	$\mu\text{A}$
					10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	1	1.6	2.8	V
			0.7	1.2	2.2	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5.3\text{ A}$ $T_J = 125^\circ\text{C}$		0.033	0.035	$\Omega$
				0.046	0.063	
		$V_{GS} = 4.5\text{ V}, I_D = 4.4\text{ A}$ $T_J = 125^\circ\text{C}$		0.046	0.05	
				0.064	0.09	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	20			A
			10			
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 5.3\text{ A}$		10.5		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		720		pF
$C_{oss}$	Output Capacitance			370		pF
$C_{rss}$	Reverse Transfer Capacitance			250		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GEN} = 10\text{ V}, R_{GEN} = 6\ \Omega$		12	20	ns
$t_r$	Turn - On Rise Time			13	30	
$t_{D(off)}$	Turn - Off Delay Time			29	50	
$t_f$	Turn - Off Fall Time			10	20	
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V},$ $I_D = 5.3\text{ A}, V_{GS} = 10\text{ V}$		19	30	nC
$Q_{gs}$	Gate-Source Charge			2.2		
$Q_{gd}$	Gate-Drain Charge			5.5		

## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				1.2	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 5.3\text{ A}$ (Note 2)		0.9	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}$ , $I_F = 1.25\text{ A}$ , $di_F/dt = 100\text{ A}/\mu\text{s}$			100	ns

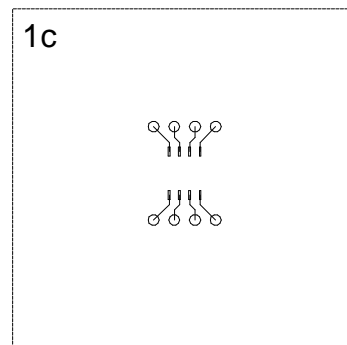
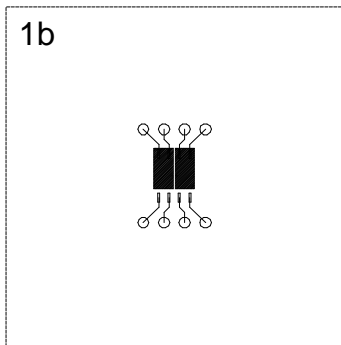
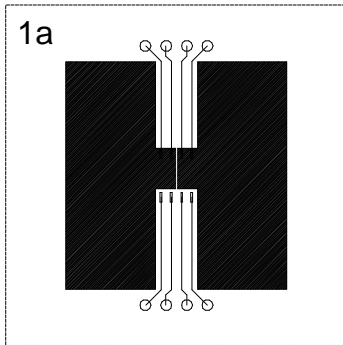
Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical  $R_{\theta JA}$  for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 78°C/W when mounted on a 0.5 in<sup>2</sup> pad of 2oz copper.
- 125°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2oz copper.
- 135°C/W when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper.

- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

# Typical Electrical Characteristics

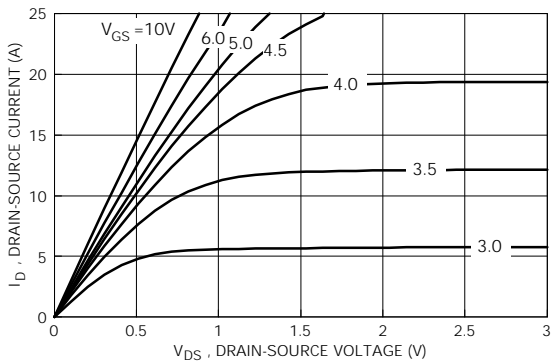


Figure 1. On-Region Characteristics.

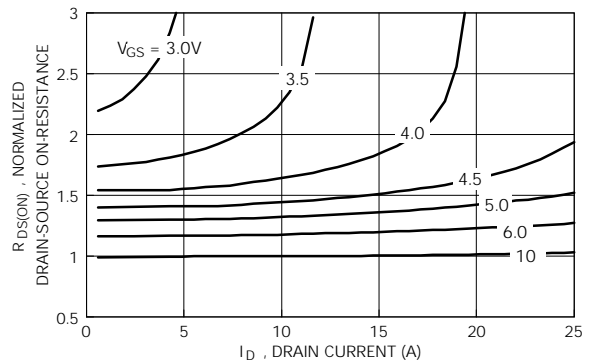


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

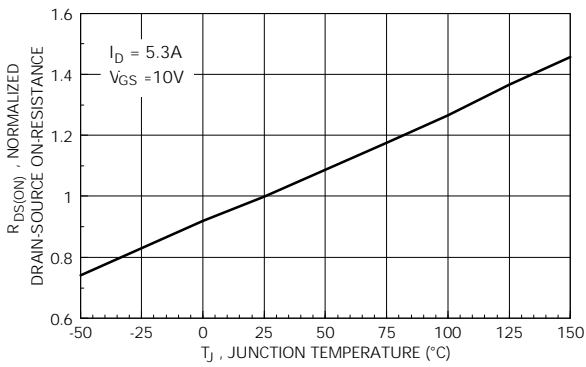


Figure 3. On-Resistance Variation with Temperature.

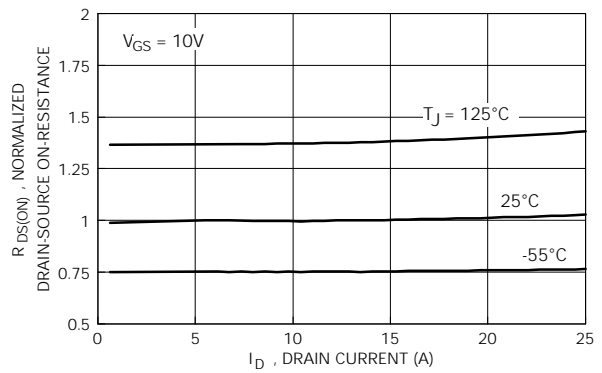


Figure 4. On-Resistance Variation with Drain Current and Temperature.

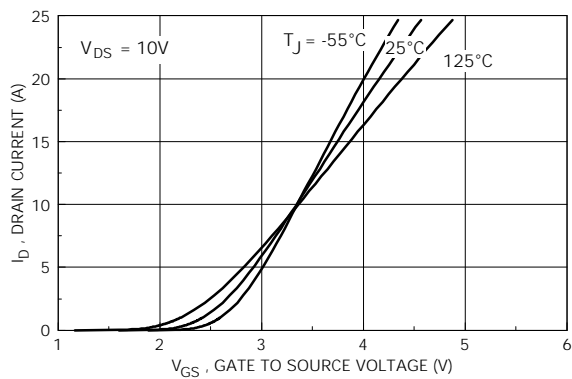


Figure 5. Transfer Characteristics.

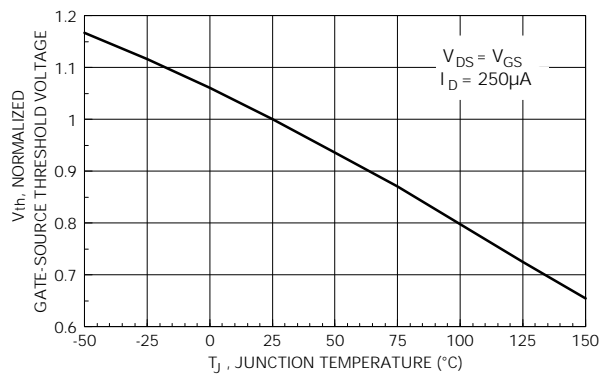


Figure 6. Gate Threshold Variation with Temperature.

## Typical Electrical Characteristics

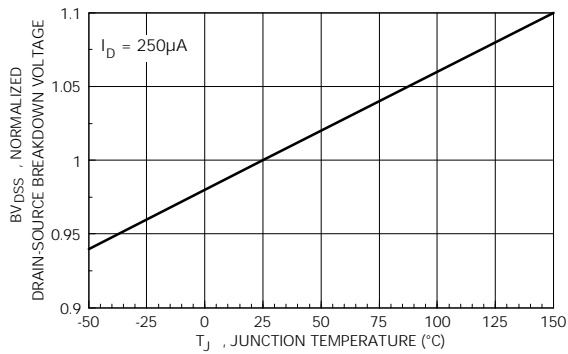


Figure 7. Breakdown Voltage Variation with Temperature.

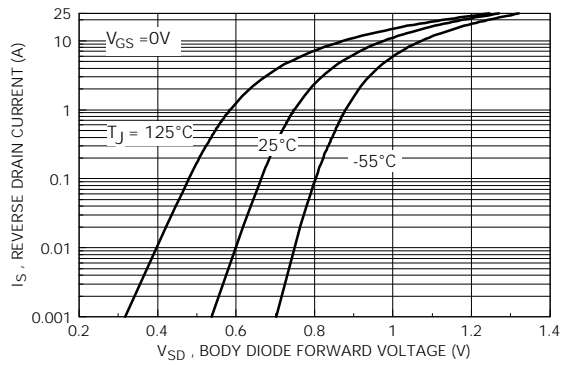


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

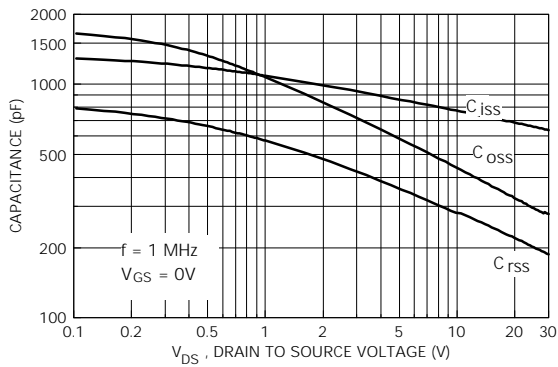


Figure 9. Capacitance Characteristics.

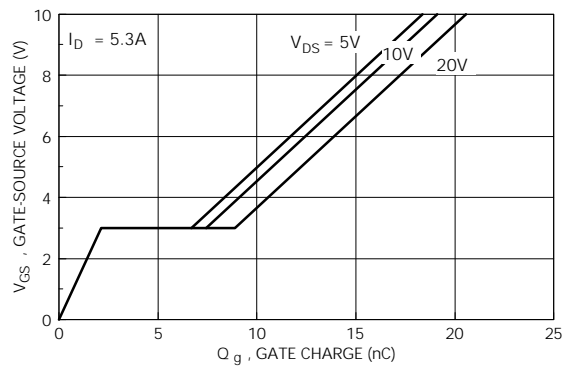


Figure 10. Gate Charge Characteristics.

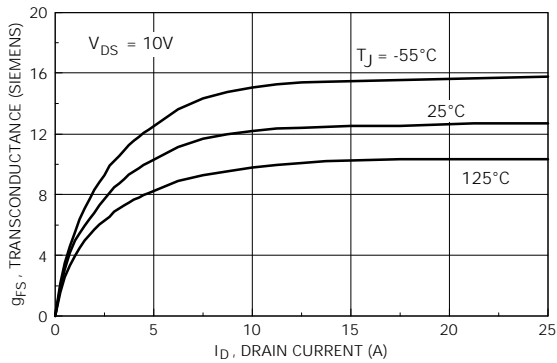
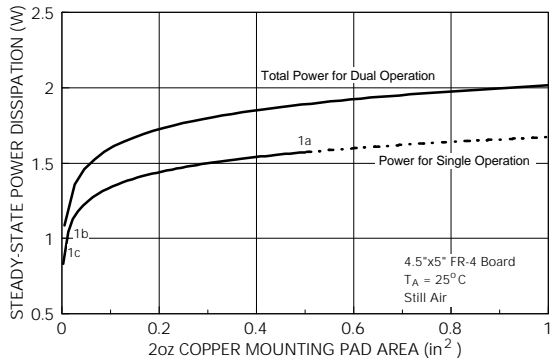
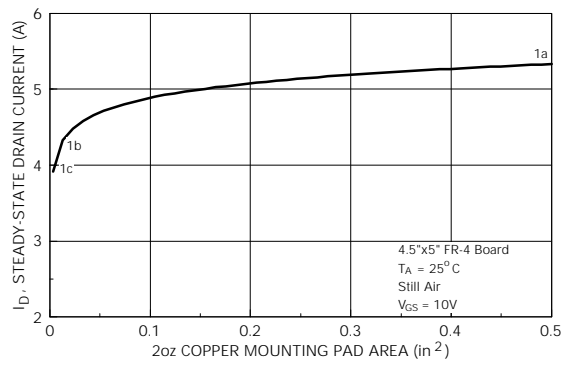


Figure 11. Transconductance Variation with Drain Current and Temperature.

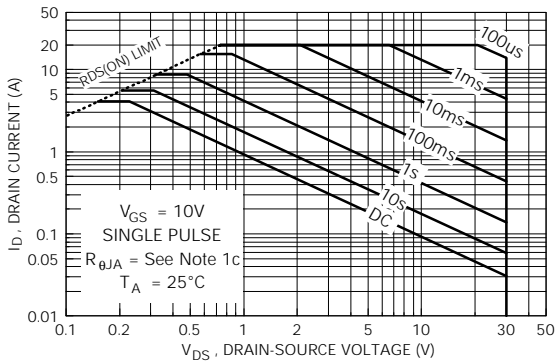
## Typical Thermal Characteristics



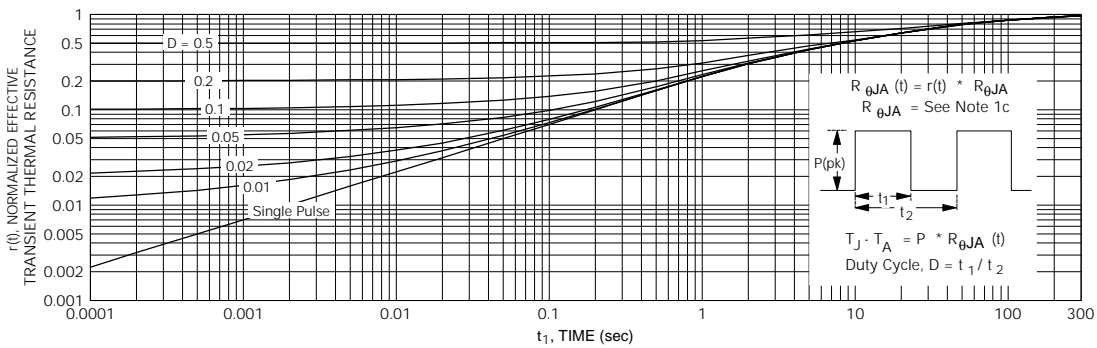
**Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**



**Figure 13. Maximum Steady-State Drain Current**



**Figure 14. Maximum Safe Operating Area.**



**Figure 15. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.