

MSM5118160F**1,048,576-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE****DESCRIPTION**

The MSM5118160F is a 1,048,576-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM5118160F achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM5118160F is available in a 42-pin plastic SOJ or 50/44-pin plastic TSOP.

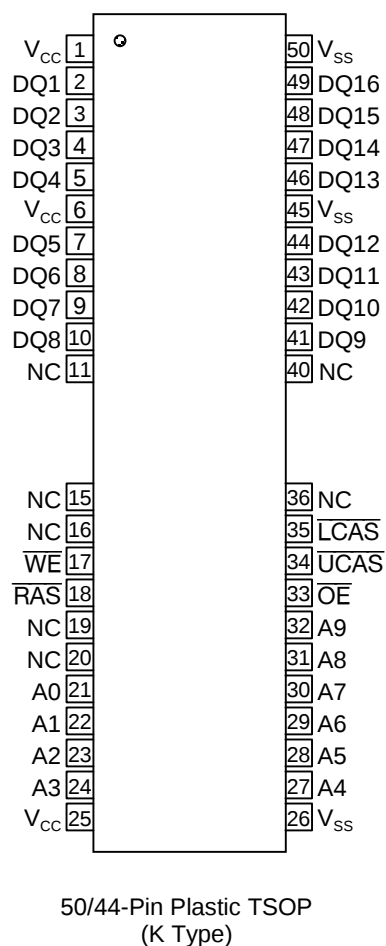
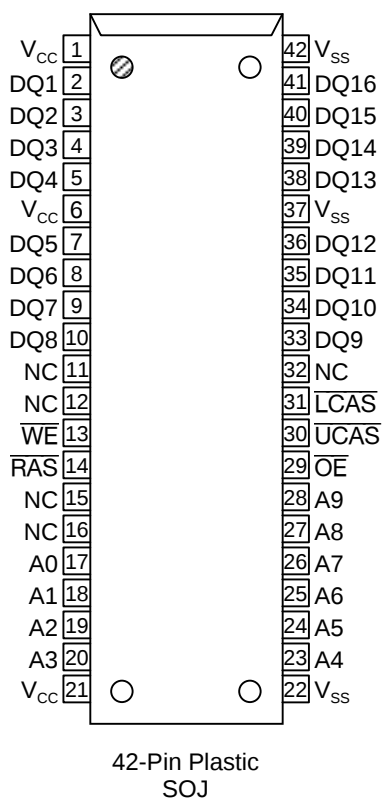
FEATURES

- 1,048,576-word × 16-bit configuration
 - Single 5V power supply, ±10% tolerance
 - Input : TTL compatible, low input capacitance
 - Output : TTL compatible, 3-state
 - Refresh : 1024 cycles/16ms
 - Fast page mode, read modify write capability
 - CAS before RAS refresh, hidden refresh, RAS-only refresh capability
 - Packages
 - 42-pin 400mil plastic SOJ (SOJ42-P-400-1.27) (Product : MSM5118160F-xxJS)
 - 50/44-pin 400mil plastic TSOP (TSOPII50/44-P-400-0.80-K) (Product : MSM5118160F-xxTS-K)
- xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM5118160F	50ns	25ns	13ns	13ns	90ns	743mW	5.5mW
	60ns	30ns	15ns	15ns	110ns	688mW	
	70ns	35ns	20ns	20ns	130ns	633mW	

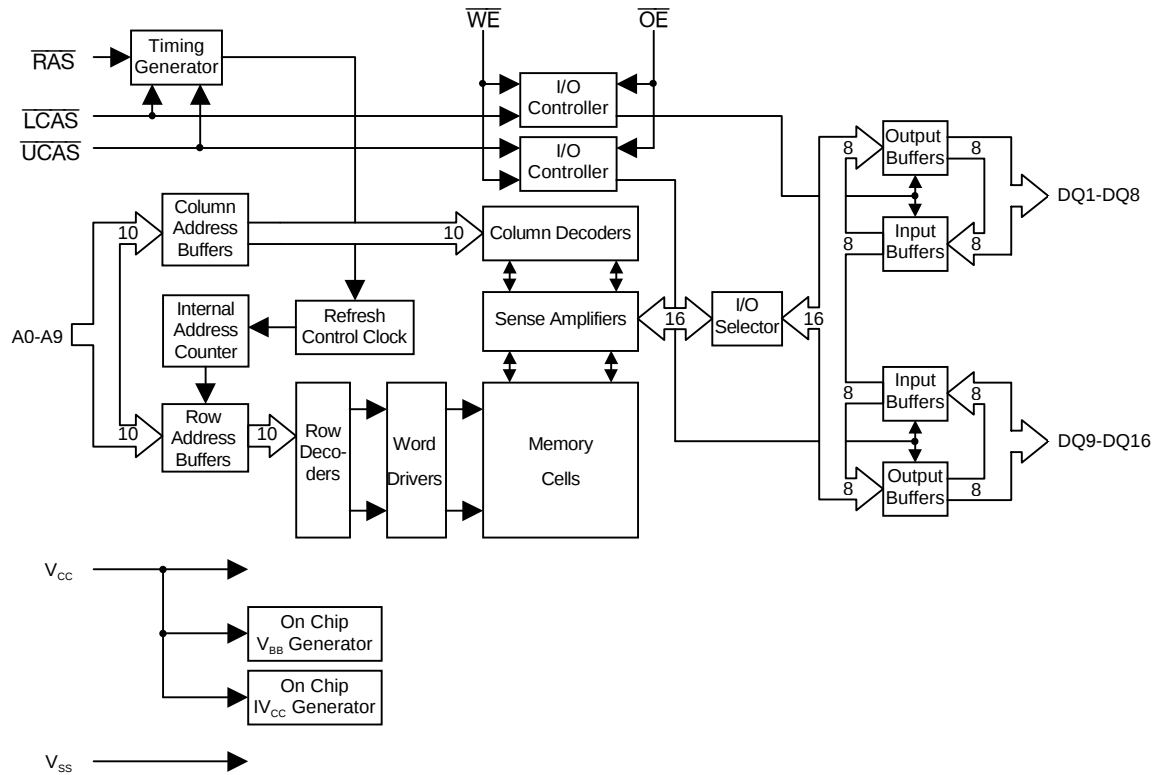
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0–A9	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{LCAS}}$	Lower Byte Column Address Strobe
$\overline{\text{UCAS}}$	Upper Byte Column Address Strobe
DQ1–DQ16	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V_{CC}	Power Supply (5V)
V_{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
RAS	LCAS	UCAS	WE	OE	DQ1-DQ8	DQ9-DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D _{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D _{OUT}	Upper Byte Read
L	L	L	H	L	D _{OUT}	D _{OUT}	Word Read
L	L	H	L	H	D _{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D _{IN}	Upper Byte Write
L	L	L	L	H	D _{IN}	D _{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

* : "H" or "L"

ELECTRICAL CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Voltage V_{CC} Supply relative to V_{SS}	V_{CC}	-0.5 to 7	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_{D^*}	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^{\circ}\text{C}$ **RECOMMENDED OPERATING CONDITIONS** $(T_a = 0 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC} + 0.5^{*1}$	V
Input Low Voltage	V_{IL}	-0.5^{*2}	—	0.8	V

Notes: *1. The input voltage is $V_{CC} + 2.0\text{V}$ when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is $V_{SS} - 2.0\text{V}$ when the pulse width is less than 20ns (the pulse width respect to the point at which V_{SS} is applied).

PIN CAPACITANCE $(V_{CC} = 5\text{V} \pm 10\%, T_a = 25^{\circ}\text{C}, f = 1 \text{ MHz})$

Parameter	Symbol	Min.	Typ.	Min.	Unit
Input Capacitance (A0 - A9)	C_{IN1}	—	—	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{IN2}	—	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	—	7	pF

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Parameter	Symbol	Condition	MSM5118160 F-50		MSM5118160 F-60		MSM5118160 F-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V _{OH}	I _{OH} = -5.0mA	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	
Output Low Voltage	V _{OL}	I _{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0V ≤ V _I ≤ 6.5V; All other pins not under test = 0V	- 10	10	- 10	10	- 10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0V ≤ V _O ≤ V _{CC}	- 10	10	- 10	10	- 10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = Min.	—	135	—	125	—	115	mA	1,2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2V$	—	1	—	1	—	1		
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, t _{RC} = Min.	—	135	—	125	—	115	mA	1,2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	$\overline{\text{RAS}} = \text{cycling}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	135	—	125	—	115	mA	1,2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, t _{PC} = Min.	—	120	—	110	—	100	mA	1,3

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
3. The address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.
4. $V_{CC} - 0.2V \leq V_{IH} \leq V_{CC} + 0.5V$, $-0.5V \leq V_{IL} \leq 0.2V$

AC CHARACTERISTICS (1/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note1,2,3

Parameter	Symbol	MSM5118160 F-50		MSM5118160 F-60		MSM5118160 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	90	—	110	—	130	—	ns	
Read Modify Write Cycle Time	t _{RWC}	131	—	155	—	185	—	ns	
Fast Page Mode Cycle Time	t _{PC}	35	—	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	76	—	85	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	13	—	15	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	25	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	30	—	35	—	40	ns	4, 12
Access Time from $\overline{\text{OE}}$	t _{OEA}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{OFF}	0	13	0	15	0	20	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	13	0	15	0	20	ns	7
Transition Time	t _T	1	50	1	50	1	50	ns	3
Refresh Period	t _{REF}	—	16	—	16	—	16	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	13	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	7	—	10	—	10	—	ns	14
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	13	10,000	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	50	—	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	—	35	—	40	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	17	37	20	45	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	12	25	15	30	15	35	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	

AC CHARACTERISTICS (2/2)

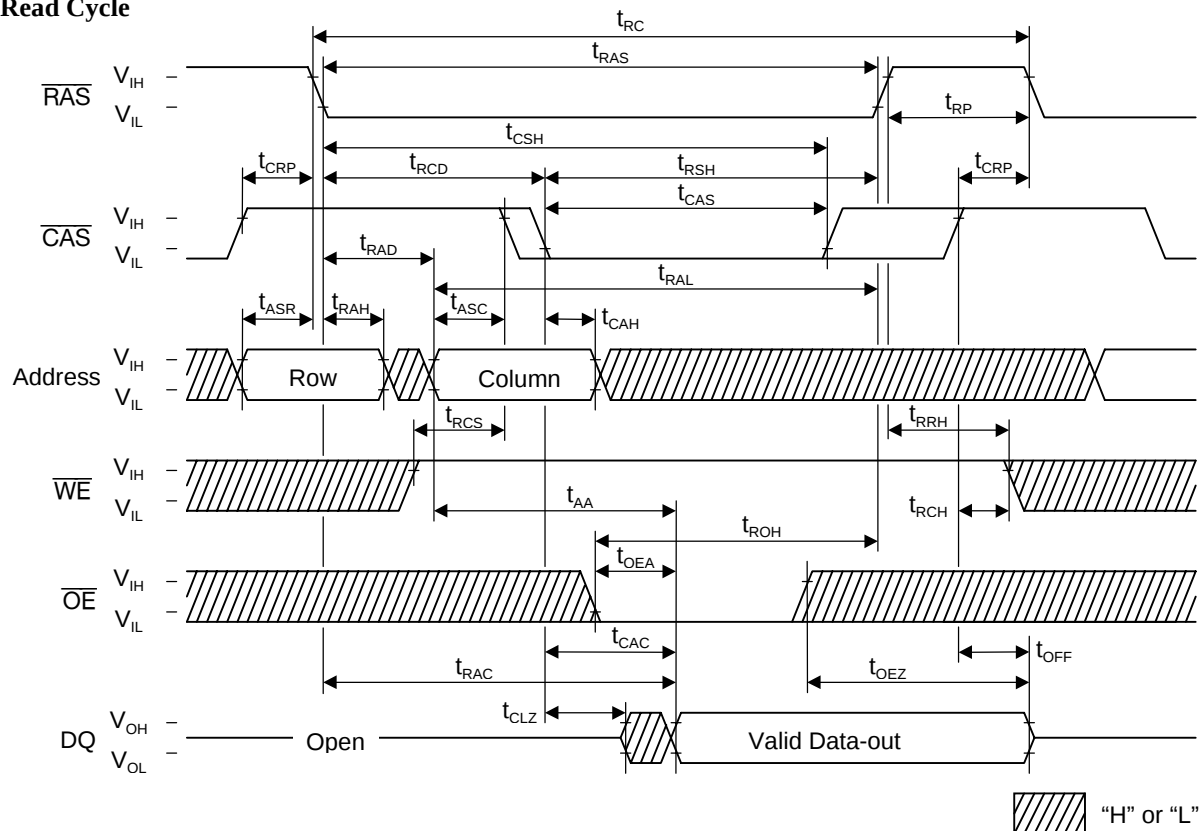
(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note1,2,3

Parameter	Symbol	MSM5118160 F-50		MSM5118160 F-60		MSM5118160 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Row Address Hold Time	t _{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	11
Column Address Hold Time	t _{CAH}	7	—	10	—	15	—	ns	11
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	25	—	30	—	35	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	11
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	8, 11
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	9, 11
Write Command Hold Time	t _{WCH}	7	—	10	—	15	—	ns	11
Write Command Pulse Width	t _{WP}	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	13	—	15	—	20	—	ns	13
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	10, 11
Data-in Hold Time	t _{DH}	7	—	10	—	15	—	ns	10, 11
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	36	—	40	—	50	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	48	—	55	—	65	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	73	—	85	—	100	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	53	—	60	—	70	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	5	—	5	—	5	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	5	—	5	—	5	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	10	—	10	—	ns	12

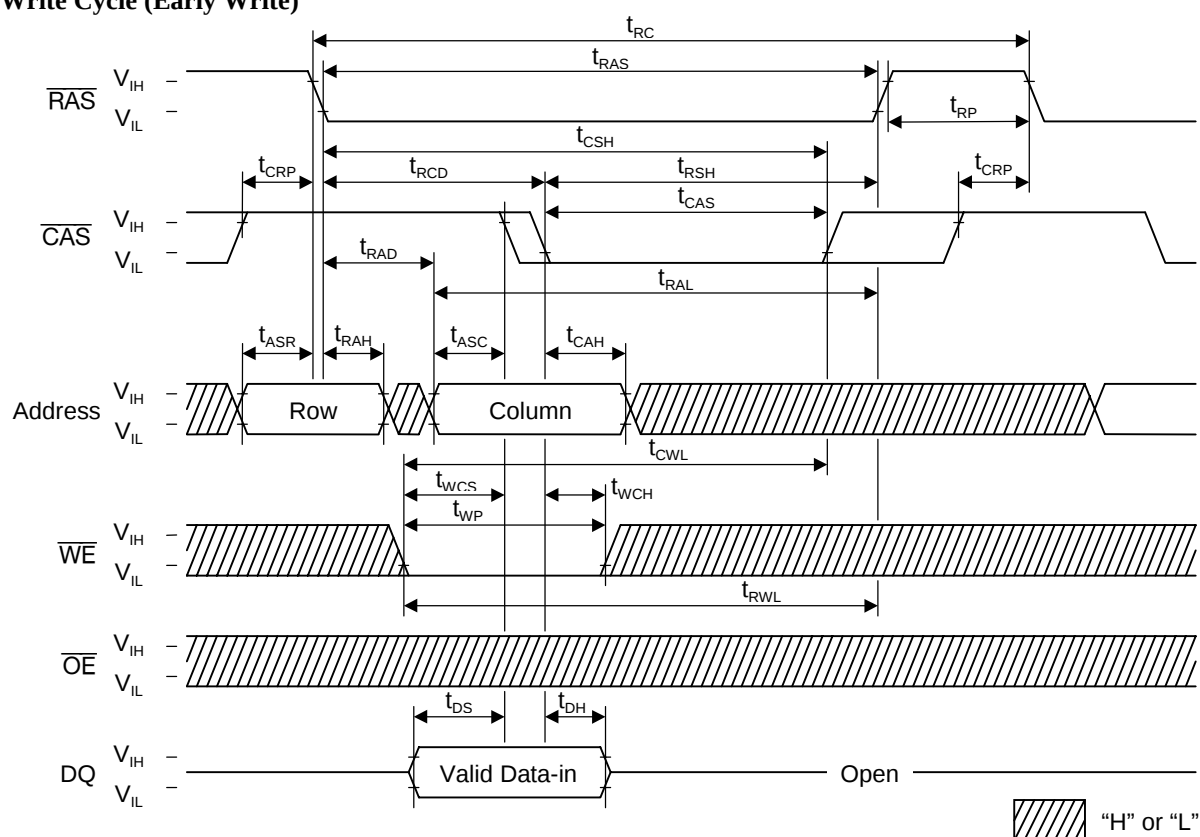
- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5\text{ns}$.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. -50 is measured with a load circuit equivalent to 2 TTL load and 50pF, and -60/-70 is measured with a load circuit equivalent to 2 TTL load and 100pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{Min.})$, then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{Min.})$, $t_{RWD} \geq t_{RWD}(\text{Min.})$, $t_{AWD} \geq t_{AWD}(\text{Min.})$ and $t_{CPWD} \geq t_{CPWD}(\text{Min.})$, then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 10. These parameters are referenced to the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$, leading edges in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 11. These parameters are determined by the falling edge of either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is earlier.
 12. These parameters are determined by the rising edge of either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is later.
 13. t_{CWL} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 14. t_{CP} is determined by the time both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.

TIMING CHART

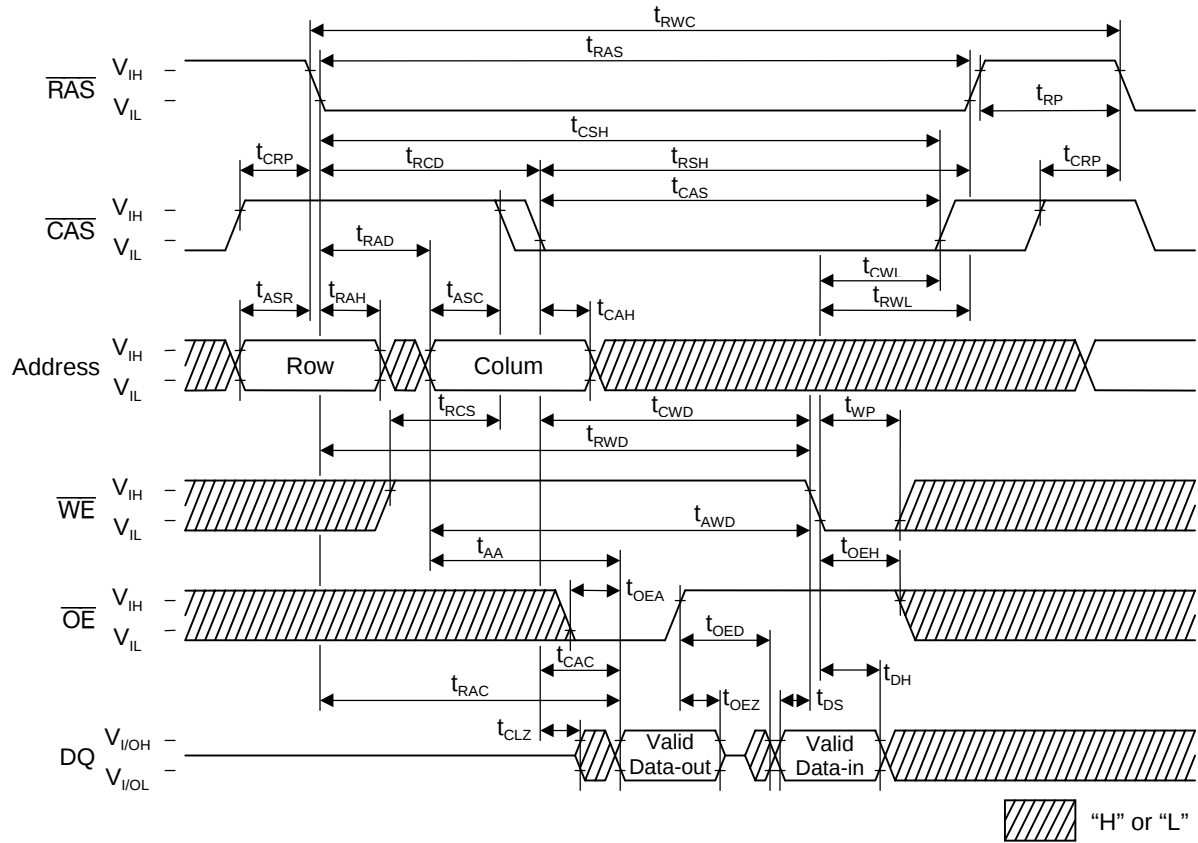
Read Cycle



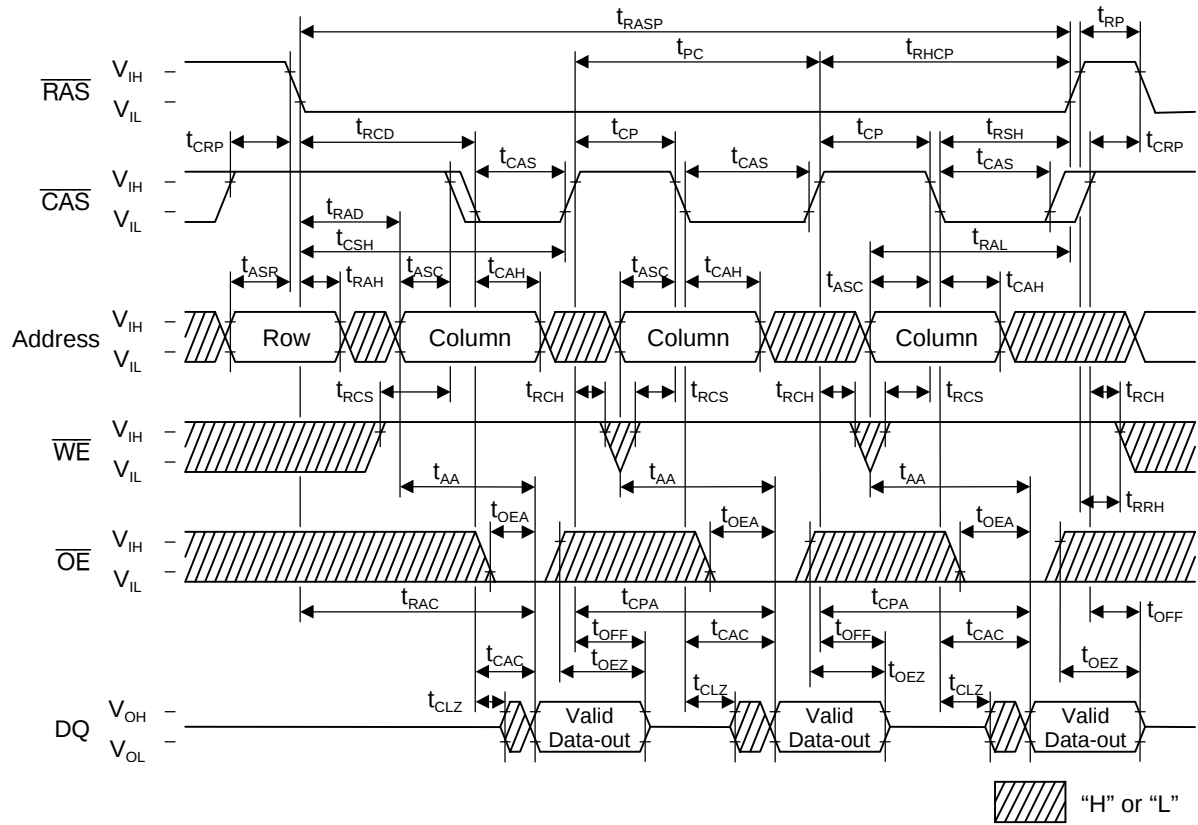
Write Cycle (Early Write)



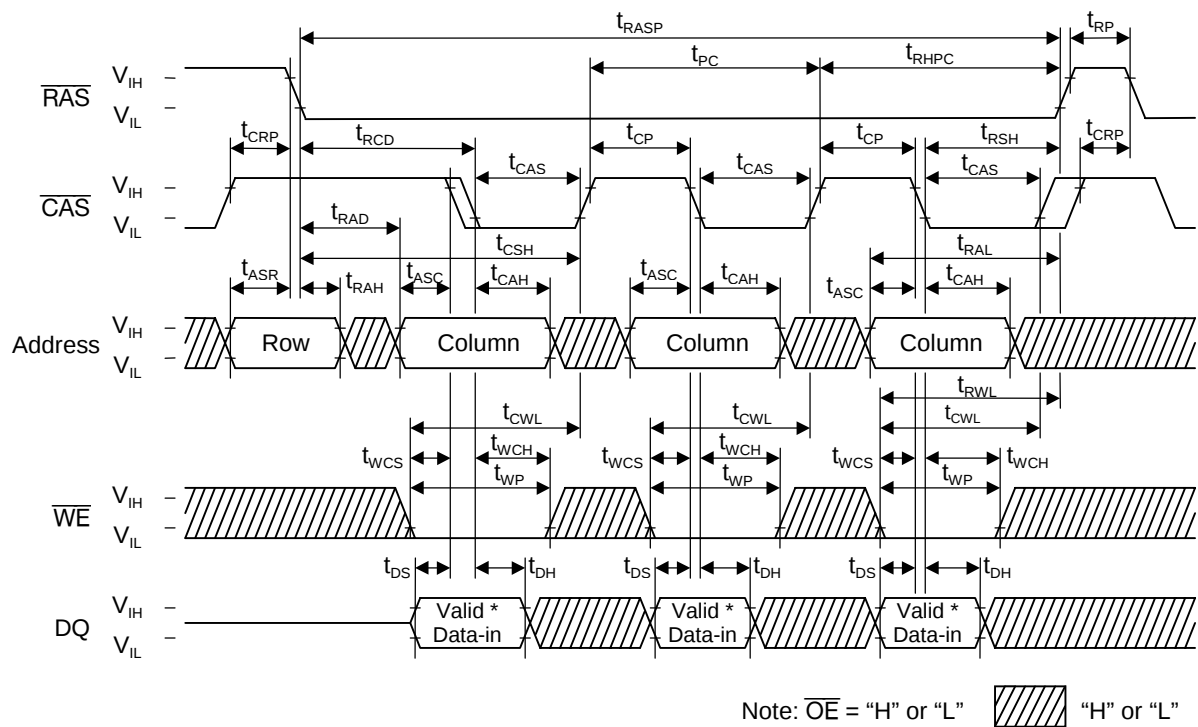
Read Modify Write Cycle



Fast Page Mode Write Cycle



Fast Page Mode Write Cycle (Early Write)

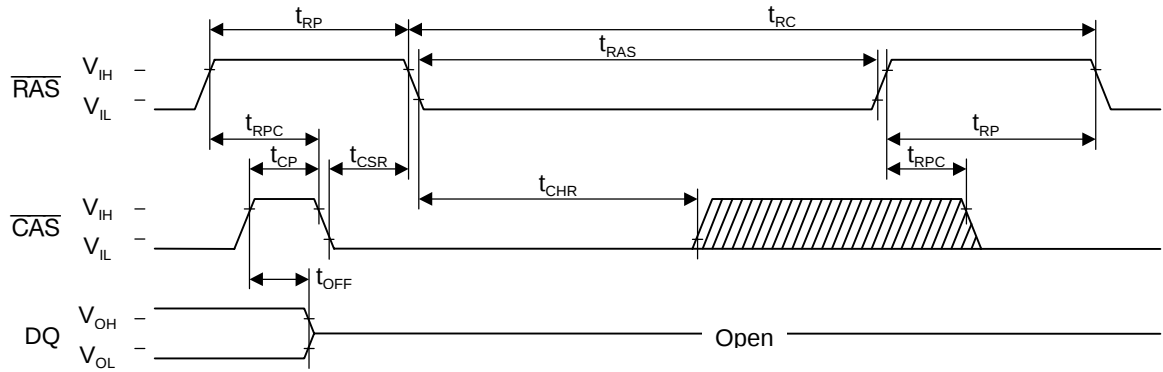


Note: In = Valid Data-in, Out = Valid Data-out  "H" or "L"

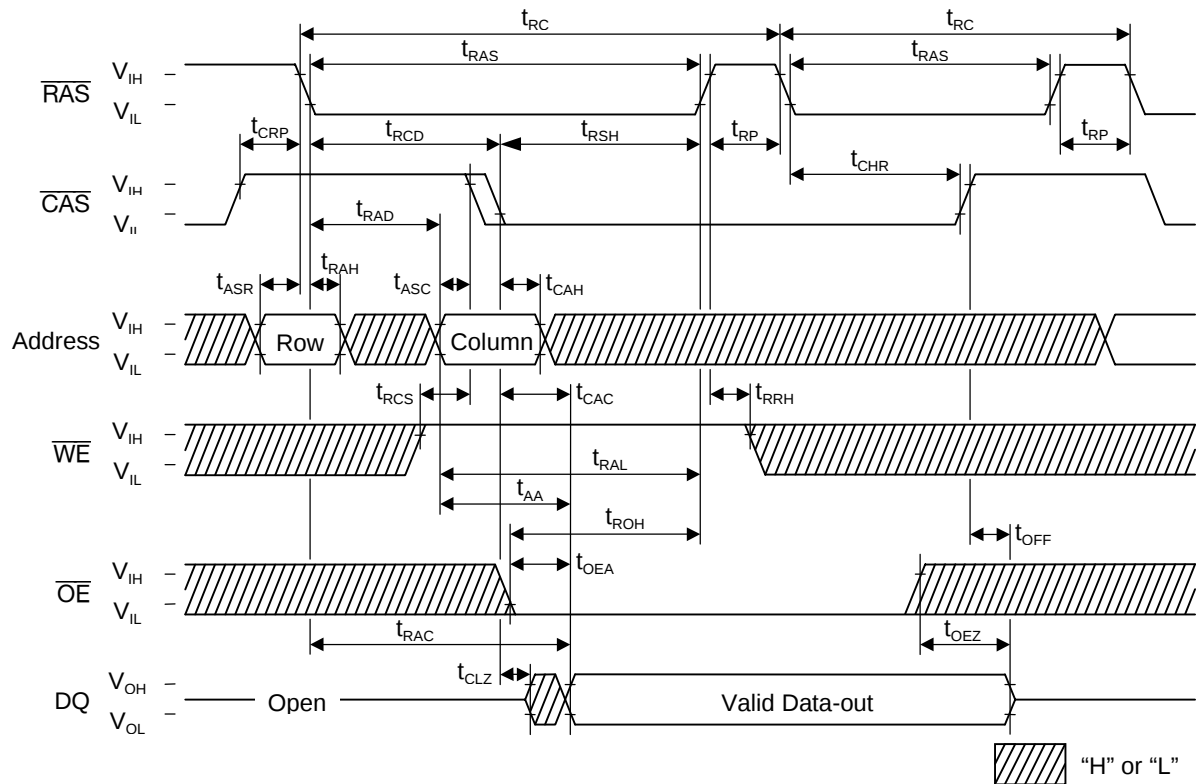
The diagram illustrates the timing relationships for a memory access cycle. The signals and their timing parameters are as follows:

- RAS:**
 - t_{RAS} : RAS pulse width (from V_{IH} to V_{IL}).
 - t_{RC} : RAS to CAS delay (from RAS falling edge to CAS falling edge).
 - t_{RP} : RAS precharge time (from RAS rising edge to next RAS falling edge).
 - t_{CRP} : RAS to CAS precharge time (from RAS falling edge to CAS falling edge).
 - t_{RPC} : RAS precharge to CAS delay (from RAS rising edge to CAS falling edge).
- CAS:**
 - t_{ASR} : CAS to Row Address Strobe delay (from CAS falling edge to Row Address Strobe rising edge).
 - t_{RAH} : CAS to Row Address Hold delay (from CAS falling edge to Row Address Strobe falling edge).
- Address:**
 - t_{OFF} : Address to Data Output delay (from Address falling edge to Data Output rising edge).
- DQ:**
 - V_{OH} and V_{OL} : Data Output high and low levels.
 - Open**: Data Output is in high-impedance state.

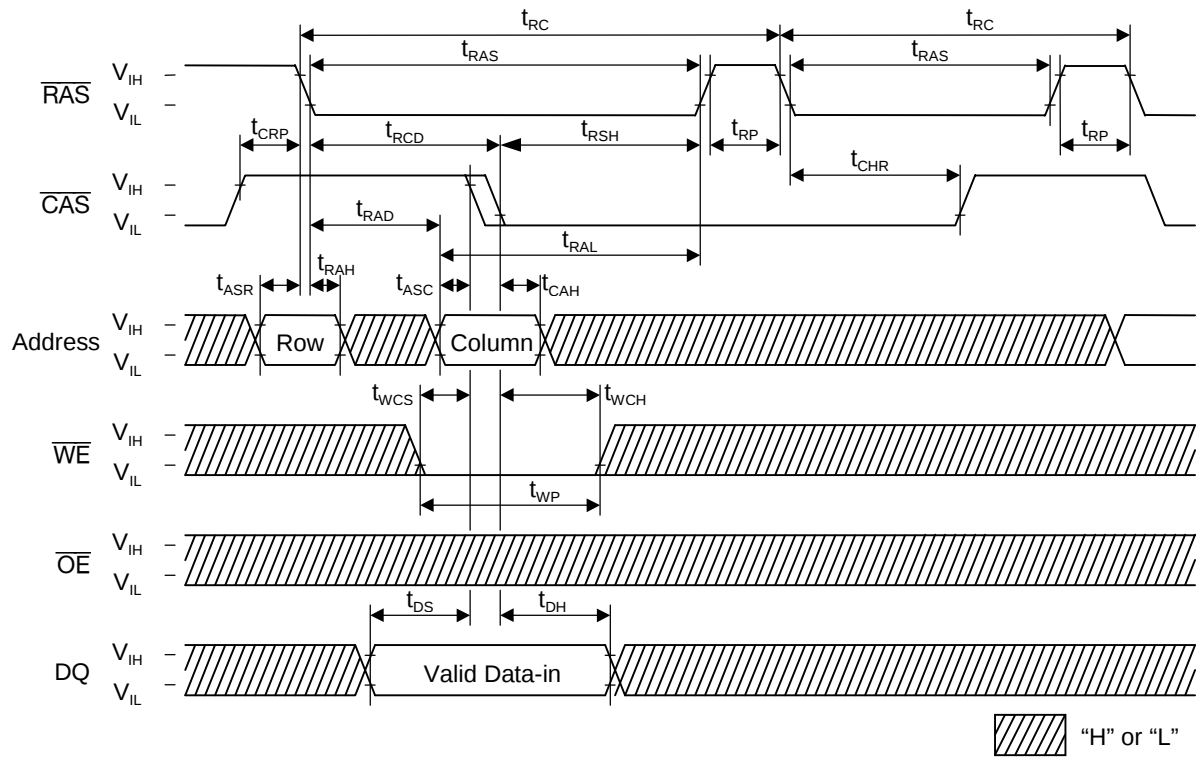
Note: $\overline{WE}$, $\overline{OE}$ = "H" or "L"  "H" or "L"

CAS before RAS Refresh Cycle

Note: $\overline{WE}$, $\overline{OE}$, Address = "H" or "L"  "H" or "L"

Hidden Refresh Read Cycle

 "H" or "L"

Hidden Refresh Write Cycle

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
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