Data Sheet April 1999 File Number 2925.4

Dual and Quad, 8MHz and 60MHz, Low Noise Operational Amplifiers

Low noise and high performance are key words describing HA-5102, HA-5104 and HA-5114. These general purpose amplifiers offer an array of dynamic specifications ranging from a 3V/µs slew rate and 8MHz bandwidth (5102/04) to 20V/µs slew rate and 60MHz gain-bandwidth-product (HA-5114). Complementing these outstanding parameters is a very low noise specification of 4.3nV/$\sqrt{Hz}$ at 1kHz.

Fabricated using the Intersil high frequency DI process, these operational amplifiers also offer excellent input specifications such as a 0.5mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 60dB channel separation. Consuming a very modest amount of power (90mW/package for duals and 150mW/package for quads), HA-5102/04/14 also provide 15mA of output current.

This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

These operational amplifiers are available in dual or quad form with industry standard pinouts allowing for immediate interchangeability with most other dual and quad operational amplifiers.

HA-5102	Dual, Comp.	HA-5104	Quad, Comp.
HA-5114	Quad, Uncomp.		

Refer to the /883 data sheet for military product.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO
HA3-5102-5	0 to 75	8 Ld PDIP	E8.3
HA7-5102-2	-55 to 125	8 Ld CERDIP	F8.3A
HA1-5104-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-5104-5	0 to 75	14 Ld CERDIP	F14.3
HA3-5104-5	0 to 75	14 Ld PDIP	E14.3
HA9P5104-9	-40 to 85	16 Ld SOIC	M16.3
HA3-5114-5	0 to 75	14 Ld PDIP	E14.3
HA9P5114-9	-40 to 85	16 Ld SOIC	M16.3

Features

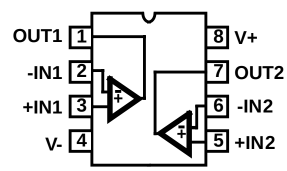
- Low Noise. . . . . 4.3nV/$\sqrt{Hz}$
- Bandwidth. 8MHz (Compensated) 60MHz (Uncompensated)
- Slew Rate . . . . 3V/µs (Compensated) 20V/µs (Uncompensated)
- Low Offset Voltage 0.5mV
- Available in Duals or Quads

Applications

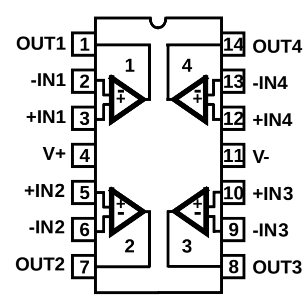
- High Q, Active Filters
- Audio Amplifiers
- Instrumentation Amplifiers
- Integrators
- Signal Generators
- For Further Design Ideas, See Application Note AN554

Pinouts

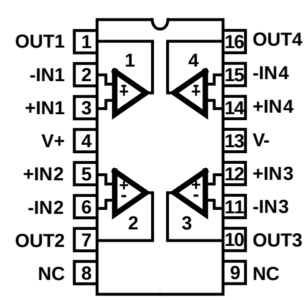
HA-5102 (PDIP, CERDIP)
TOP VIEW



HA-5104 (PDIP, CERDIP)
HA-5114 (PDIP)
TOP VIEW



HA5104/5114 (SOIC)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals. 40V
Differential Input Voltage 7V
Input Voltage . . . . $\pm V_{SUPPLY}$
Output Short Circuit Duration (Note 3). . . . . Indefinite

Operating Conditions

Temperature Range
HA-5102/5104-2. . . . . -55°C to 125°C
HA-5102/5104/5114-5 . . . . 0°C to 75°C
HA-5104/5114-9. . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Lead PDIP Package	92	N/A
8 Lead CERDIP Package	135	50
14 Lead CERDIP Package	80	30
14 Lead PDIP Package	86	N/A
SOIC Package (HA-5104, HA-5114)	96	N/A

Maximum Junction Temperature (Note 1, Hermetic Package) . .175°C
Maximum Junction Temperature (Plastic Package) . . . . .150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below 175°C for hermetic packages, and below 150°C for plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. Any one amplifier may be shorted to ground indefinitely.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, Unless Otherwise Specified

PARAMETER		TEMP. (°C)	HA-5102-2, -5			HA-5104-2, -5 HA-5114 -5			HA-5104-9 HA-5114-9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS												
Offset Voltage		25	-	0.5	2.0	-	0.5	2.5	-	0.5	2.5	mV
		Full	-	-	2.5	-	-	3.0	-	-	3.0	mV
Offset Voltage Average Drift		Full	-	3	-	-	3	-	-	3	-	µV/°C
Bias Current		25	-	130	200	-	130	200	-	130	200	nA
		Full	-	-	325	-	-	325	-	-	500	nA
Offset Current		25	-	30	75	-	30	75	-	30	75	nA
		Full	-	-	125	-	-	125	-	-	125	nA
Input Resistance		25	-	500	-	-	500	-	-	500	-	kΩ
Common Mode Range		Full	±12	-	-	±12	-	-	±12	-	-	V
TRANSFER CHARACTERISTICS												
Large Signal Voltage Gain, ($V_{OUT} = \pm5V$, $R_L = 2k\Omega$)		25	100	250	-	100	250	-	80	250	-	kV/V
		Full	100	-	-	100	-	-	80	-	-	kV/V
Common Mode Rejection Ratio ($V_{CM} = \pm5.0V$)		Full	86	95	-	86	95	-	80	95	-	dB
Small Signal Bandwidth, HA-5102/5104 ($A_V = 1$)		25	-	8	-	-	8	-	-	8	-	MHz
Gain Bandwidth Product, HA-5114 ($A_V = 10$)		25	-	60	-	-	60	-	-	60	-	MHz
Channel Separation (Note 4)		25	-	60	-	-	60	-	-	60	-	dB
OUTPUT CHARACTERISTICS												
Output Voltage Swing	($R_L = 10k\Omega$)	Full	±12	±13	-	±12	±13	-	±12	±13	-	V
	($R_L = 2k\Omega$)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current, ($V_{OUT} = \pm5V$)		Full	±10	±15	-	±10	±15	-	±7	±15	-	mA
Full Power Bandwidth (Note 5)	HA-5102/5104	25	16	47	-	16	47	-	16	47	-	kHz
	HA-5114	25	191	318	-	191	318	-	191	318	-	kHz

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

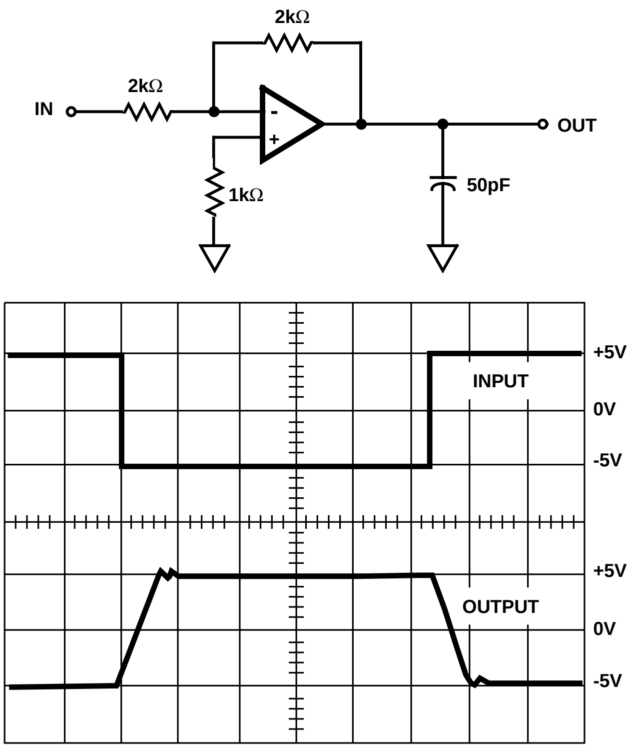
PARAMETER		TEMP. (°C)	HA-5102-2, -5 MIN	HA-5102-2, -5 TYP	HA-5102-2, -5 MAX	HA-5104-2, -5 HA-5114 -5 MIN	HA-5104-2, -5 HA-5114 -5 TYP	HA-5104-2, -5 HA-5114 -5 MAX	HA-5104-9 HA-5114-9 MIN	HA-5104-9 HA-5114-9 TYP	HA-5104-9 HA-5114-9 MAX	UNITS
Output Resistance		25	-	110	-	-	110	-	-	110	-	Ω
STABILITY												
Minimum Stable Closed Loop Gain	HA-5102/5104	Full	1	-	-	1	-	-	1	-	-	V/V
	HA-5114	Full	10	-	-	10	-	-	10	-	-	V/V
TRANSIENT RESPONSE (Note 6)												
Rise Time	HA-5102/5104	25	-	108	200	-	108	200	-	108	200	ns
	HA-5114	25	-	48	100	-	48	100	-	48	100	ns
Overshoot	HA-5102/5104	25	-	20	35	-	20	35	-	20	35	%
	HA-5114	25	-	30	40	-	30	40	-	30	40	%
Slew Rate	HA-5102/5104	25	1	3	-	1	3	-	1	3	-	V/µs
	HA-5114	25	12	20	-	12	20	-	12	20	-	V/µs
Settling Time (Note 7)	HA-5102/5104	25	-	4.5	-	-	4.5	-	-	4.5	-	µs
	HA-5114	25	-	0.6	-	-	0.6	-	-	0.6	-	µs
NOISE CHARACTERISTICS (Note 8)												
Input Noise Voltage	f = 10Hz	25	-	9	25	-	9	25	-	9	25	$nV/\sqrt{Hz}$
	f = 1kHz	25	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	$nV/\sqrt{Hz}$
Input Noise Current	f = 10Hz	25	-	5.1	15	-	5.1	15	-	5.1	15	$pA/\sqrt{Hz}$
	f = 1kHz	25	-	0.57	3	-	0.57	3	-	0.57	3	$pA/\sqrt{Hz}$
Broadband Noise Voltage	f = DC to 30kHz	25	-	870	-	-	870	-	-	870	-	nV_{RMS}
POWER SUPPLY CHARACTERISTICS												
Supply Current (All Amps)		25	-	3.0	5.0	-	5.0	6.5	-	5.0	6.5	mA
Power Supply Rejection Ratio, (ΔV_S = ±5V)		Full	86	100	-	86	100	-	80	100	-	dB

NOTES:

4. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 100mV_{PEAK}; R_S = 1kΩ.
5. Full power bandwidth is guaranteed by equation: Full power bandwidth $= \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
6. Refer to Test Circuits section of the data sheet.
7. Settling time is measured to 0.1% of final value for a 1V input step, and A_V = -10 for HA-5114, and a 10V input step, A_V = -1 for HA-5102/5104.
8. The limits for these parameters are guaranteed based on lab characterization, and reflect lot-to-lot variation.

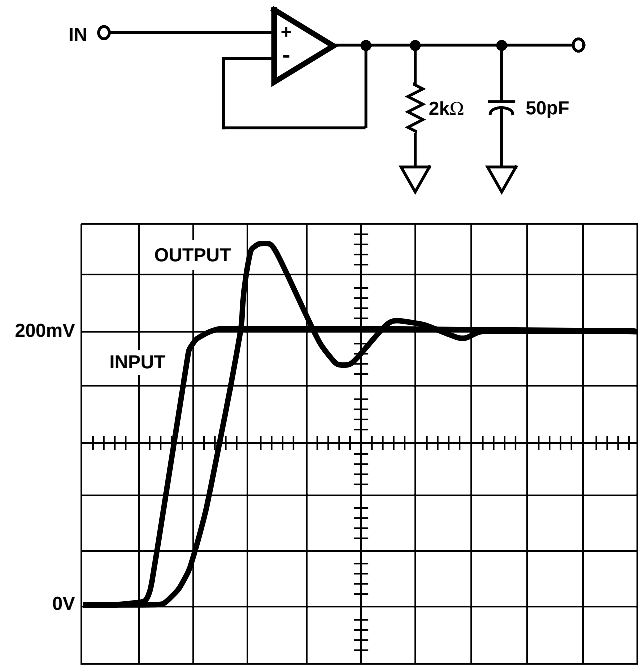
Test Circuits and Waveforms

HA-5102, HA-5104



Vertical = 5V/Div., Horizontal = 5µs/Div. (A_V = -1)

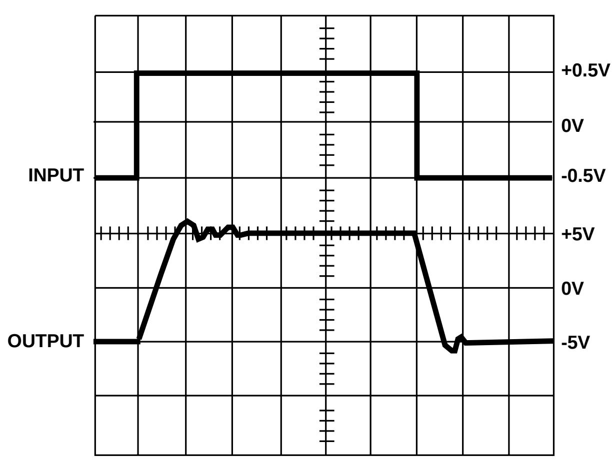
FIGURE 1. LARGE SIGNAL RESPONSE CIRCUIT



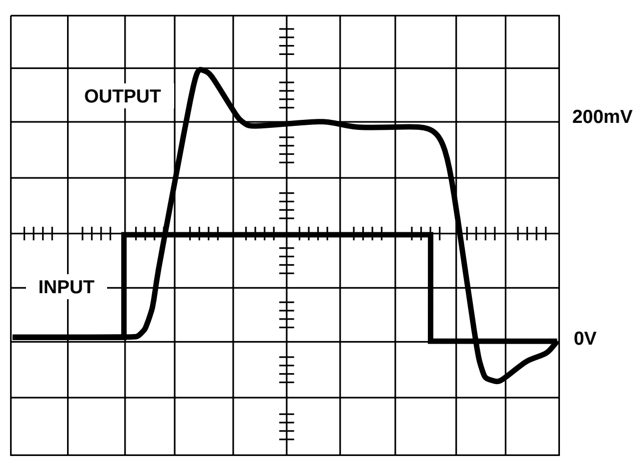
Vertical = 40mV/Div., Horizontal = 50ns/Div. (A_V = +1)

FIGURE 2. SMALL SIGNAL RESPONSE CIRCUIT

HA-5114

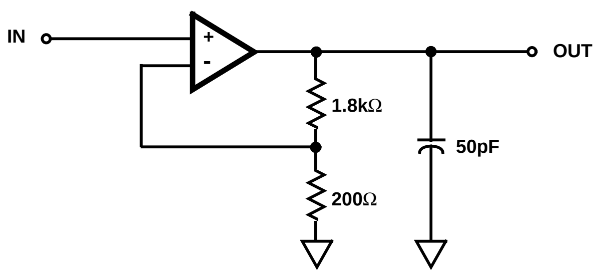


Input = 0.5V/Div., Output = 5V/Div., Time = 500ns/Div.



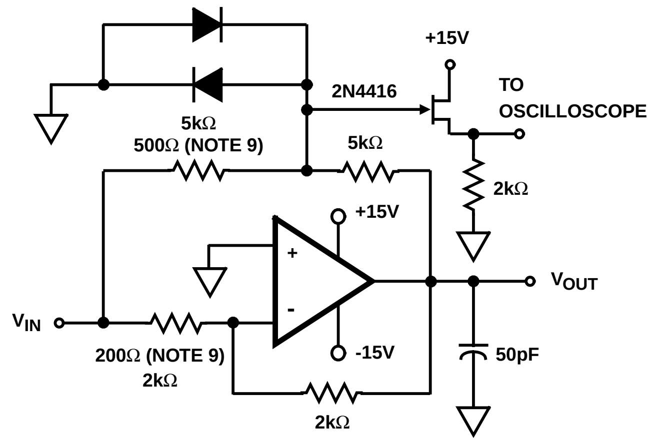
Input = 10mV/Div., Output = 50mV/Div., Time = 50ns/Div.

Test Circuits and Waveforms (Continued)



NOTE: A_V = +10.

FIGURE 3. LARGE AND SMALL SIGNAL RESPONSE CIRCUIT (A_V = +10)

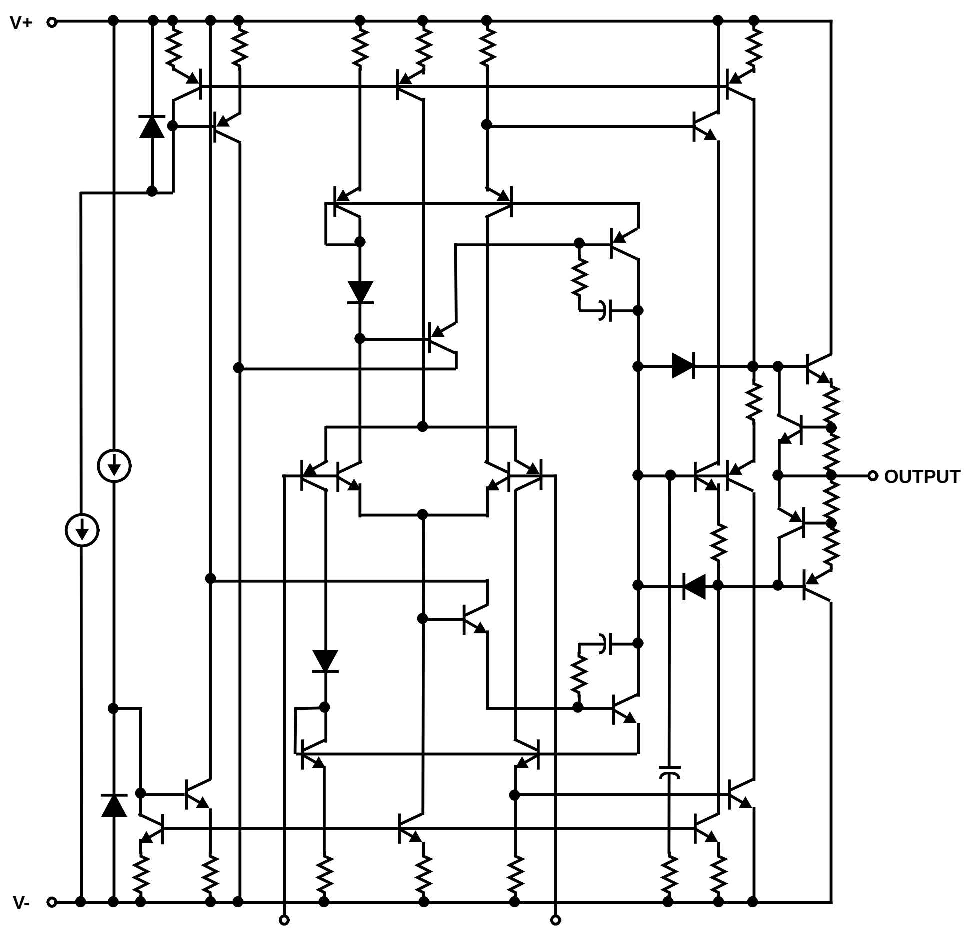


NOTES:

9. A_V = -1 (HA-5102/5104), A_V = -10 (HA-5114).
10. Feedback and summing resistors should be 0.1% matched.
11. Clipping diodes are optional, HP5082-2810 recommended.

FIGURE 4. SETTLING TIME CIRCUIT

Simplified Schematic



Typical Performance Curves

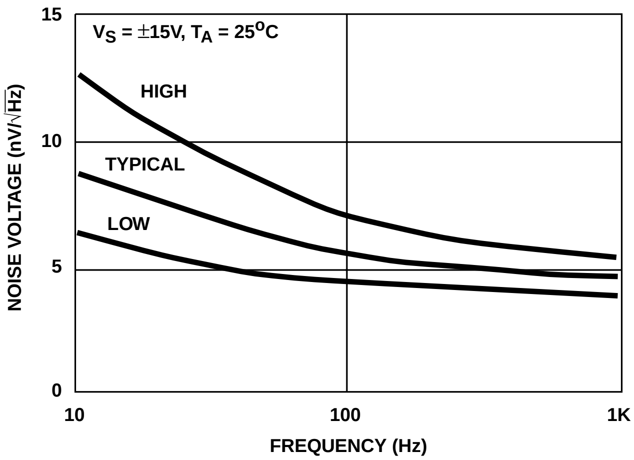


FIGURE 5. INPUT NOISE VOLTAGE DENSITY

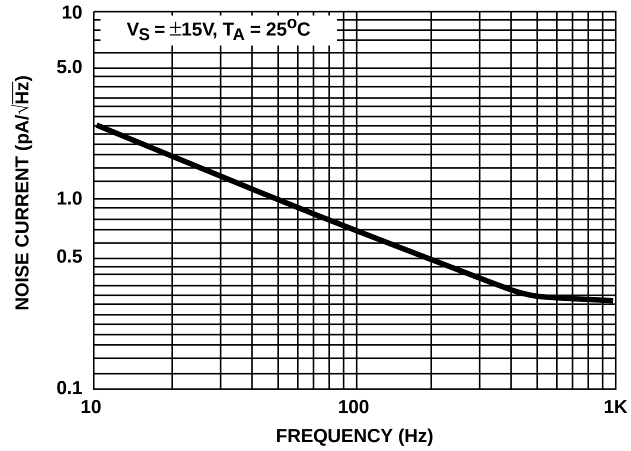
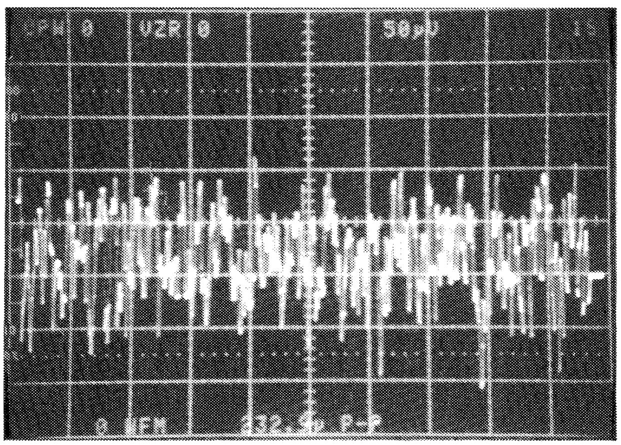
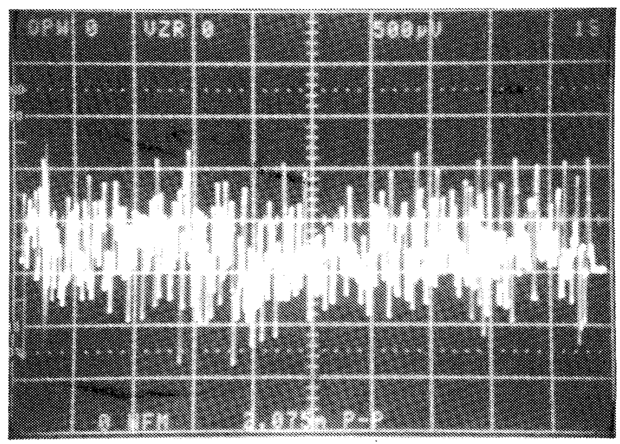


FIGURE 6. INPUT NOISE CURRENT DENSITY



$V_S = \pm15V$, $T_A = 25^oC$, 50μV/Div., 1s/Div., A_V = 1000V/V
Input Noise = 0.232μV_{P-P}
FIGURE 7. 0.1Hz TO 10Hz NOISE



$V_S = \pm15V$, $T_A = 25^oC$, 500μV/Div., 1s/Div., A_V = 1000V/V
Total Output Noise = 2.075μV_{P-P}
FIGURE 8. 0.1Hz TO 1MHz NOISE

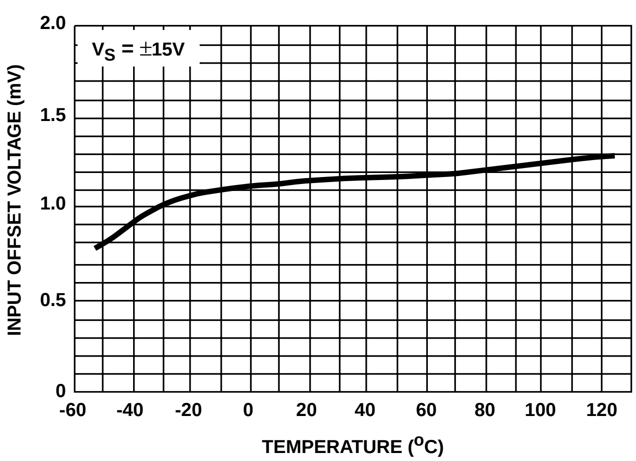


FIGURE 9. V_{IO} vs TEMPERATURE

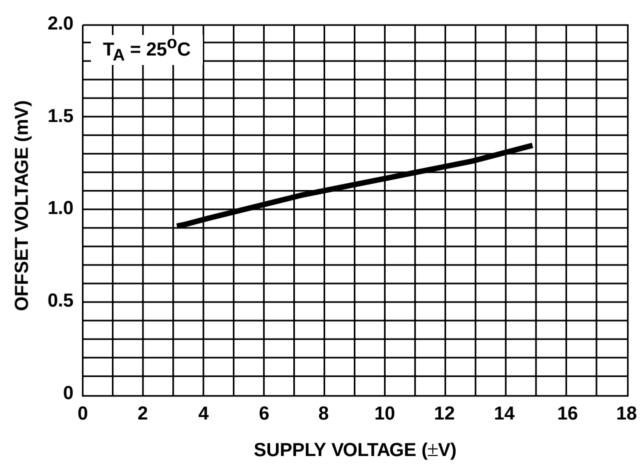


FIGURE 10. V_{IO} vs V_S

Typical Performance Curves (Continued)

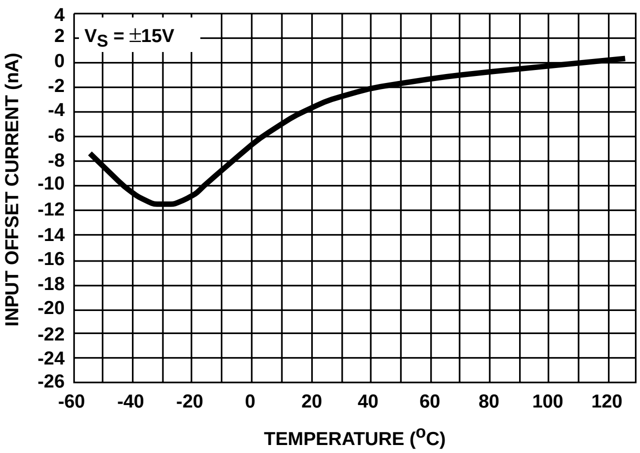


FIGURE 11. I_{IO} vs TEMPERATURE

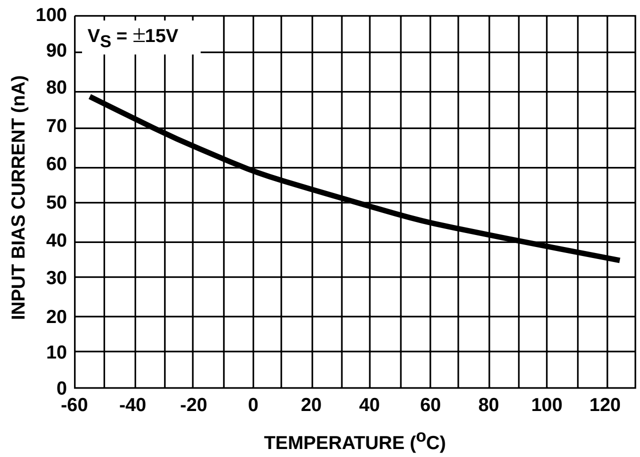


FIGURE 12. I_{BIAS} vs TEMPERATURE

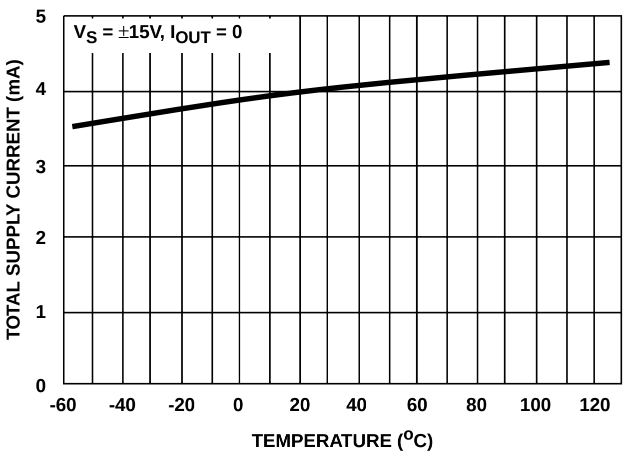


FIGURE 13. I_{CC} vs TEMPERATURE (HA-5104/14)

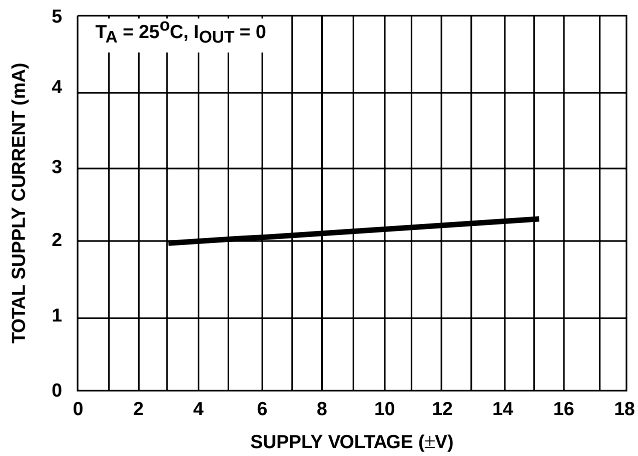


FIGURE 14. I_{CC} vs V_S (HA-5102)

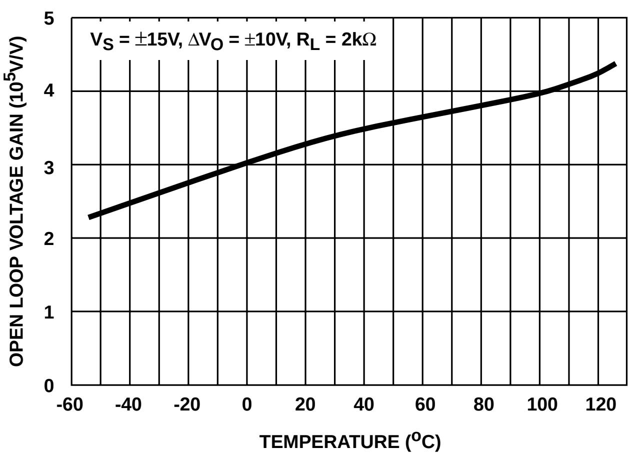


FIGURE 15. A_{VOL} vs TEMPERATURE

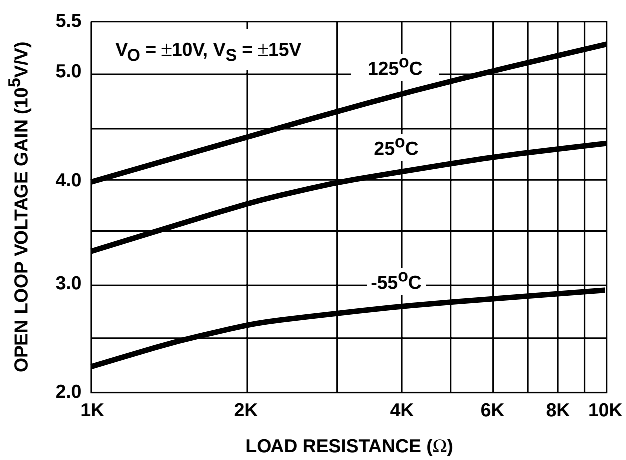


FIGURE 16. A_{VOL} vs LOAD RESISTANCE

Typical Performance Curves (Continued)

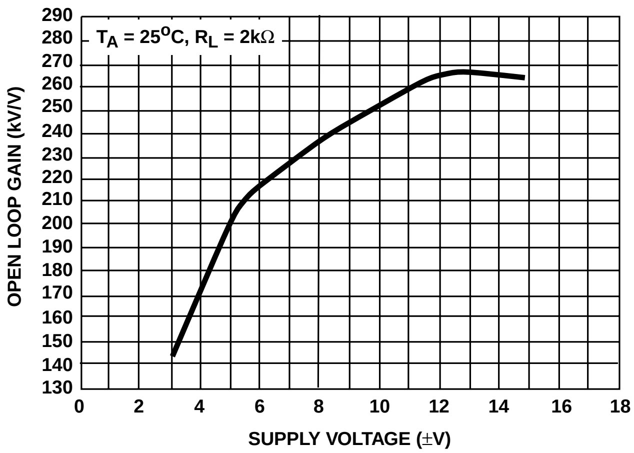


FIGURE 17. A_{VOL} vs V_S

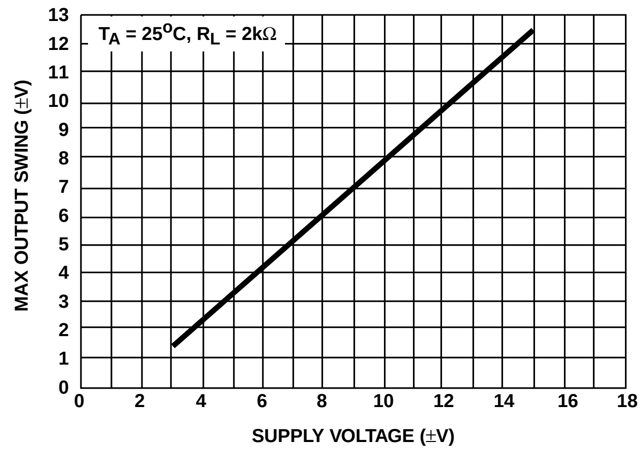


FIGURE 18. V_{OUT} vs V_S

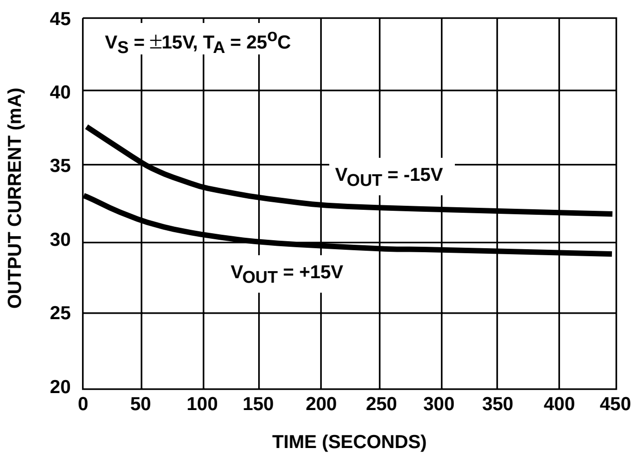


FIGURE 19. OUTPUT SHORT CIRCUIT CURRENT vs TIME

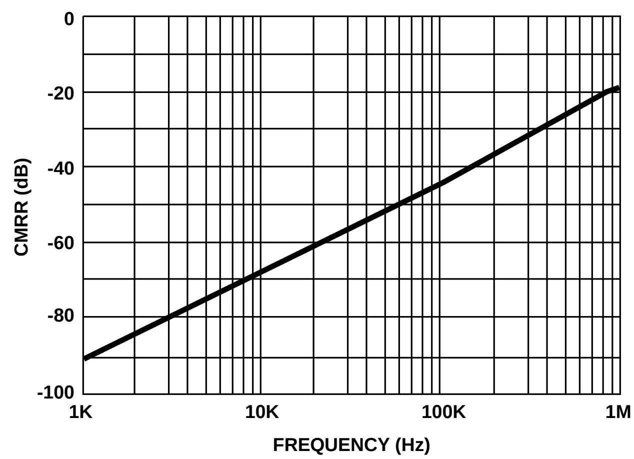


FIGURE 20. CMRR vs FREQUENCY

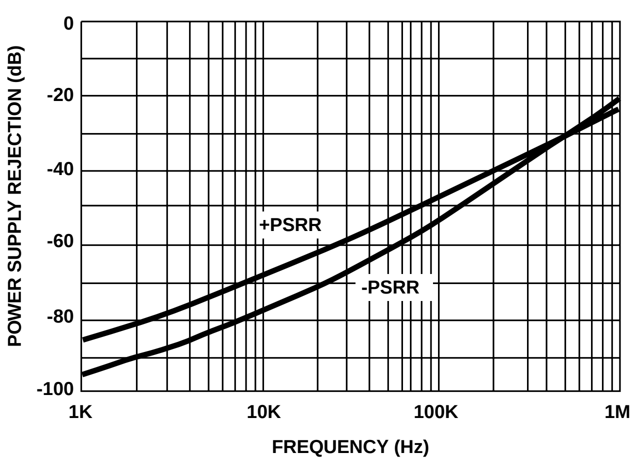


FIGURE 21. PSRR vs FREQUENCY

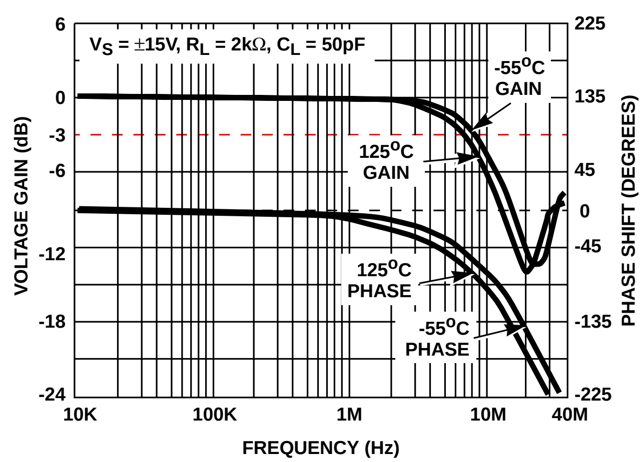


FIGURE 22. HA-5104/02 UNITY GAIN FREQUENCY RESPONSE

Typical Performance Curves (Continued)

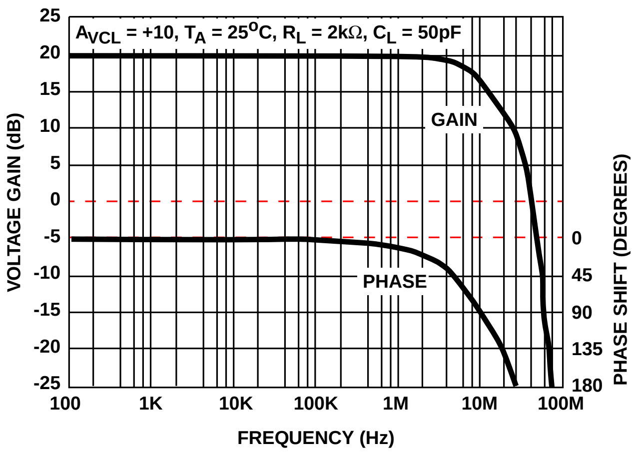


FIGURE 23. HA-5114 FREQUENCY RESPONSE

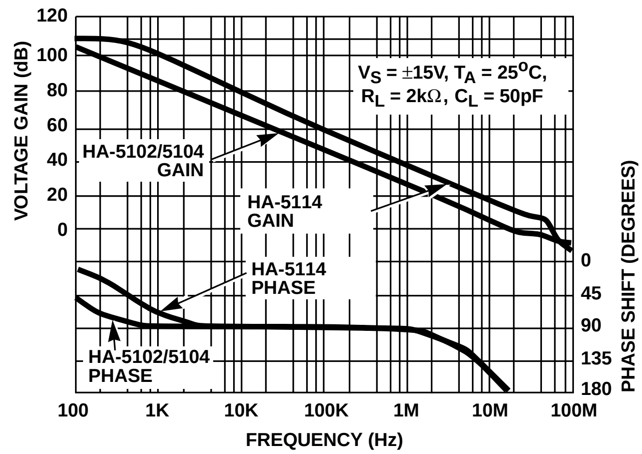


FIGURE 24. OPEN LOOP GAIN vs FREQUENCY

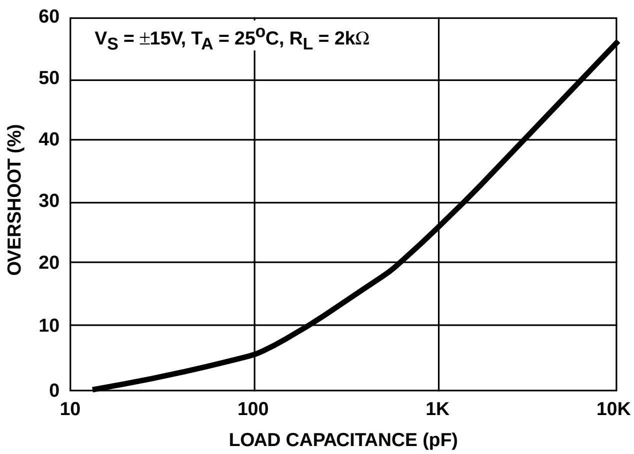


FIGURE 25. SMALL SIGNAL OVERSHOOT vs C_{LOAD}

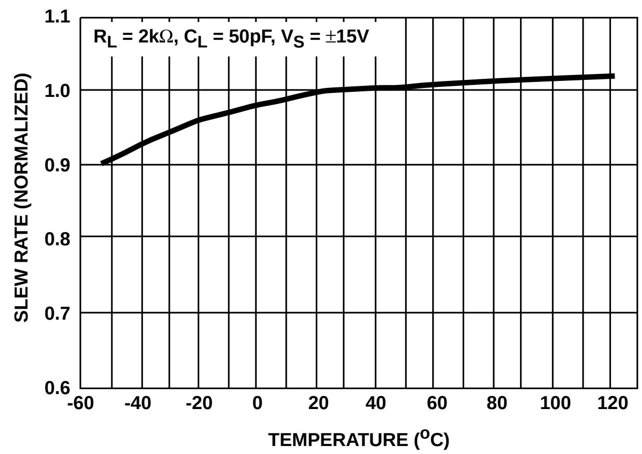


FIGURE 26. SLEW RATE vs TEMPERATURE

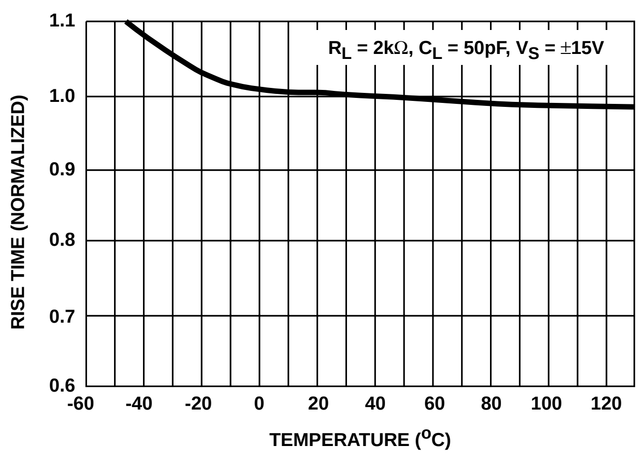


FIGURE 27. RISE TIME vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

98.4 mils x 67.3 mils x 19 mils
2500µm x 1710µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (POWERED UP):

Unbiased

TRANSISTOR COUNT:

93

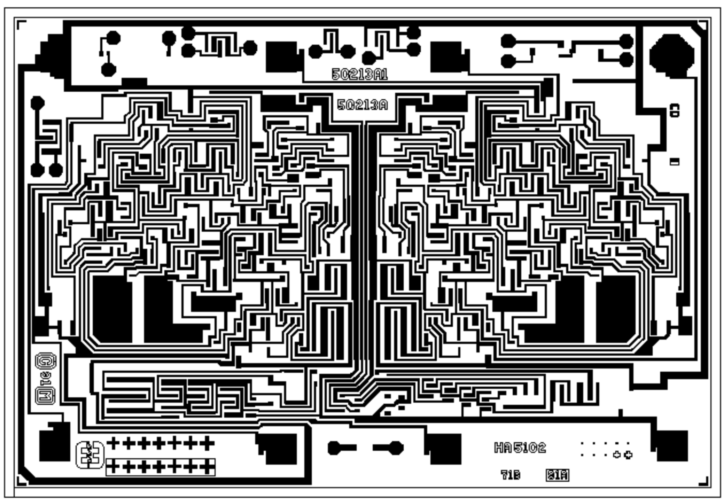
PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5102

V-   +IN1   -IN1   OUT1



+IN2   -IN2   OUT2   V+

Die Characteristics

DIE DIMENSIONS:

95 mils x 99 mils x 19 mils
2420μm x 2530μm x 483μm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (POWERED UP):

Unbiased

TRANSISTOR COUNT:

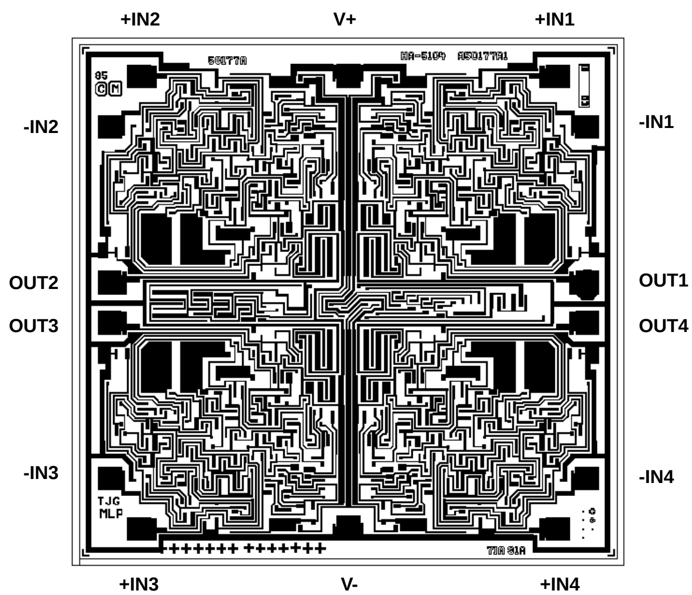
175

PROCESS:

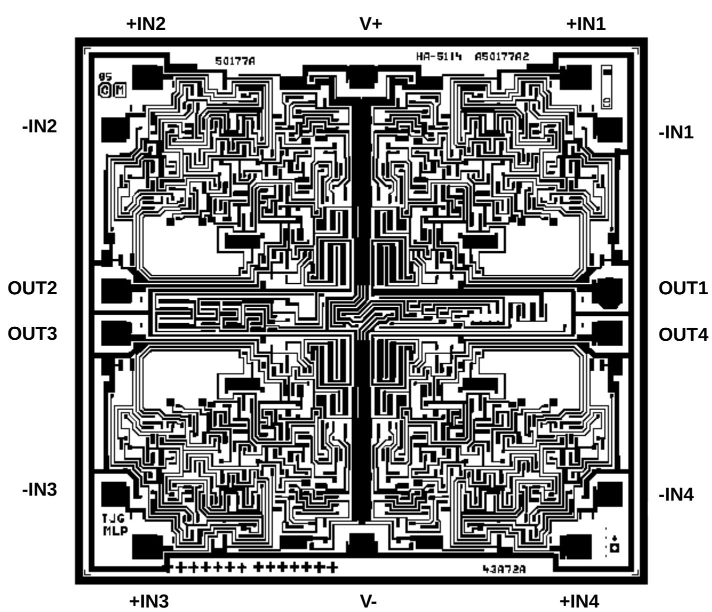
Bipolar Dielectric Isolation

Metallization Mask Layout

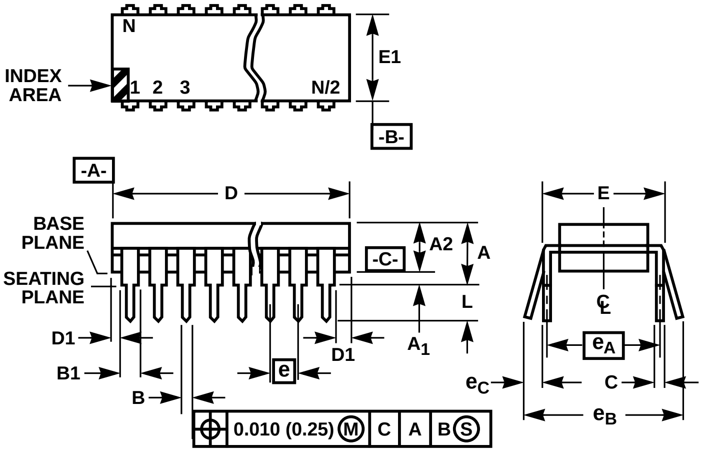
HA-5104



HA-5114



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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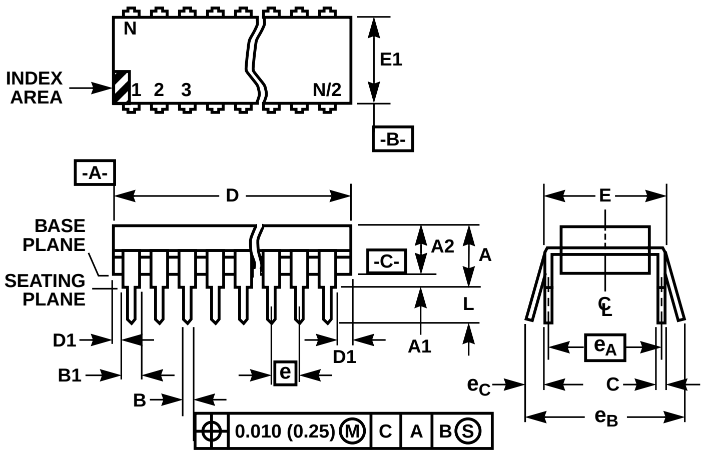
Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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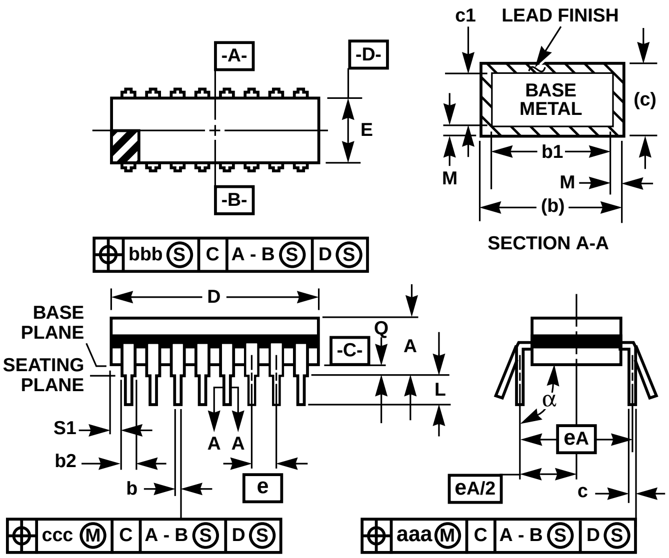
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

F8.3A **MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)**
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

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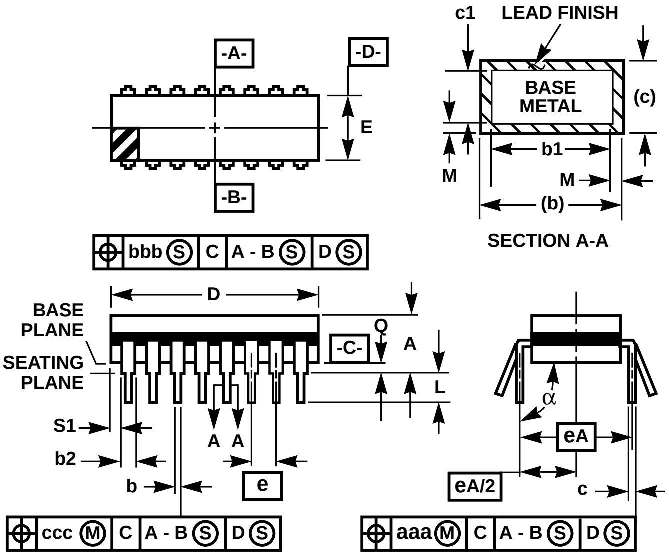
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F14.3 **MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)**
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

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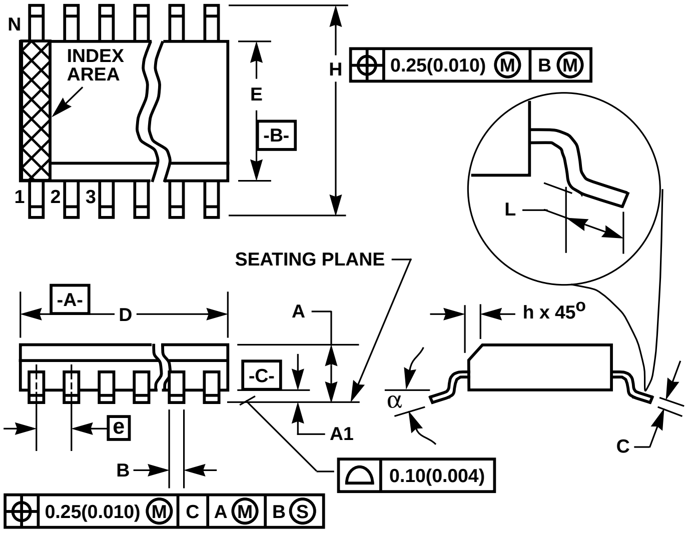
Small Outline Plastic Packages (SOIC)



M16.3 **(JEDEC MS-013-AA ISSUE C)**
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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