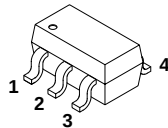


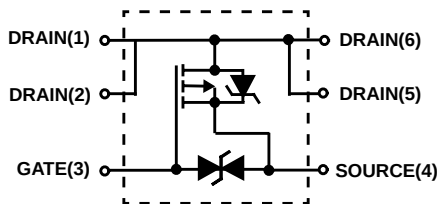
**3A, 20V, 0.115 Ohm, P-Channel,
2.5V Specified Power MOSFET**

Packaging

TSOP-6



Symbol



Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.115\Omega$, $V_{GS} = -4.5V$
 - $r_{DS(ON)} = 0.120\Omega$, $V_{GS} = -4.0V$
 - $r_{DS(ON)} = 0.190\Omega$, $V_{GS} = -2.5V$
- 2.5 V Gate Drive Capability
- Small Profile Package
- Gate to Source Protection Diode
- Simulation Models
 - Temperature Compensated PSPICE™ and SABER Electrical Models
 - Spice and SABER Thermal Impedance Models
 - www.intersil.com
- Peak Current vs Pulse Width Curve
- Transient Thermal Impedance Curve vs Board Mounting Area
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
ITF87052SVT	TSOP-6 (SC-95)	052

NOTE: When ordering, use the entire part number. ITF87052SVT is available only in tape and reel.

Absolute Maximum Ratings $T_A = 25^\circ C$, Unless Otherwise Specified

	ITF87052SVT	UNITS
Drain to Source Voltage (Note 1)	-20	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	-20	V
Gate to Source Voltage	-12/+6	V
Drain Current		
Continuous ($T_A = 25^\circ C$, $V_{GS} = -4.5V$) (Note 2)	3.0	A
Continuous ($T_A = 25^\circ C$, $V_{GS} = -4.0V$) (Note 2)	3.0	A
Continuous ($T_A = 100^\circ C$, $V_{GS} = -4.0V$) (Note 2)	1.5	A
Continuous ($T_A = 100^\circ C$, $V_{GS} = -2.5V$) (Note 2)	1.5	A
Pulsed Drain Current	Figure 4	
Power Dissipation (Note 2)	2.0	W
Derate Above $25^\circ C$	16	mW/ $^\circ C$
Operating and Storage Temperature	-55 to 150	$^\circ C$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	300	$^\circ C$
Package Body for 10s, See Techbrief TB370.	260	$^\circ C$

NOTES:

1. $T_J = 25^\circ C$ to $125^\circ C$.
2. 62.5 $^\circ C/W$ measured using FR-4 board with 0.40 in² (258.1 mm²) copper pad at 2 second.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_A = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V Figure 11	-20	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20V, V _{GS} = 0V	-	-	-10	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±12V	-	-	±10	μA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA Figure 10	-0.5	-	-1.5	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 3.0A, V _{GS} = -4.5V Figures 8, 9	-	0.080	0.115	Ω	
		I _D = 1.5A, V _{GS} = -4.0V Figure 8	-	0.086	0.120	Ω	
		I _D = 1.5A, V _{GS} = -2.5V Figure 8	-	0.130	0.190	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Ambient	R _{θJA}	Pad Area = 0.40 in ² (258.1 mm ²) (Note 2)	-	-	62.5	°C/W	
		Pad Area = 0.013 in ² (8.6 mm ²) Figure 20	-	-	202	°C/W	
		Pad Area = 0.009 in ² (5.8 mm ²) Figure 20	-	-	210	°C/W	
SWITCHING SPECIFICATIONS (V _{GS} = -2.5V)							
Turn-On Delay Time	t _{d(ON)}	V _{DD} = -10V, I _D = 1.5A	-	320	-	ns	
Rise Time	t _r	V _{GS} = -2.5V, R _{GS} = 22Ω	-	1200	-	ns	
Turn-Off Delay Time	t _{d(OFF)}	Figures 14, 18, 19	-	650	-	ns	
Fall Time	t _f		-	820	-	ns	
SWITCHING SPECIFICATIONS (V _{GS} = -4.5V)							
Turn-On Delay Time	t _{d(ON)}	V _{DD} = -10V, I _D = 3.0A	-	130	-	ns	
Rise Time	t _r	V _{GS} = -4.5V, R _{GS} = 19Ω	-	540	-	ns	
Turn-Off Delay Time	t _{d(OFF)}	Figures 15, 18, 19	-	800	-	ns	
Fall Time	t _f		-	860	-	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to -4.5V	V _{DD} = -10V, I _D = 3.0A, I _{g(REF)} = 1.0mA Figures 13, 16, 17	-	8	-	nC
Gate Charge at -2V	Q _{g(-2)}	V _{GS} = 0V to -2V		-	3	-	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to -0.5V		-	0.3	-	nC
Gate to Source Gate Charge	Q _{gs}			-	1	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	2.5	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = -10V, V _{GS} = 0V, f = 1MHz Figure 12	-	540	-	pF	
Output Capacitance	C _{OSS}		-	200	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	120	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = -3.0\text{A}$	-	-0.82	-	V
Reverse Recovery Time	t_{rr}	$I_{SD} = -3.0\text{A}$, $dI_{SD}/dt = 10\text{A}/\mu\text{s}$	-	30	-	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = -3.0\text{A}$, $dI_{SD}/dt = 10\text{A}/\mu\text{s}$	-	2	-	nC

Typical Performance Curves

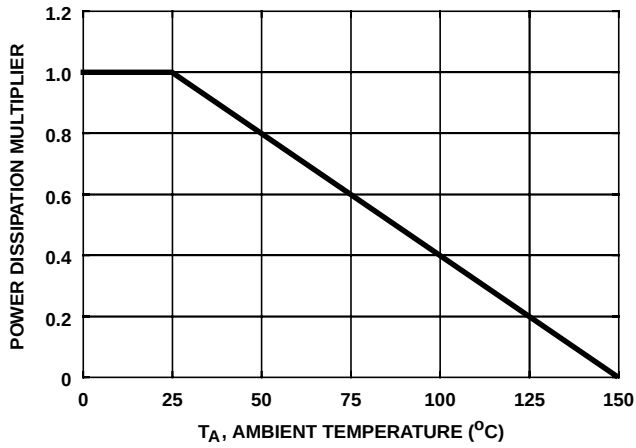


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

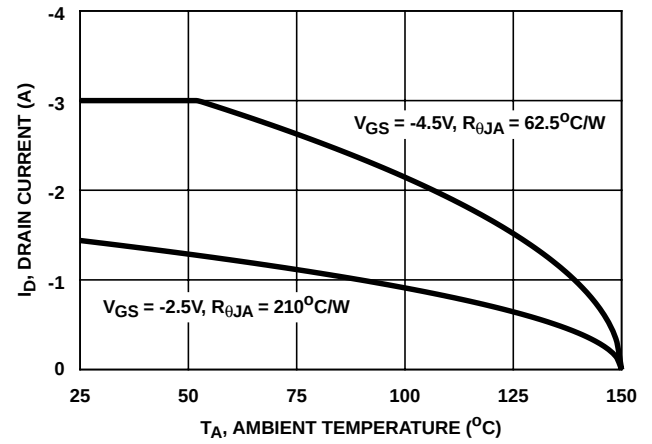


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

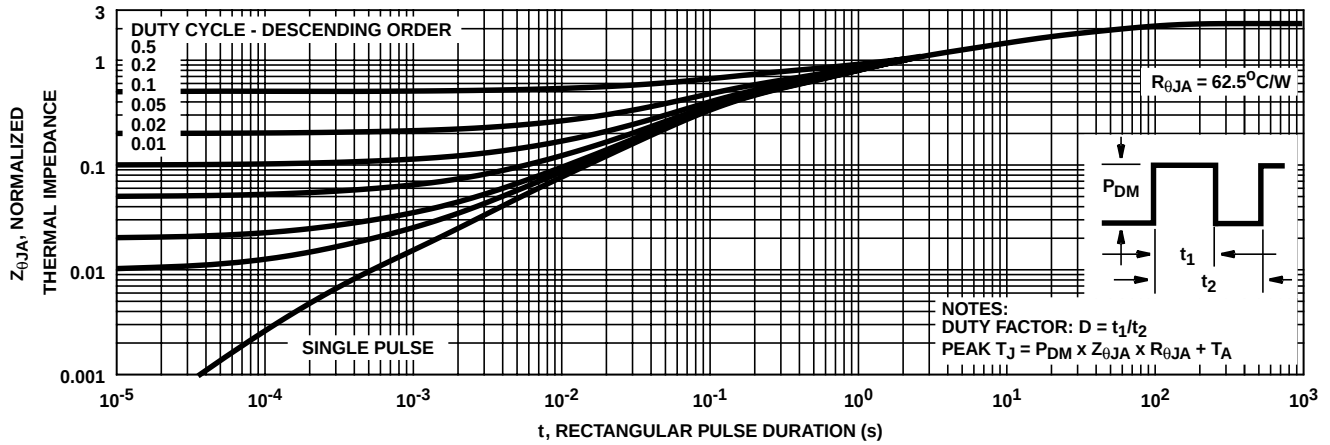


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

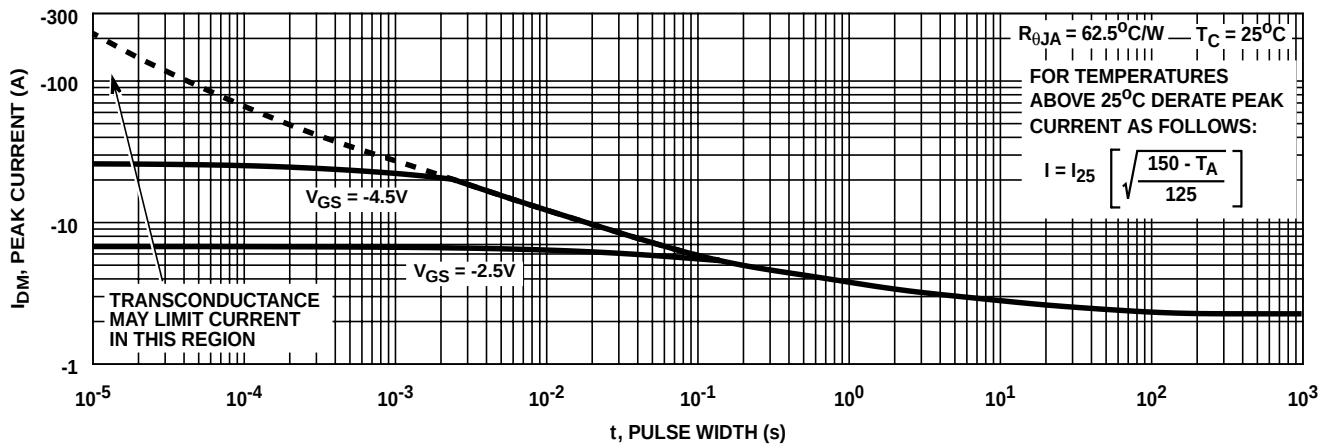


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

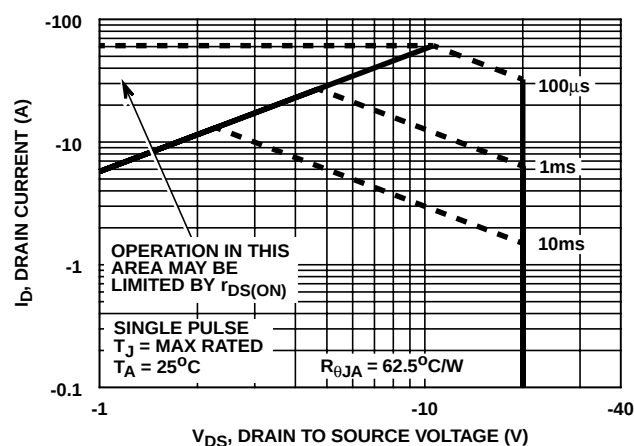


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

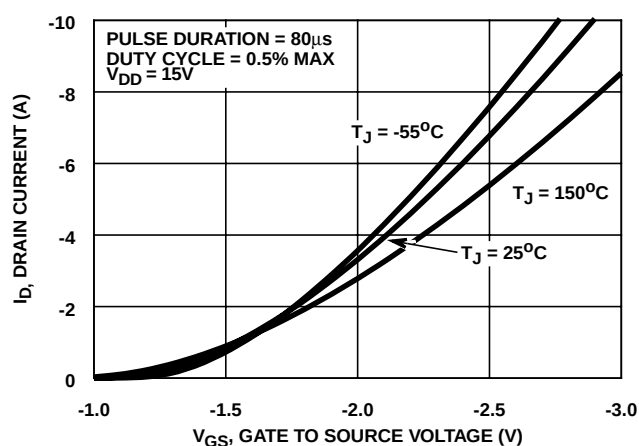


FIGURE 6. TRANSFER CHARACTERISTICS

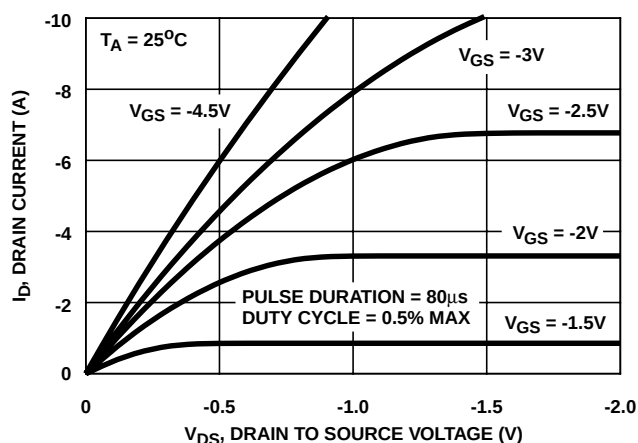


FIGURE 7. SATURATION CHARACTERISTICS

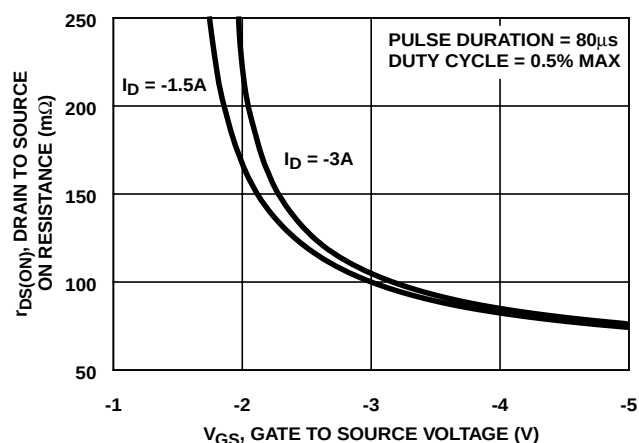


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

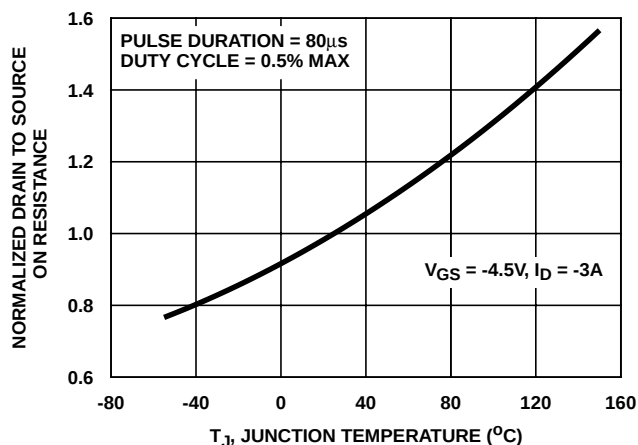


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

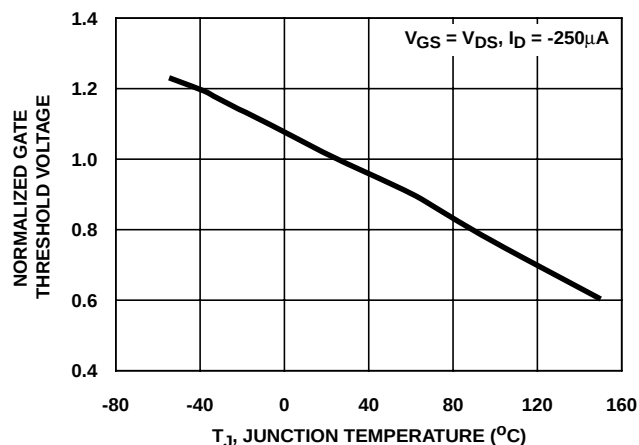


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

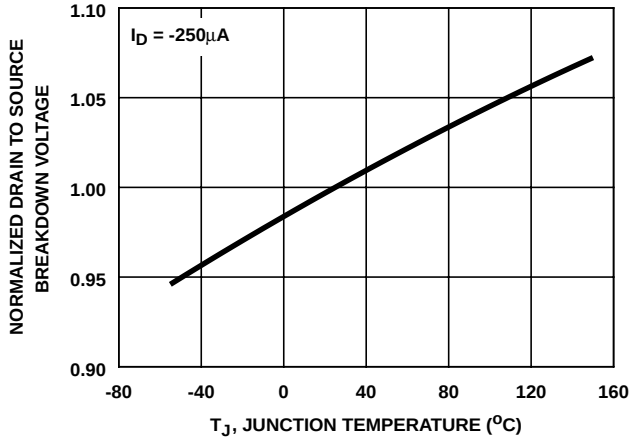


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

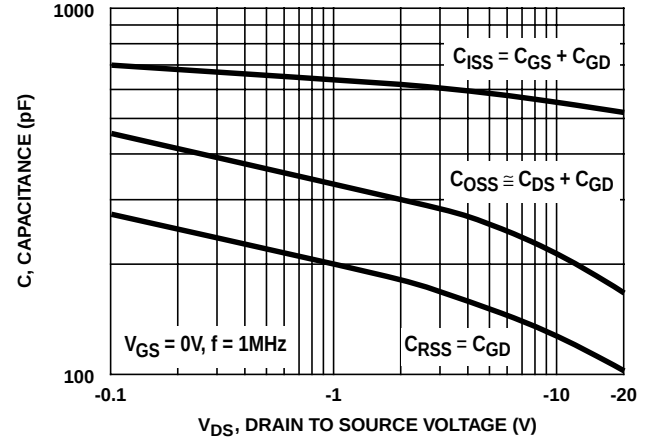
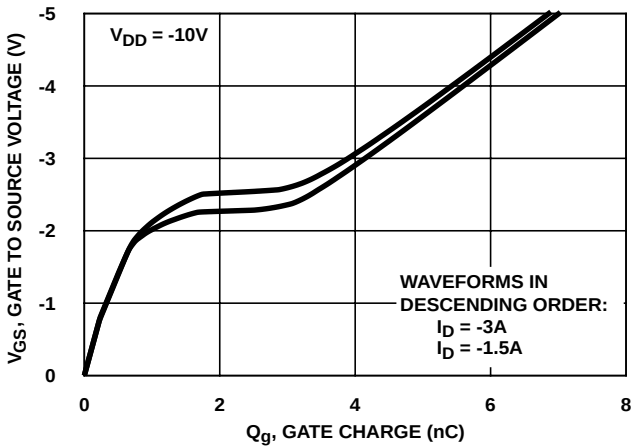


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

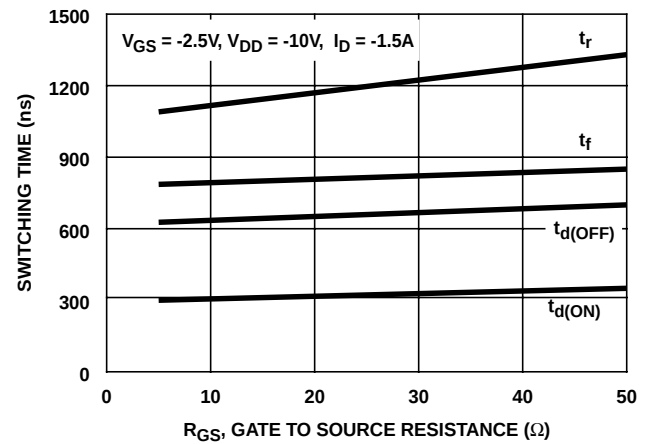


FIGURE 14. SWITCHING TIME vs GATE RESISTANCE

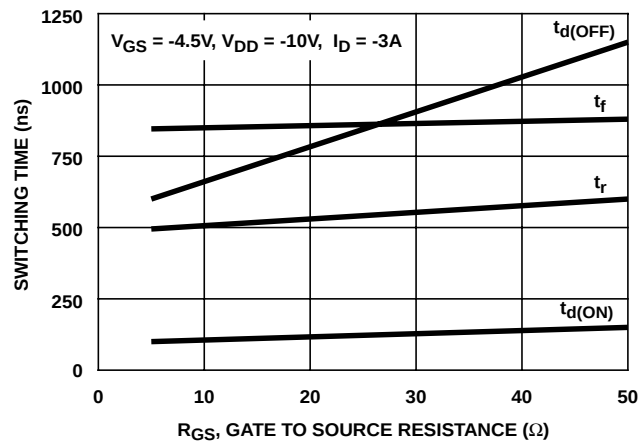


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

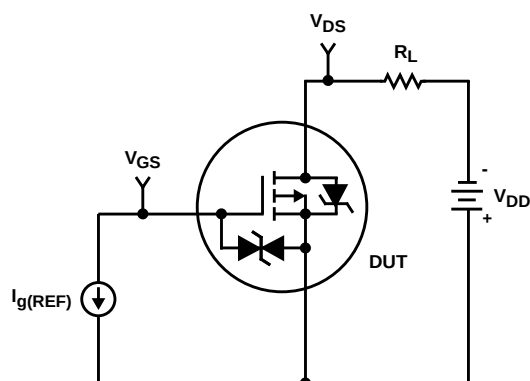


FIGURE 16. GATE CHARGE TEST CIRCUIT

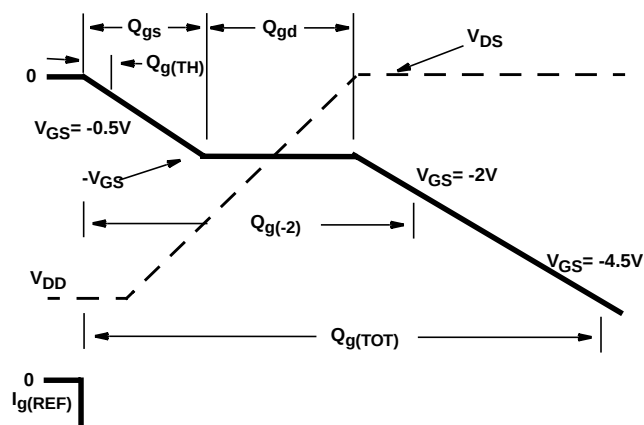


FIGURE 17. GATE CHARGE WAVEFORMS

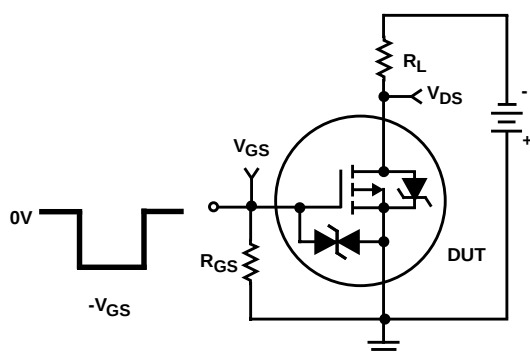


FIGURE 18. SWITCHING TIME TEST CIRCUIT

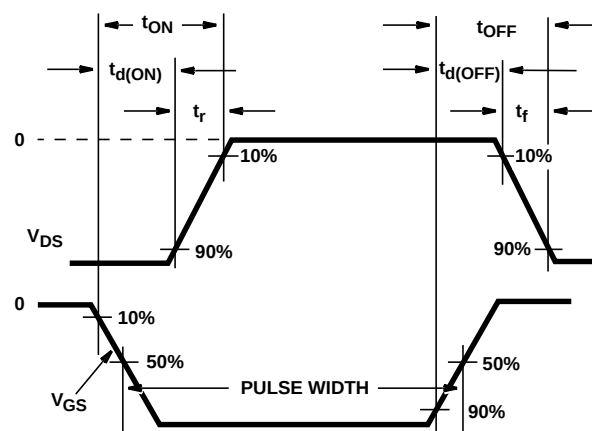


FIGURE 19. SWITCHING TIME WAVEFORM

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}\text{C}$), and thermal resistance $R_{\theta JA}$ ($^{\circ}\text{C}/\text{W}$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TSOP-6 package, the environment in which it is applied will have a significant influence on the part's current and maximum

power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Intersil provides thermal information to assist the designer's preliminary application evaluation. Figure 20 defines the

$R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Intersil device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM} .

Thermal resistances corresponding to other copper areas can be obtained from Figure 20 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a coefficient added to a constant. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 120.6 - 18.9 \times \ln(\text{Area}) \quad (\text{EQ. 2})$$

The transient thermal impedance ($Z_{\theta JA}$) is also affected by varied top copper board area. Figure 21 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the

graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, C THERM1 through C THERM5 and R THERM1 through R THERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

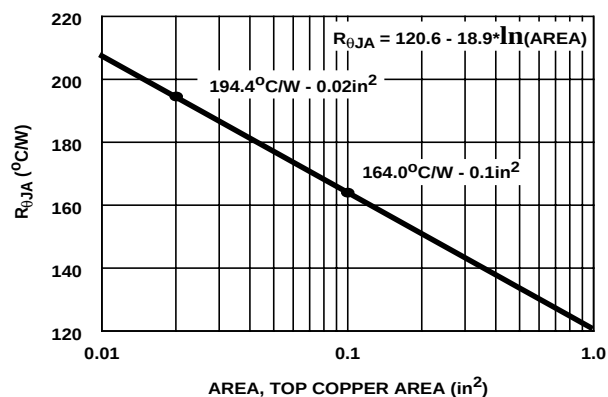


FIGURE 20. THERMAL RESISTANCE vs MOUNTING PAD

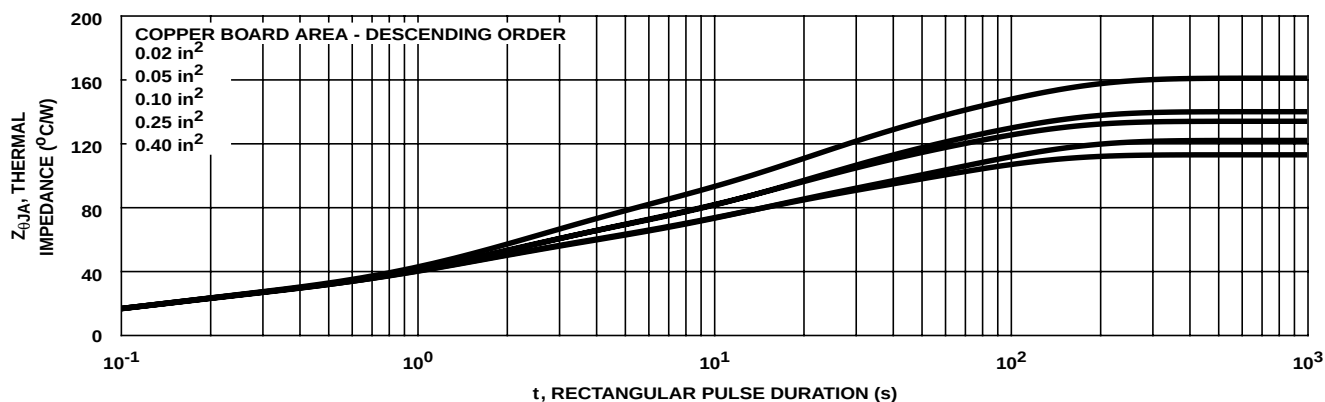


FIGURE 21. THERMAL IMPEDANCE vs MOUNTING PAD AREA

SABER Electrical Model

REV January 2000

template itf87052svt n2,n1,n3

electrical n2,n1,n3

```

{
var i iscl
dp..model dbodymod = (isl = 2.4e-11, ikf = 0.06, cjo = 2e-10, tt = 5.1e-9, m = 0.27, rs = 1.7e-2, trs1 = 1.7e-3, trs2 = 2e-6)
dp..model dbreakmod = (rs = 4e-1, trs1 = 1e-3, trs2 = 2e-6)
dp..model desd1mod = (bv = 10.8, tbv1 = -1.9e-3, nl = 11, rs = 450)
dp..model desd2mod = (bv = 10.8, tbv1 = -1.9e-3, nl = 11, rs = 450)
dp..model dplcapmod = (cjo = 2.2e-10, isl = 10e-30, nl = 10, m = 0.31, vj = 0.45)
m..model mmedmod = (type=_p, vto = -0.95, kp = 1.7, is = 1e-30, tox = 1, rs = 0.1)
m..model mstrongmod = (type=_p, vto = -1.10, kp = 9.7, is = 1e-30, tox = 1)
m..model mweakmod = (type=_p, vto = -0.75, kp = 0.06, is = 1e-30, tox = 1, rs = 0.1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = 2.5, voff = 1.5)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = 1.5, voff = 2.5)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = 0.75, voff = -0.5)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = -0.5, voff = 0.75)

```

```

c.ca n12 n8 = 9.3e-10
c.cb n15 n14 = 9.7e-10
c.cin n6 n8 = 4.5e-10

```

```

dp.dbody n5 n7 = model=dbodymod
dp.dbreak n7 n11 = model=dbreakmod
dp.desd1 n91 n9 = model=desd1mod
dp.desd2 n91 n7 = model=desd2mod
dp.dplcap n10 n6 = model=dplcapmod

```

i.it n8 n17 = 1

```

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 3.6e-9
l.lsource n3 n7 = 4.3e-9

```

```

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

```

```

res.rbreak n17 n18 = 1, tc1 = 7.2e-4, tc2 = -5e-7
res.rdrain n50 n16 = 1e-3, tc1 = 1.7e-1, tc2 = 1e-5
res.rgate n9 n20 = 650
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 36
res.rlsource n3 n7 = 43
res.rslc1 n5 n51 = 1e-6, tc1 = 1e-3, tc2 = 1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 4.8e-2, tc1 = -1e-4, tc2 = 9e-6
res.rvtemp n18 n19 = 1, tc1 = 0, tc2 = 2e-6
res.rvthres n22 n8 = 1, tc1 = 1.5e-3, tc2 = 3e-6

```

spe.ebreak n5 n11 n17 n18 = -27.08

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n5 n10 n8 n6 = 1

spe.evtemp n6 n20 n18 n22 = 1

spe.evthres n6 n21 n19 n8 = 1

```

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

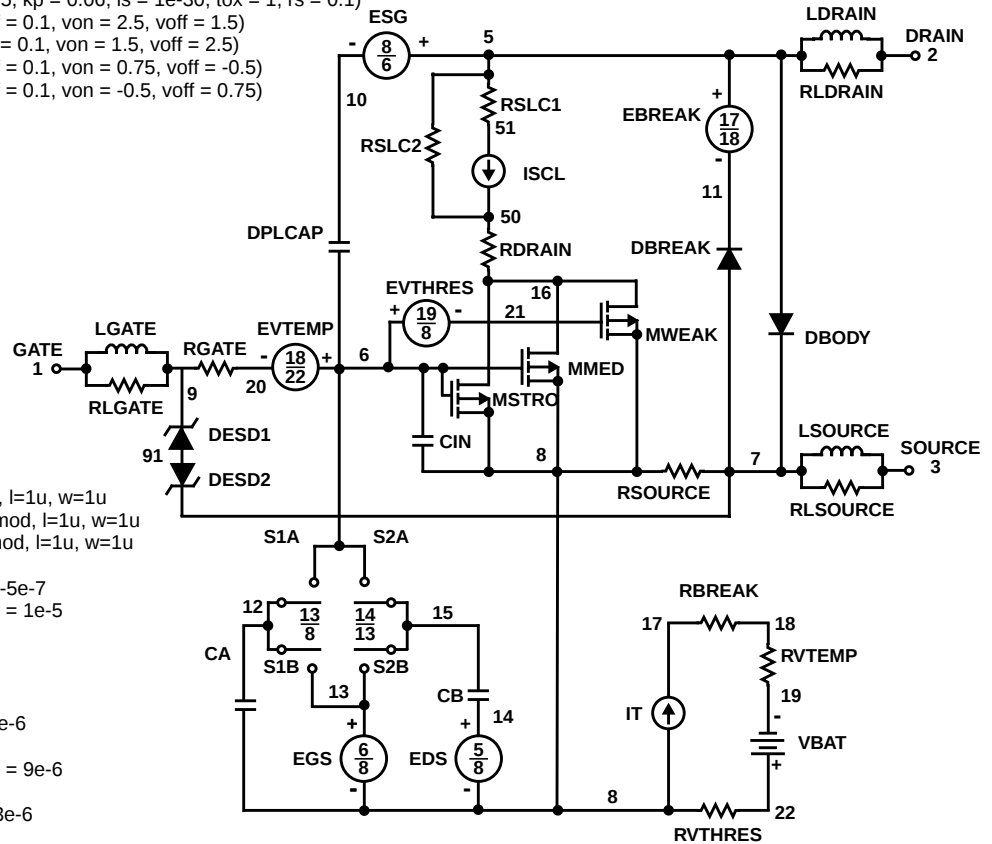
```

v.vbat n22 n19 = dc=1

```

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = (((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/32)** 2.1))
}
}

```



SPICE Thermal Model

REV January 2000

ITF87052SVT

Copper Area = 0.02 in²

CTHERM1 th 8 1.1e-3

CTHERM2 8 7 5.0e-3

CTHERM3 7 6 7.0e-3

CTHERM4 6 5 9.0e-3

CTHERM5 5 4 1.1e-2

CTHERM6 4 3 4.0e-2

CTHERM7 3 2 3.0e-1

CTHERM8 2 tl 1.5

R THERM1 th 8 2.5e-1

R THERM2 8 7 6.0e-1

R THERM3 7 6 1.25

R THERM4 6 5 8

R THERM5 5 4 10

R THERM6 4 3 43

R THERM7 3 2 48

R THERM8 2 tl 50

SABER Thermal Model

Copper Area = 0.02 in²

template thermal_model th tl

thermal_c th, tl

```
{
  ctherm.ctherm1 th 8 = 1.1e-3
  ctherm.ctherm2 8 7 = 5.0e-3
  ctherm.ctherm3 7 6 = 7.0e-3
  ctherm.ctherm4 6 5 = 9.0e-3
  ctherm.ctherm5 5 4 = 1.1e-2
  ctherm.ctherm6 4 3 = 4.0e-2
  ctherm.ctherm7 3 2 = 3.0e-1
  ctherm.ctherm8 2 tl = 1.5

```

```
rtherm.rtherm1 th 8 = 2.5e-1
rtherm.rtherm2 8 7 = 6.0e-1
rtherm.rtherm3 7 6 = 1.25
rtherm.rtherm4 6 5 = 8
rtherm.rtherm5 5 4 = 10
rtherm.rtherm6 4 3 = 43
rtherm.rtherm7 3 2 = 48
rtherm.rtherm8 2 tl = 50
}
```

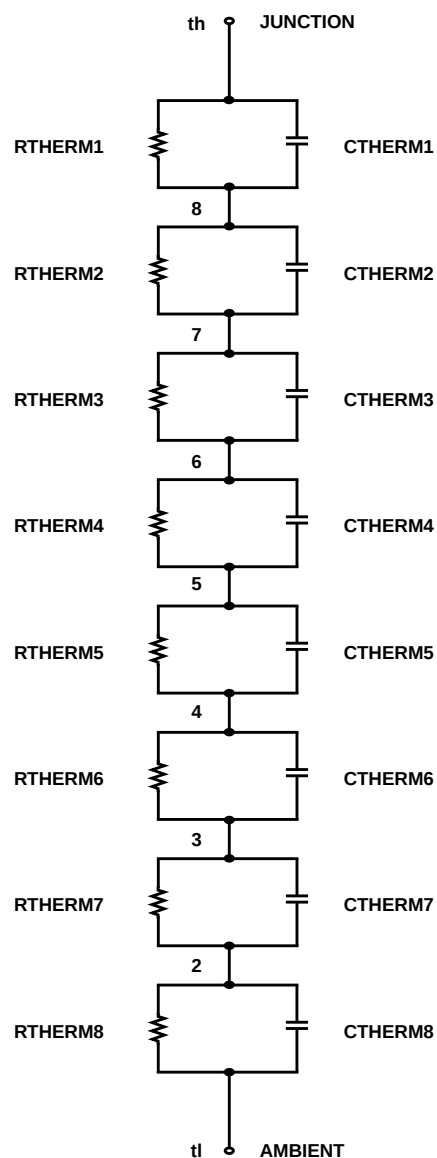
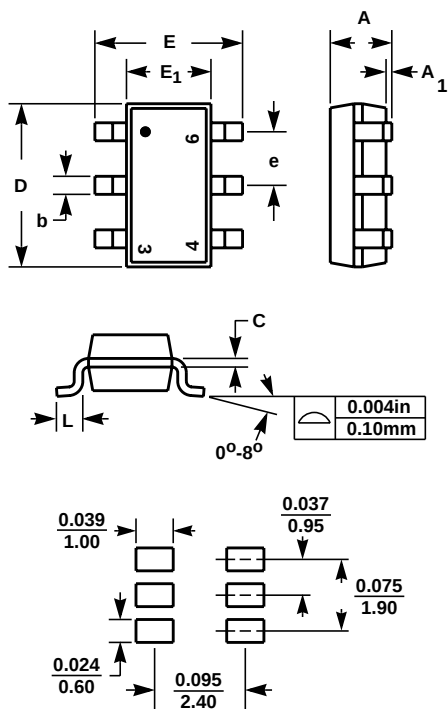


TABLE 1. Thermal Models

COMPONENT	0.02 in ²	0.05 in ²	0.10 in ²	0.25 in ²	0.40 in ²
CTHERM6	4.0e-2	4.0e-2	4.2e-2	4.0e-2	4.0e-2
CTHERM7	3.0e-1	3.5e-1	3.3e-1	3.0e-1	2.8e-1
CTHERM8	1.5	1.5	1.5	1.5	1.5
R THERM6	43	35	35	27	27
R THERM7	48	40	37	30	29
R THERM8	50	45	42	45	37

MO-193AA (TSOP-6)

6 LEAD JEDEC MO-193AA TSOP PLASTIC PACKAGE
(SIMILAR TO SSOT™-6)



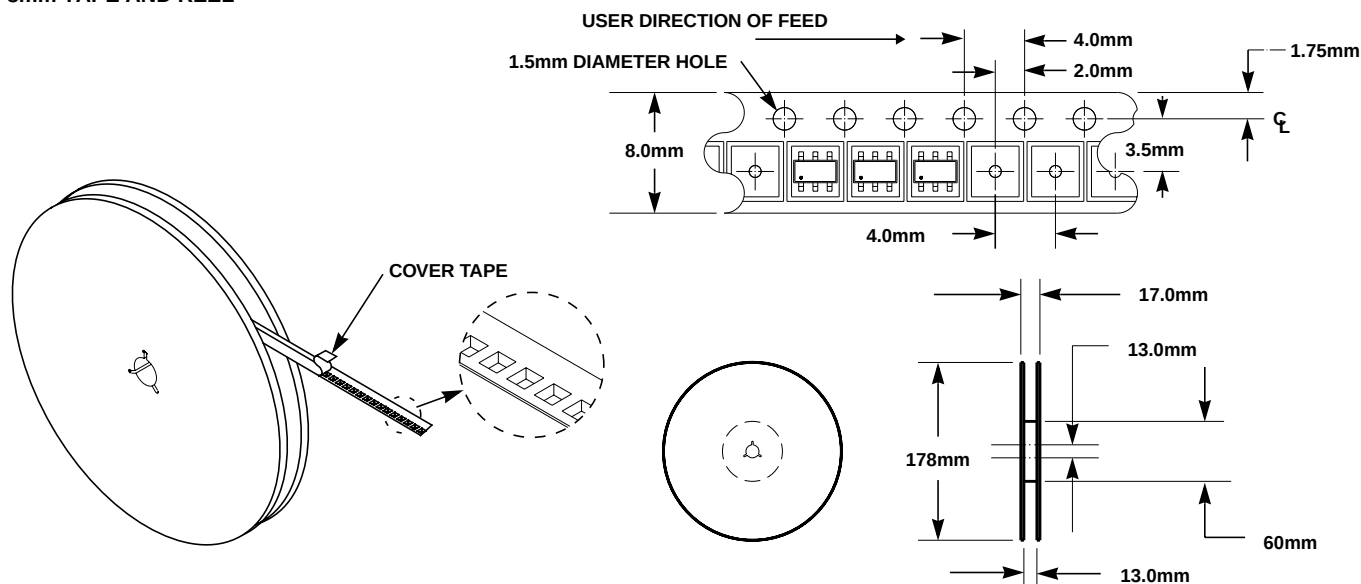
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.035	0.043	0.90	1.10	
A ₁	0.004		0.10		
b	0.012	0.020	0.30	0.50	
c	0.003	0.008	0.08	0.20	
D	0.107	0.122	2.70	3.10	2
E	0.103	0.118	2.60	3.00	
E ₁	0.056	0.070	1.40	1.80	3
e	0.037 BSC		0.95 BSC		
L	0.014	0.021	0.35	0.55	4

NOTES:

1. All dimensions are within the allowable dimensions of Rev. B of JEDEC MO-193AA outline dated 10-99.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.006 inches (0.15mm) per side.
4. "L" is the length of terminal for soldering.
5. Controlling dimension: Millimeter.
6. Revision 1 dated 2-00.

MO-193AA (TSOP-6)

8mm TAPE AND REEL

**GENERAL INFORMATION**

1. 3000 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

SSOT™-6 is a trademark of Fairchild Semiconductor.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site **www.intersil.com**

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029