

22A, 100V, 0.080 Ohm, N-Channel Power MOSFETs

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA9845.

Ordering Information

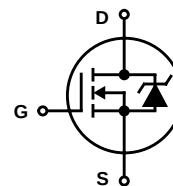
PART NUMBER	PACKAGE	BRAND
RFP22N10	TO-220AB	RFP22N10
RF1S22N10SM	TO-263AB	F1S22N10

NOTE: When ordering use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, e.g. RF1S22N10SM9A.

Features

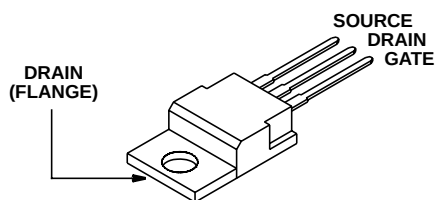
- 22A, 100V
- $r_{DS(ON)} = 0.080\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

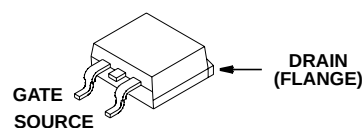


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



RFP22N10, RF1S22N10SM

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	RFP22N10, RF1S22N10SMS	UNITS	
Drain to Source Voltage (Note 1)	V_{DSS}	100	V
Drain to Gate Voltage ($R_{GS} = 1M\Omega$) (Note 1)	V_{DGR}	100	V
Gate to Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	22	A
Pulsed Drain Current	I_{DM}	50	A
Maximum Power Dissipation	P_D	100	W
Linear Derating Factor		0.67	W/ $^{\circ}C$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^{\circ}C$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300	$^{\circ}C$
Package Body for 10s, See Techbrief 334	T_{pkq}	260	$^{\circ}C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0 (Figure 7)		100	-	-	V
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 9)		2	-	4	V
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V		-	-	1	μA
		V _{DS} = 80V, V _{GS} = 0V, T _C = 150 ⁰ C		-	-	50	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0		-	-	±100	nA
Drain to Source On Resistance (Note 2)	r _{DS(ON)}	I _D = 22A, V _{GS} = 10V (Figure 8)		-	-	0.080	Ω
Turn-On Time	t _(ON)	V _{DD} = 50V R _L = 4.5Ω, V _{GS} = 10V, R _{GS} = 25Ω (Figure 11)		-	-	60	ns
Turn-On Delay Time	t _{d(ON)}			-	13	-	ns
Rise Time	t _r			-	24	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	65	-	ns
Fall Time	t _f			-	18	-	ns
Turn-Off Time	t _(OFF)			-	-	120	ns
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 80V, I _D ≈ 22A, R _L = 3.64Ω I _{g(REF)} = 1mA (Figure 11)	-	-	150	nC
Gate Charge at 10V	Q _{G(10)}	V _{GS} = 0V to 10V		-	-	75	nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 0V to 2V		-	-	3.5	nC
Thermal Resistance Junction to Case	R _{θJC}			-	-	1.5	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-220 and TO-263		-	-	62	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 22\text{A}$	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 22\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	200	ns

NOTE:

2. Pulse Test: Pulse Duration = 300 μs maximum, duty cycle = 2%.

Typical Performance Curves Unless otherwise Specified

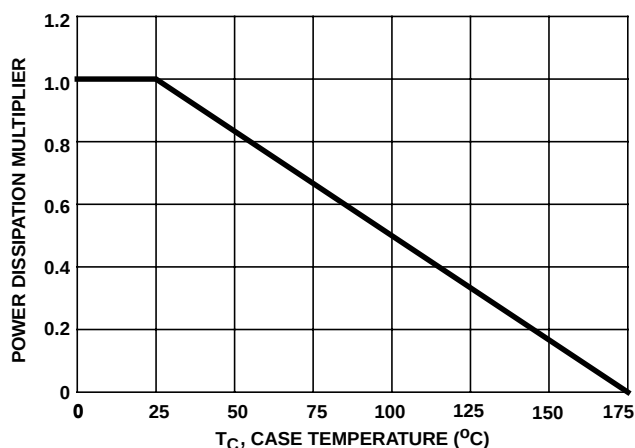


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

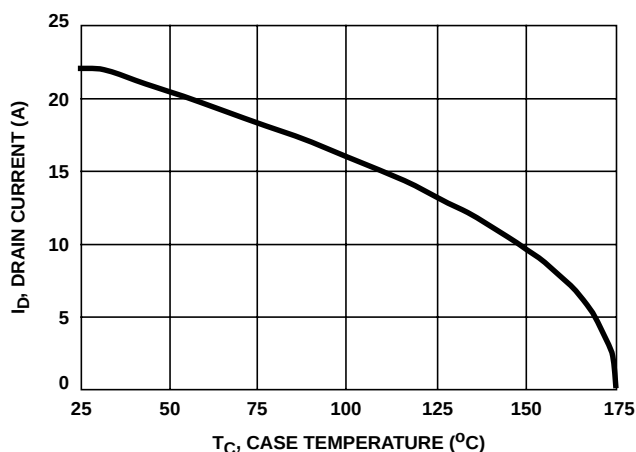


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

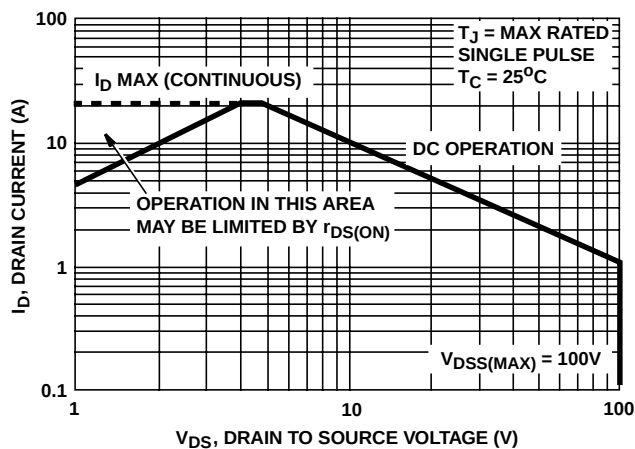


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

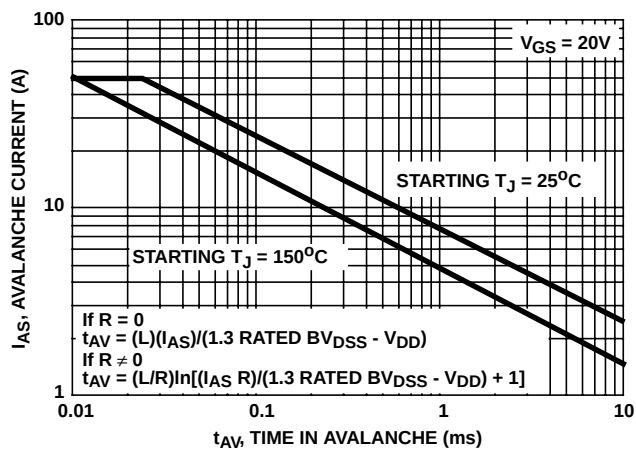


FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

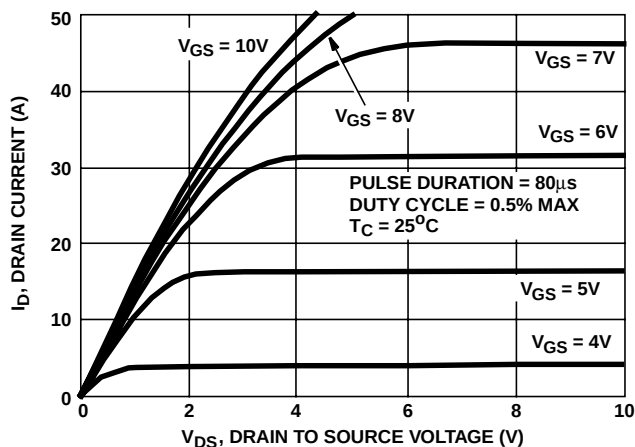


FIGURE 5. SATURATION CHARACTERISTICS

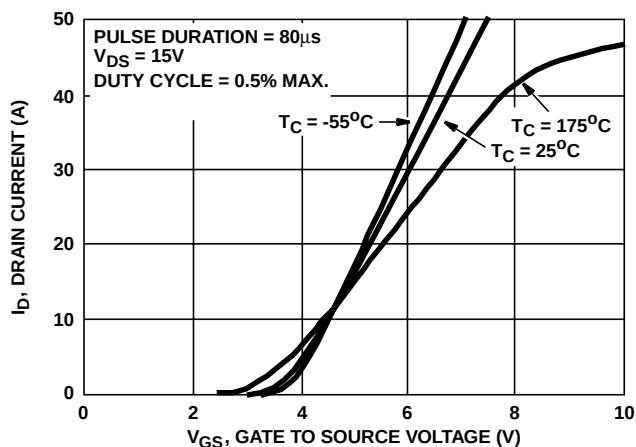


FIGURE 6. TRANSER CHARACTERISTICS

Typical Performance Curves Unless otherwise Specified (Continued)

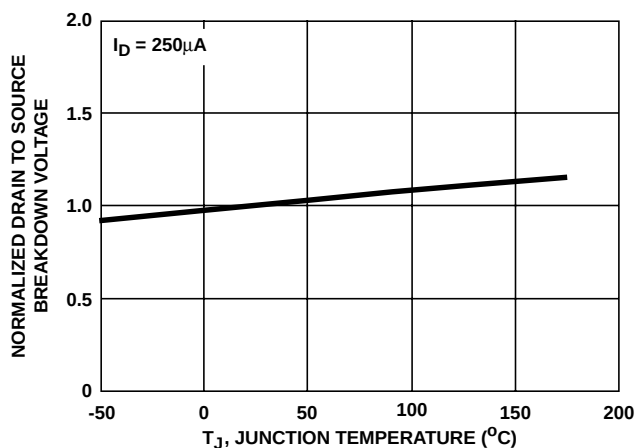


FIGURE 7. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

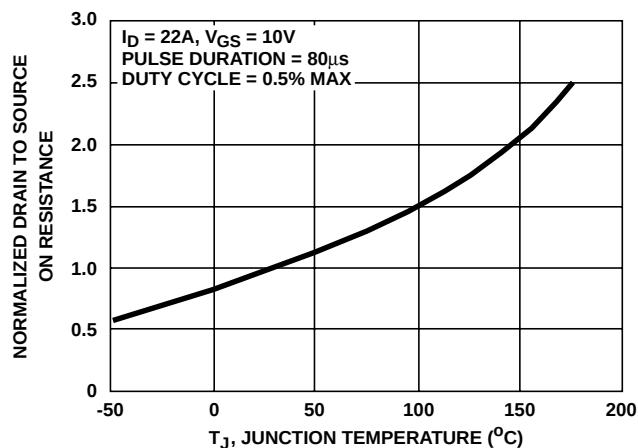


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

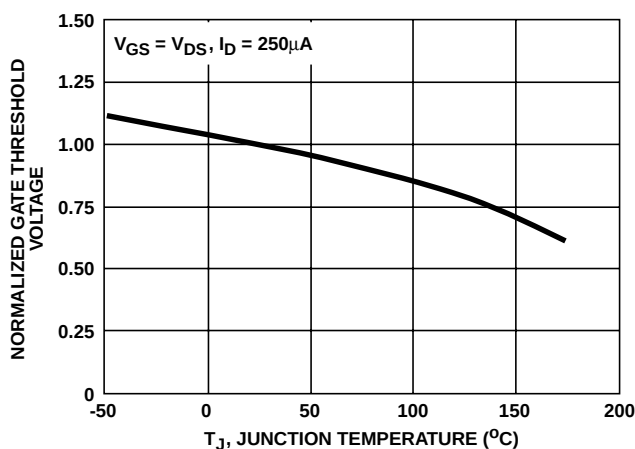


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

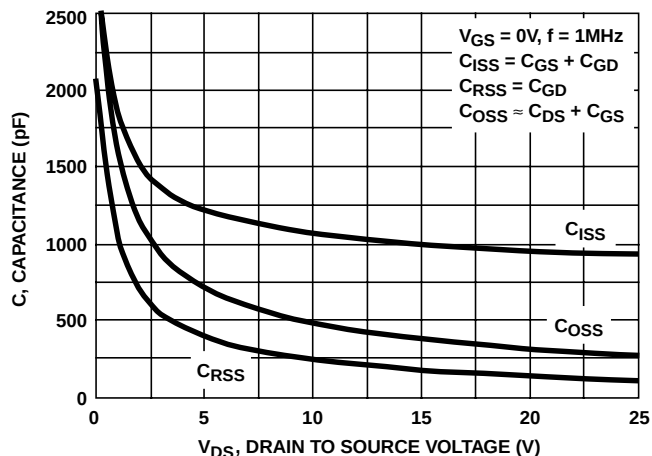
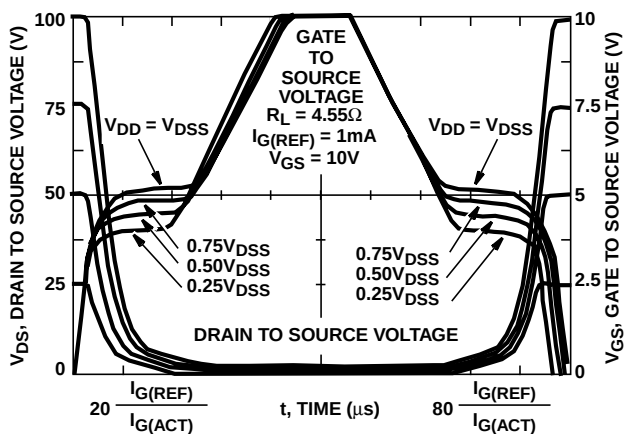


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

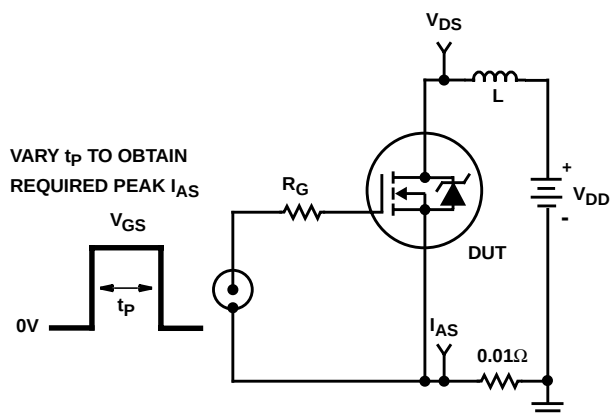


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

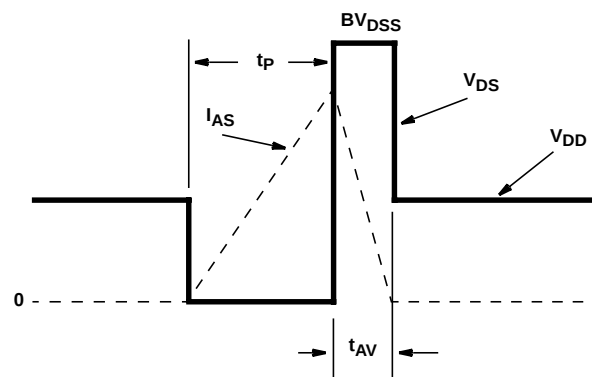


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

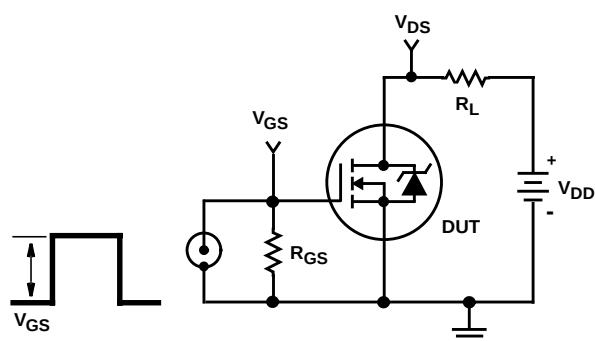


FIGURE 14. SWITCHING TIME TEST CIRCUIT

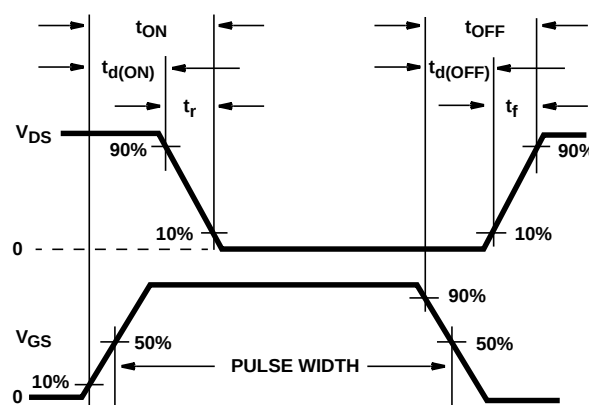


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

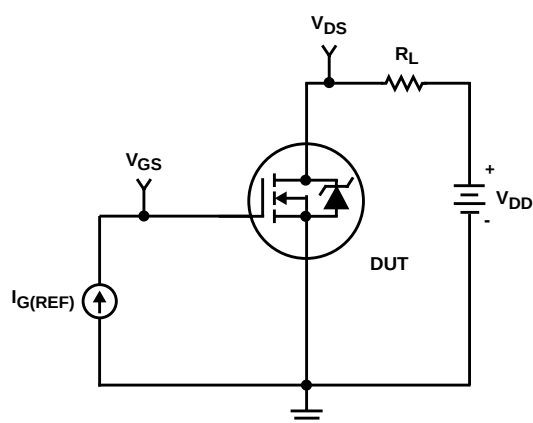


FIGURE 16. GATE CHARGE TEST CIRCUIT

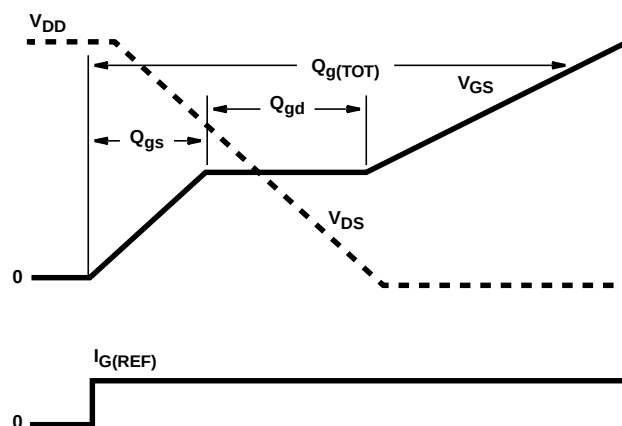


FIGURE 17. GATE CHARGE WAVEFORMS

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