-2A, -80V and -100V, 3.500 Ohm, P-Channel Power MOSFETs

These are P-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters. motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA_____.

Ordering Information

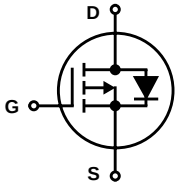
PART NUMBER	PACKAGE	BRAND
RFP2P08	TO-220AB	RFP2P08
RFP2P10	TO-220AB	RFP2P10

NOTE: When ordering, use entire part number.

Features

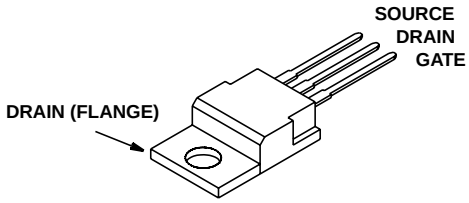
- -2A, -80V and -100V
- $r_{DS(ON)} = 3.500\Omega$
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards

Symbol



Packaging

TO-220AB



	RFP2P08	RFP2P10	UNITS
Drain to Source Voltage (Note 1) . . . . . V_{DSS}	-80	-100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1) . . . . . V_{DGR}	-80	-100	V
Continuous Drain Current . . . . . I_D	2	2	A
Pulsed Drain Current (Note 3) . . . . . I_{DM}	5	5	A
Gate to Source Voltage . . . . . V_{GS}	±20	±20	V
Maximum Power Dissipation . . . . . P_D	25	25	W
Linear Derating Factor	0.2	0.2	W/^{o}Caaa
Operating and Storage Temperature . . . . . T_J, T_{STG}	-55 to 150	-55 to 150	^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s . . . . . T_L	300	300	^{o}C
Package Body for 10s, See Techbrief 334 . . . . . T_{pkg}	260	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. T_J = 25^{o}C to 125^{o}C.

Electrical Specifications T_C = 25^{o}C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	ID = -250µA, VGS = 0				
RFP2P08			-80	-	-	V
RFP2P10			-100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = -250µA	-2	-	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	-1	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, T_C = 125^{o}C	-	-	-25	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = -2A, V_{GS} = -10V (Figures 6, 7)	-	-	3.500	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = -2A, V_{GS} = -10V	-	-	-7.0	V
Turn-On Delay Time	$t_{d(ON)}$	I_D = ≈ 1A, V_{DD} = -50V, R_G = 50Ω, V_{GS} = -10V, R_L = 46.5Ω (Figures 10, 11, 12)	-	7	25	ns
Rise Time	t_r		-	15	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	14	45	ns
Fall Time	t_f		-	11	25	ns
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f =1MHz (Figure 9)	-	-	150	pF
Output Capacitance	C_{OSS}		-	-	80	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	30	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	5	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = -1A	-	-	-1.4	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = -2A, dI_{SD}/dt = 50A/µs	-	135	-	ns

NOTES:

2. Pulse Test: Pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves Unless otherwise Specified

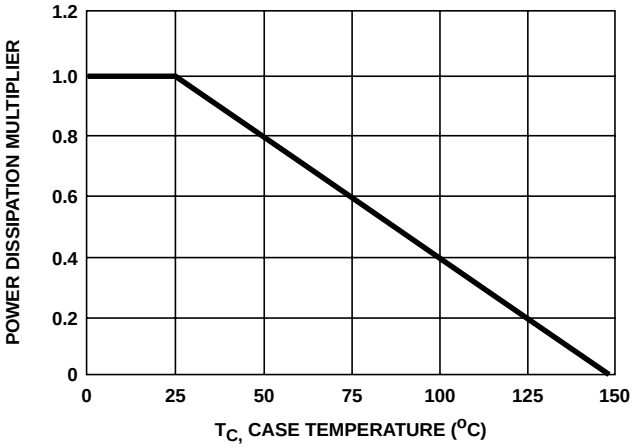


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

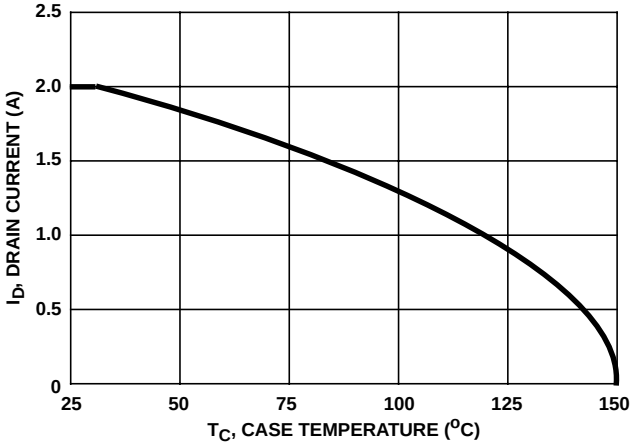


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

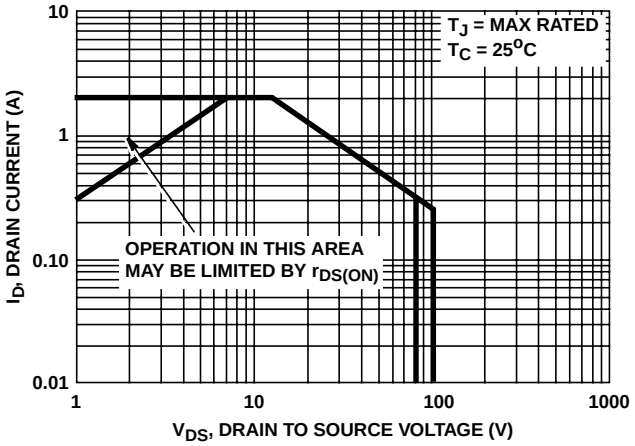


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

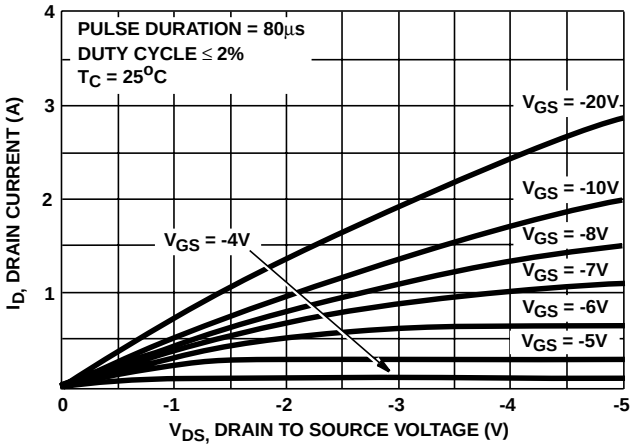


FIGURE 4. SATURATION CHARACTERISTICS

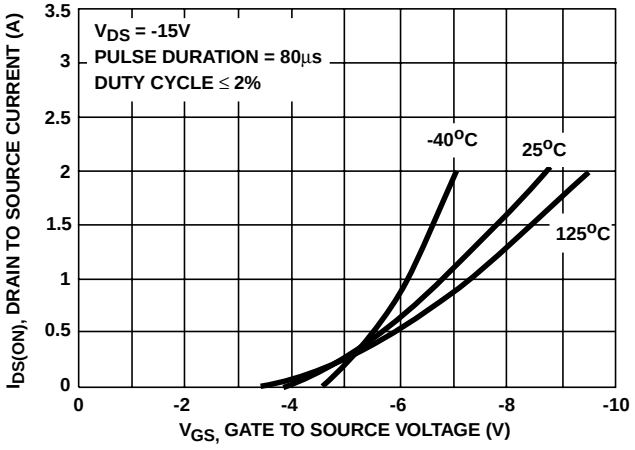


FIGURE 5. TRANSER CHARACTERISTICS

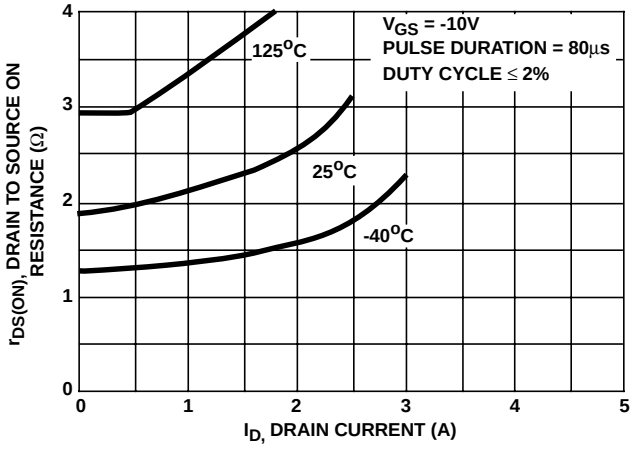


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless otherwise Specified **(Continued)**

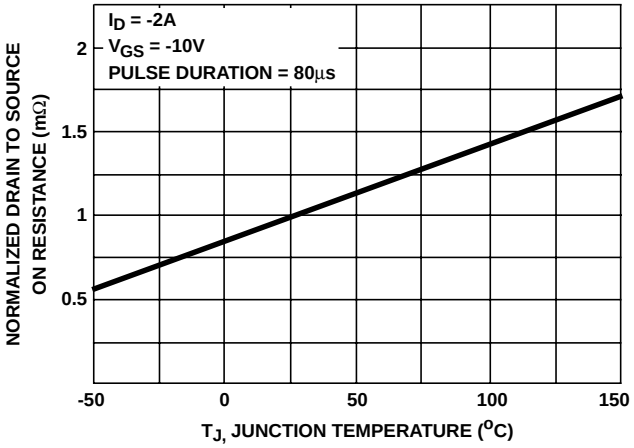


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

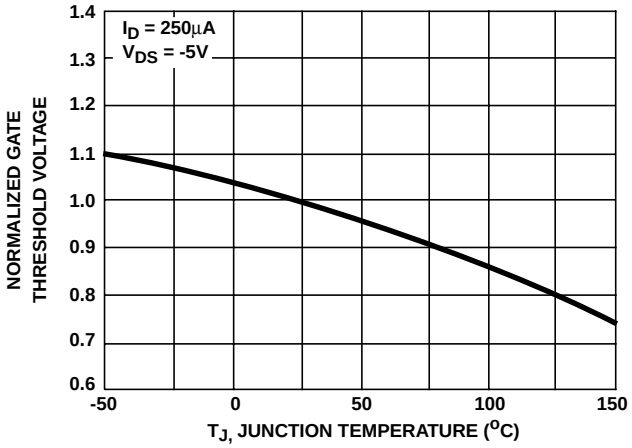


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

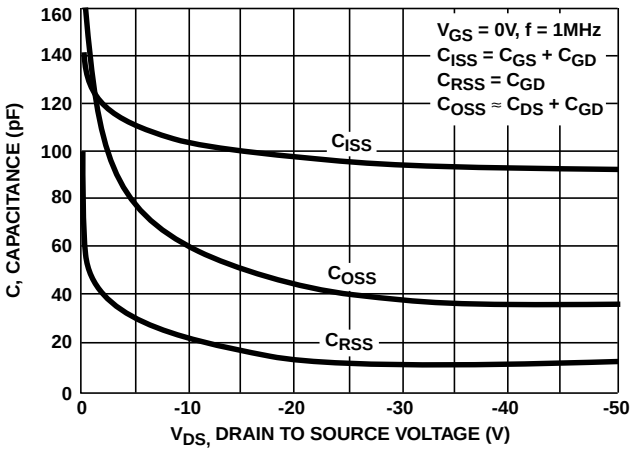
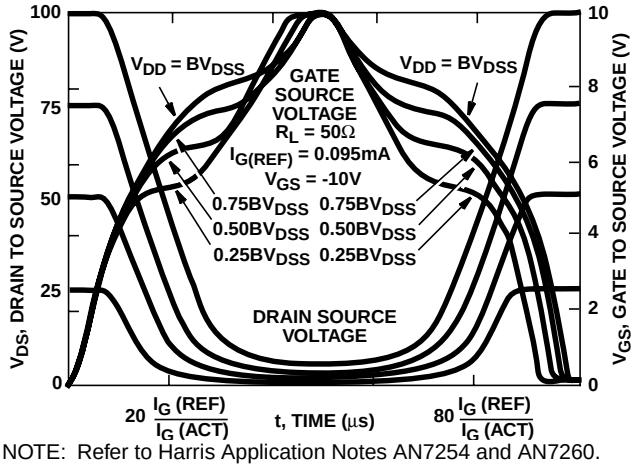


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuit and Waveforms

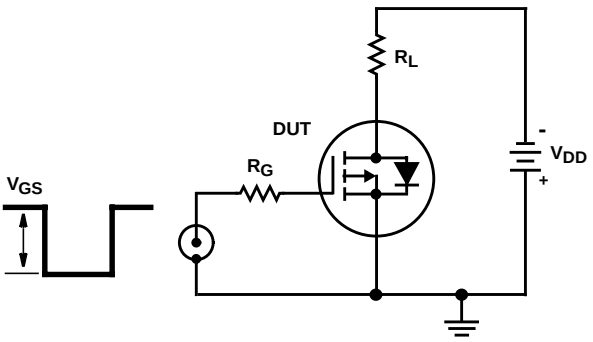


FIGURE 11. SWITCHING TIME TEST CIRCUIT

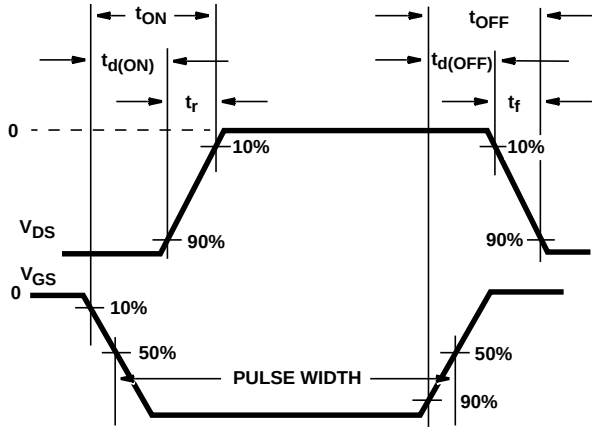


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

Test Circuit and Waveforms

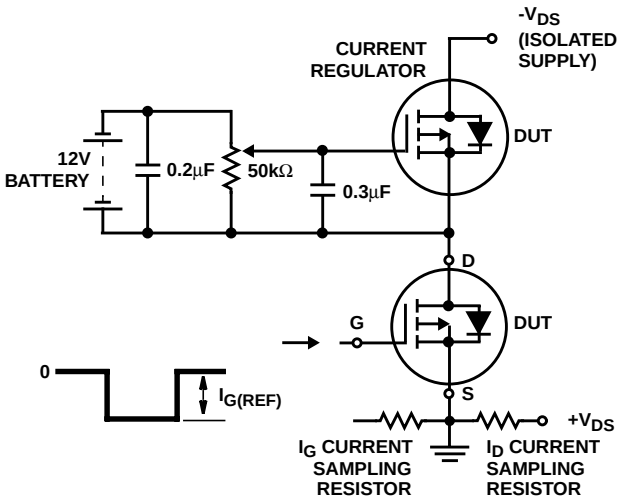


FIGURE 13. GATE CHARGE TEST CIRCUIT

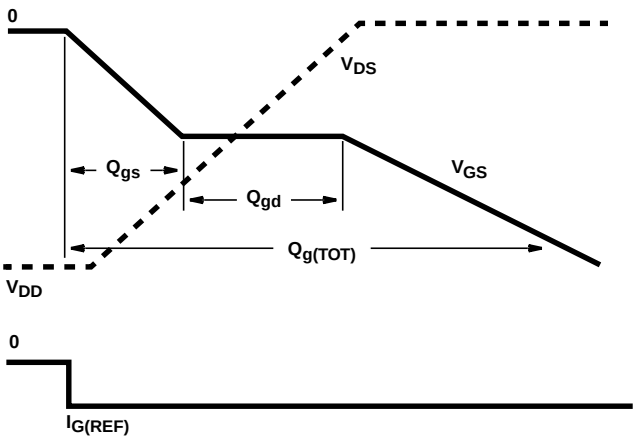


FIGURE 14. GATE CHARGE WAVEFORMS