74HC1G66; 74HCT1G66

Single-pole single-throw analog switch

Rev. 04 — 19 December 2008 Product data sheet

1. General description

74HC1G66 and 74HCT1G66 are high-speed Si-gate CMOS devices. They are single-pole single-throw analog switches. The switch has two input/output pins (Y and Z) and an active HIGH enable input pin (E). When pin E is LOW, the analog switch is turned off.

The non-standard output currents are equal to those of the 74HC4066 and 74HCT4066.

2. Features

- Wide supply voltage range from 2.0 V to 10.0 V for the 74HC1G66
- Very low ON resistance:
  - 45 Ω (typ.) at V_{CC} = 4.5 V
  - 30 Ω (typ.) at V_{CC} = 6.0 V
  - 25 Ω (typ.) at V_{CC} = 9.0 V
- High noise immunity
- Low power dissipation
- Multiple package options
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC1G66GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74HCT1G66GW				
74HC1G66GV	–40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74HCT1G66GV				

NXP founded by Philips

4. Marking

Table 2. Marking codes

Type number	Marking
74HC1G66GW	HL
74HCT1G66GW	TL
74HC1G66GV	H66
74HCT1G66GV	T66

5. Functional diagram

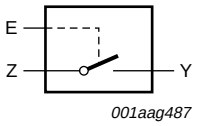


Fig 1. Logic symbol

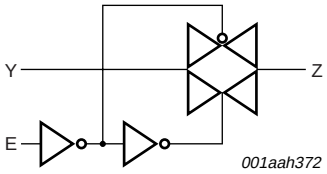


Fig 2. Logic diagram

6. Pinning information

6.1 Pinning

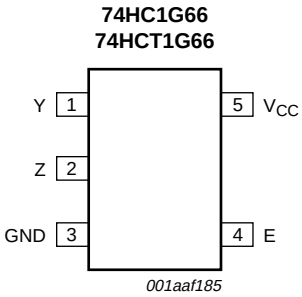


Fig 3. Pin configuration SOT353-1 and SOT753

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
Y	1	independent input or output
Z	2	independent input or output
GND	3	ground (0 V)
E	4	enable input (active HIGH)
V_{CC}	5	supply voltage

© NXP B.V. 2008. All rights reserved.

7. Functional description

Table 4. Function table[1]

Input E	Switch
L	OFF
H	ON

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+11.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	74HC1G66			74HCT1G66			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	10.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_{SW}	switch voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
		V_{CC} = 10.0 V	-	-	35	-	-	-	ns/V

[1] To avoid drawing V_{CC} current out of pin Z, when switch current flows in pin Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin Z, no V_{CC} current will flow out of terminal Y. In this case there is no limit for the voltage drop across the switch, but the voltage at pins Y and Z may not exceed V_{CC} or GND.

© NXP B.V. 2008. All rights reserved.

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC1G66								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
		V_{CC} = 9.0 V	6.3	4.7	-	6.3	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
		V_{CC} = 9.0 V	-	4.3	2.7	-	2.7	V
I_I	input leakage current	E; V_I = V_{CC} or GND						
		V_{CC} = 6.0 V	-	0.1	1.0	-	1.0	µA
		V_{CC} = 10.0 V	-	0.2	2.0	-	2.0	µA
$I_{S(OFF)}$	OFF-state leakage current	Y or Z; V_{CC} = 10 V; see Figure 4	-	0.1	1.0	-	1.0	µA
$I_{S(ON)}$	ON-state leakage current	Y or Z; V_{CC} = 10 V; see Figure 5	-	0.1	1.0	-	1.0	µA
I_{CC}	supply current	E, Y or Z; V_I = V_{CC} or GND; V_{SW} = GND or V_{CC}						
		V_{CC} = 6.0 V	-	1.0	10	-	20	µA
		V_{CC} = 10.0 V	-	2.0	20	-	40	µA
C_I	input capacitance		-	1.5	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	8	-	-	-	pF

© NXP B.V. 2008. All rights reserved.

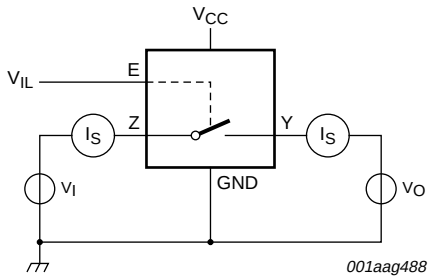
Table 7. Static characteristics *…continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HCT1G66								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	0.1	1.2	0.8	-	0.8	V
I_I	input leakage current	E; V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	0.1	1.0	-	1.0	µA
$I_{S(OFF)}$	OFF-state leakage current	Y or Z; V_{CC} = 5.5 V; see Figure 4	-	0.1	1.0	-	1.0	µA
$I_{S(ON)}$	ON-state leakage current	Y or Z; V_{CC} = 5.5 V; see Figure 5	-	0.1	1.0	-	1.0	µA
I_{CC}	supply current	E, Y or Z; V_I = V_{CC} or GND; V_{SW} = GND or V_{CC}; V_{CC} = 4.5 V to 5.5 V	-	1	10	-	20	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} – 2.1 V; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A	-	-	500	-	850	µA
C_I	input capacitance		-	1.5	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	8	-	-	-	pF

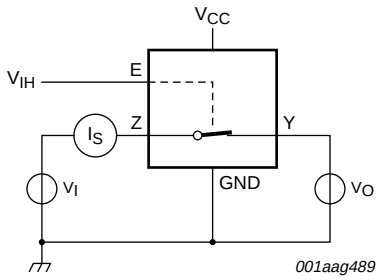
[1] Typical values are measured at T_{amb} = 25 °C.

10.1 Test circuits



V_I = V_{CC} or GND and V_O = GND or V_{CC}.

Fig 4. Test circuit for measuring OFF-state leakage current



V_I = V_{CC} or GND and V_O = open circuit.

Fig 5. Test circuit for measuring ON-state leakage current

© NXP B.V. 2008. All rights reserved.

10.2 ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graph see Figure 7.

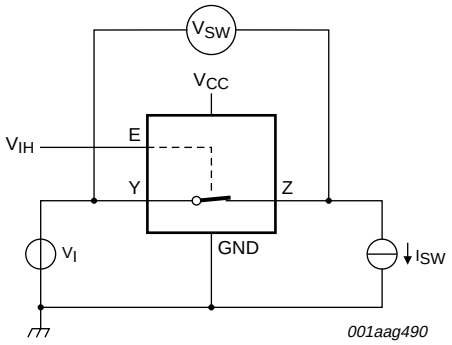
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[2]	Max	Min	Max	
74HC1G66[1]								
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}; see Figure 6						
		I_{SW} = 0.1 mA; V_{CC} = 2.0 V	-	-	-	-	-	Ω
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	42	118	-	142	Ω
		I_{SW} = 1 mA; V_{CC} = 6.0 V	-	31	105	-	126	Ω
		I_{SW} = 1 mA; V_{CC} = 9.0 V	-	23	88	-	105	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND; see Figure 6						
		I_{SW} = 0.1 mA; V_{CC} = 2.0 V	-	75	-	-	-	Ω
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	29	95	-	115	Ω
		I_{SW} = 1 mA; V_{CC} = 6.0 V	-	23	82	-	100	Ω
		I_{SW} = 1 mA; V_{CC} = 9.0 V	-	18	70	-	80	Ω
		V_I = V_{CC}; see Figure 6						
		I_{SW} = 0.1 mA; V_{CC} = 2.0 V	-	75	-	-	-	Ω
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	35	106	-	128	Ω
		I_{SW} = 1 mA; V_{CC} = 6.0 V	-	27	94	-	113	Ω
		I_{SW} = 1 mA; V_{CC} = 9.0 V	-	21	78	-	95	Ω
74HCT1G66								
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}; see Figure 6						
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	42	118	-	142	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND; see Figure 6						
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	29	95	-	115	Ω
		V_I = V_{CC}; see Figure 6						
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	35	106	-	128	Ω

[1] At supply voltages approaching 2 V, the ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using this supply voltage.

[2] Typical values are measured at T_{amb} = 25 °C.

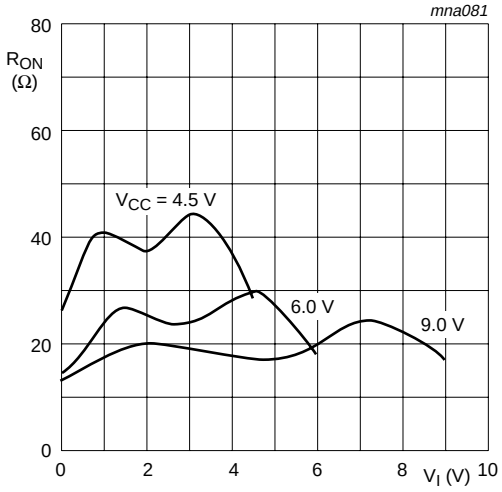
© NXP B.V. 2008. All rights reserved.

10.3 ON resistance test circuit and graphs



$R_{ON} = V_{SW} / I_{SW}$.

Fig 6. Test circuit for measuring ON resistance



T_{amb} = 25 °C.

Fig 7. Typical ON resistance as a function of input voltage

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; R_L = 1 kΩ, unless otherwise specified; For test circuit see Figure 10.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
74HC1G66									
t_{pd}	propagation delay	Y to Z or Z to Y; R_L = ∞ Ω; see Figure 8	[2]						
		V_{CC} = 2.0 V		-	8	75	-	90	ns
		V_{CC} = 4.5 V		-	3	15	-	18	ns
		V_{CC} = 6.0 V		-	2	13	-	15	ns
		V_{CC} = 9.0 V		-	1	10	-	12	ns
t_{en}	enable time	E to Y or Z; see Figure 9	[2]						
		V_{CC} = 2.0 V		-	50	125	-	150	ns
		V_{CC} = 4.5 V		-	16	25	-	30	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	11	-	-	-	ns
		V_{CC} = 6.0 V		-	13	21	-	26	ns
		V_{CC} = 9.0 V		-	9	16	-	20	ns

© NXP B.V. 2008. All rights reserved.

Table 9. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; R_L = 1 kΩ, unless otherwise specified; For test circuit see Figure 10.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{dis}	disable time	E to Y or Z; see Figure 9	[2]						
		V_{CC} = 2.0 V		-	27	190	-	225	ns
		V_{CC} = 4.5 V		-	16	38	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	11	-	-	-	ns
		V_{CC} = 6.0 V		-	14	33	-	38	ns
		V_{CC} = 9.0 V		-	12	16	-	20	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[3]	-	9	-	-	-	pF
74HCT1G66									
t_{pd}	propagation delay	Y to Z or Z to Y; R_L = ∞ Ω; see Figure 8	[2]						
		V_{CC} = 4.5 V		-	3	15	-	18	ns
t_{en}	enable time	E to Y or Z; see Figure 9	[2]						
		V_{CC} = 4.5 V		-	15	30	-	36	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	12	-	-	-	ns
t_{dis}	disable time	E to Y or Z; see Figure 9	[2]						
		V_{CC} = 4.5 V		-	13	44	-	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	12	-	-	-	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} − 1.5 V	[3]	-	9	-	-	-	pF

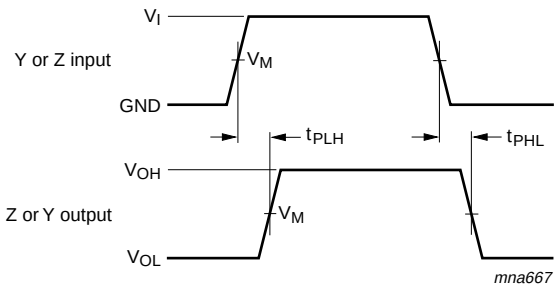
[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation P_D (µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
C_{SW} = maximum switch capacitance in pF (see Table 7);
V_{CC} = supply voltage in Volt;
$\Sigma ((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$ = sum of outputs.

© NXP B.V. 2008. All rights reserved.

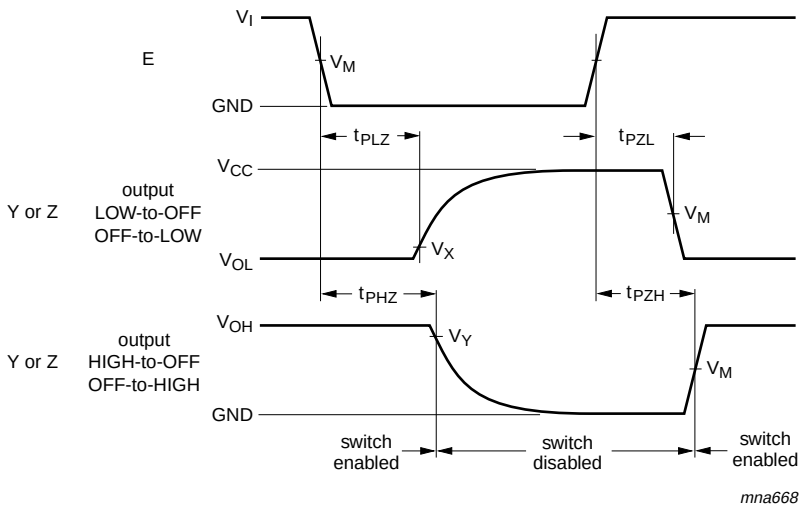
11.1 Waveforms and test circuit



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Input (Y or Z) to output (Z or Y) propagation delays



Measurement points are given in Table 10.

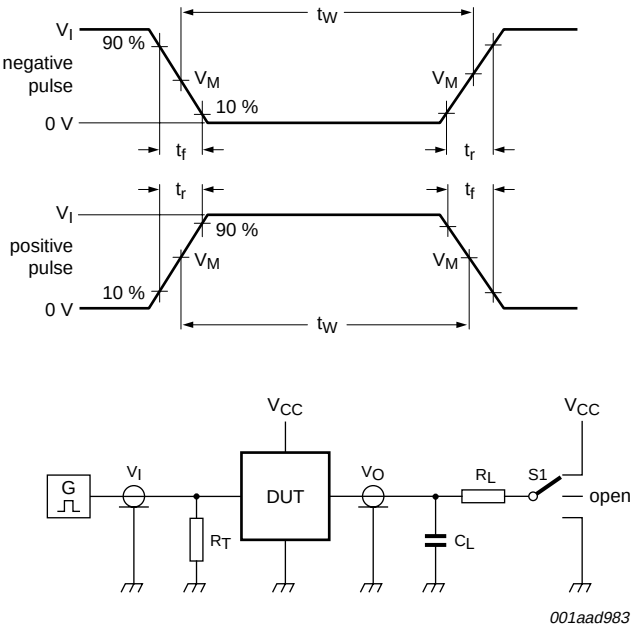
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Enable and disable times

Table 10. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC1G66	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 10%	V_{OH} – 10%
74HCT1G66	1.3 V	1.3 V	V_{OL} + 10%	V_{OH} – 10%

© NXP B.V. 2008. All rights reserved.



Test data is given in Table 11.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 10. Test circuit for measuring switching times

Table 11. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f[1]	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC1G66	GND to V_{CC}	6 ns	50 pF, 15 pF	1 kΩ, ∞ Ω	open	GND	V_{CC}
74HCT1G66	GND to 3 V	6 ns	50 pF, 15 pF	1 kΩ, ∞ Ω	open	GND	V_{CC}

[1] There is no constraint on t_r, t_f with a 50% duty factor when measuring f_{max}.

11.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics for 74HC1G66 and 74HCT1G66

GND = 0 V; $t_r = t_f$ = 6.0 ns; C_L = 50 pF; unless otherwise specified. All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; R_L = 10 kΩ; see Figure 11				%
		V_{CC} = 4.5 V; V_I = 4.0 V (p-p)	-	0.04	-	%
		V_{CC} = 9.0 V; V_I = 8.0 V (p-p)	-	0.02	-	%
		f_i = 10 kHz; R_L = 10 kΩ; see Figure 11				
		V_{CC} = 4.5 V; V_I = 4.0 V (p-p)	-	0.12	-	%
		V_{CC} = 9.0 V; V_I = 8.0 V (p-p)	-	0.06	-	%

© NXP B.V. 2008. All rights reserved.

Table 12. Additional dynamic characteristics for 74HC1G66 and 74HCT1G66 *…continued*

GND = 0 V; $t_r = t_f$ = 6.0 ns; C_L = 50 pF; unless otherwise specified. All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(-3dB)}$	−3 dB frequency response	R_L = 50 Ω; C_L = 10 pF; see Figure 12 and 13				
		V_{CC} = 4.5 V	-	180	-	MHz
		V_{CC} = 9.0 V	-	200	-	MHz
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; f_i = 1 MHz; see Figure 14 and 15				
		V_{CC} = 4.5 V	-	−50	-	dB
		V_{CC} = 9.0 V	-	−50	-	dB

11.3 Test circuits and graphs

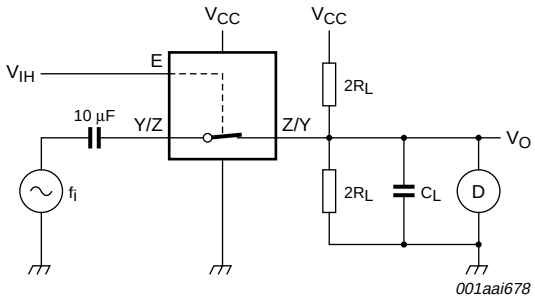
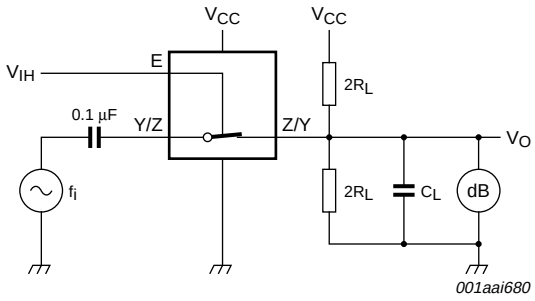


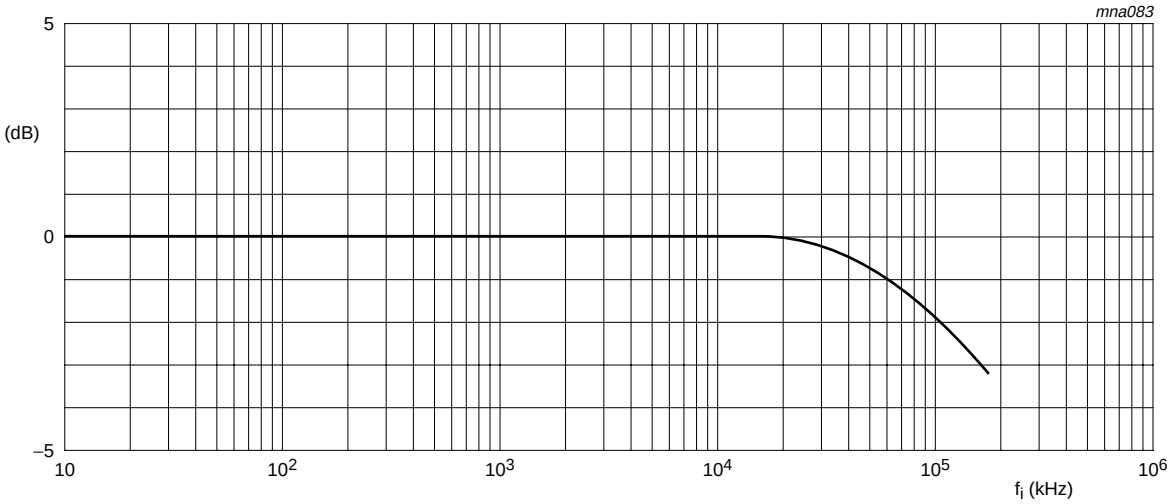
Fig 11. Test circuit for measuring total harmonic distortion



With f_i = 1 MHz adjust the switch input voltage for a 0 dBm level at the switch output, (0 dBm = 1 mW into 50 Ω). Then Increase the input frequency until the dB meter reads −3 dB

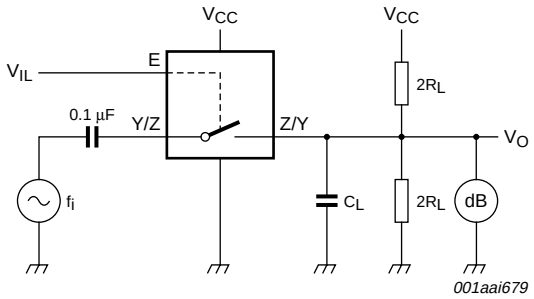
Fig 12. Test circuit for measuring the −3 dB frequency response

© NXP B.V. 2008. All rights reserved.



Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

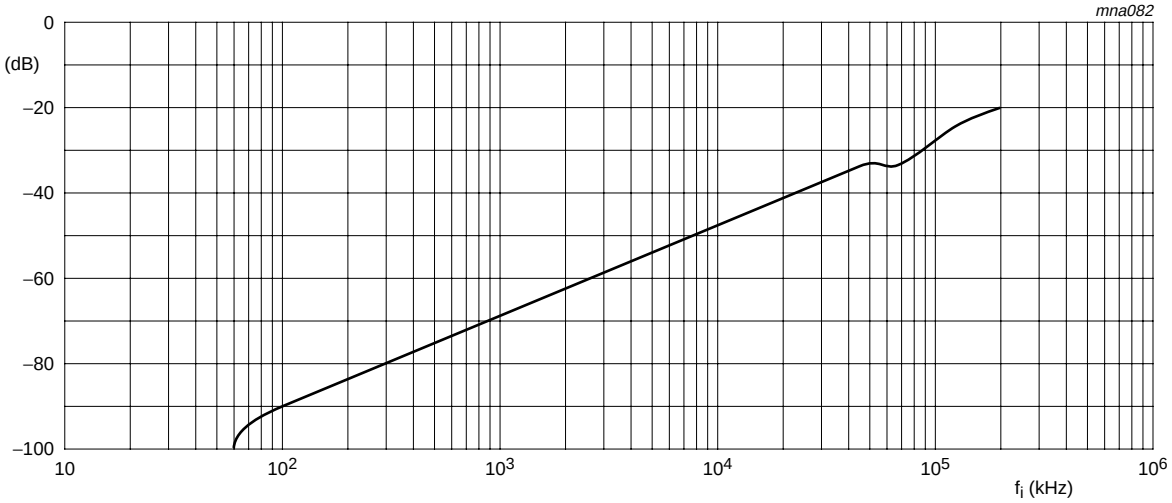
Fig 13. Typical −3 dB frequency response



Adjust the switch input voltage for a 0 dBm level, (0 dBm = 1 mW into 600 Ω)

Fig 14. Test circuit for measuring isolation (OFF-state)

© NXP B.V. 2008. All rights reserved.



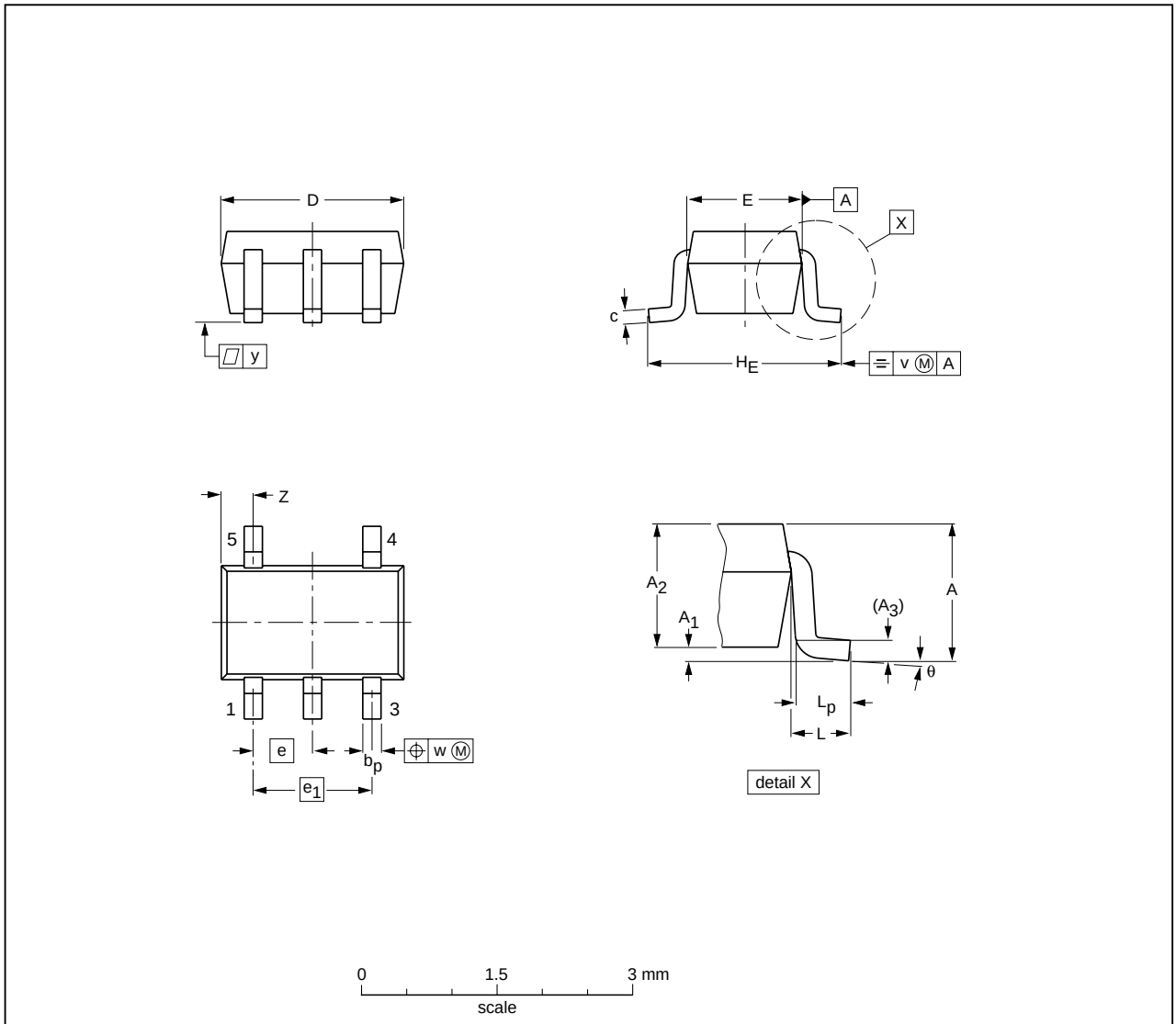
Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

Fig 15. Typical isolation (OFF-state) as a function of frequency

© NXP B.V. 2008. All rights reserved.

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

Note

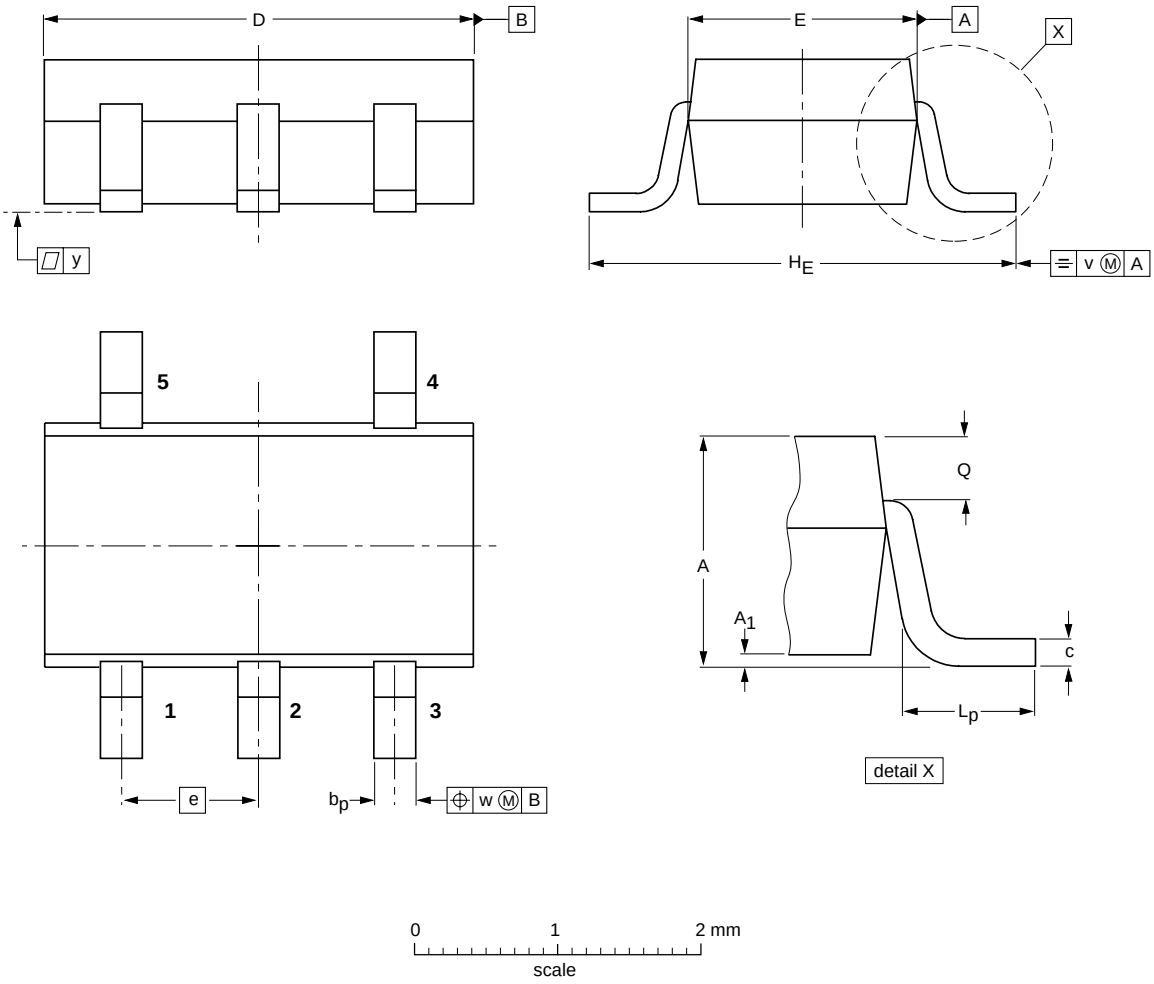
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~00-09-01~~ 03-02-19

Fig 16. Package outline SOT353-1 (TSSOP5)

© NXP B.V. 2008. All rights reserved.

Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig 17. Package outline SOT753 (SC-74A)

© NXP B.V. 2008. All rights reserved.

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic
DUT	Device Under Test

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT1G66_4	20081219	Product data sheet	-	74HC_HCT1G66_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package SOT353 changed to SOT353-1 in Table 1 and Figure 16. • Quick Reference Data and Soldering sections removed. • Section 2 “Features” updated.			
74HC_HCT1G66_3	20020515	Product specification	-	74HC_HCT1G66_2
74HC_HCT1G66_2	20010302	Product specification	-	74HC_HCT1G66_1
74HC_HCT1G66_1	19980803	Product specification	-	-

© NXP B.V. 2008. All rights reserved.

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2008. All rights reserved.

17. Contents

1	**General description**	**1**
2	**Features**	**1**
3	**Ordering information**	**1**
4	**Marking**	**2**
5	**Functional diagram**	**2**
6	**Pinning information**	**2**
6.1	Pinning	2
6.2	Pin description	2
7	**Functional description**	**3**
8	**Limiting values**	**3**
9	**Recommended operating conditions**	**3**
10	**Static characteristics**	**4**
10.1	Test circuits	5
10.2	ON resistance	6
10.3	ON resistance test circuit and graphs	7
11	**Dynamic characteristics**	**7**
11.1	Waveforms and test circuit	9
11.2	Additional dynamic characteristics	10
11.3	Test circuits and graphs	11
12	**Package outline**	**14**
13	**Abbreviations**	**16**
14	**Revision history**	**16**
15	**Legal information**	**17**
15.1	Data sheet status	17
15.2	Definitions	17
15.3	Disclaimers	17
15.4	Trademarks	17
16	**Contact information**	**17**
17	**Contents**	**18**

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2008. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 19 December 2008
Document identifier: 74HC_HCT1G66_4

founded by

PHILIPS