

74HC4024

7-stage binary ripple counter

Rev. 7 — 31 October 2013

Product data sheet

1. General description

The 74HC4024 is a 7-stage binary ripple counter with a clock input (\overline{CP}), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q0 to Q6). The counter advances on the HIGH-to-LOW transition of \overline{CP} . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} . Each counter stage is a static toggle flip-flop. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+80\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

3. Applications

- Frequency dividing circuits
- Time delay circuits.



6. Pinning information

6.1 Pinning

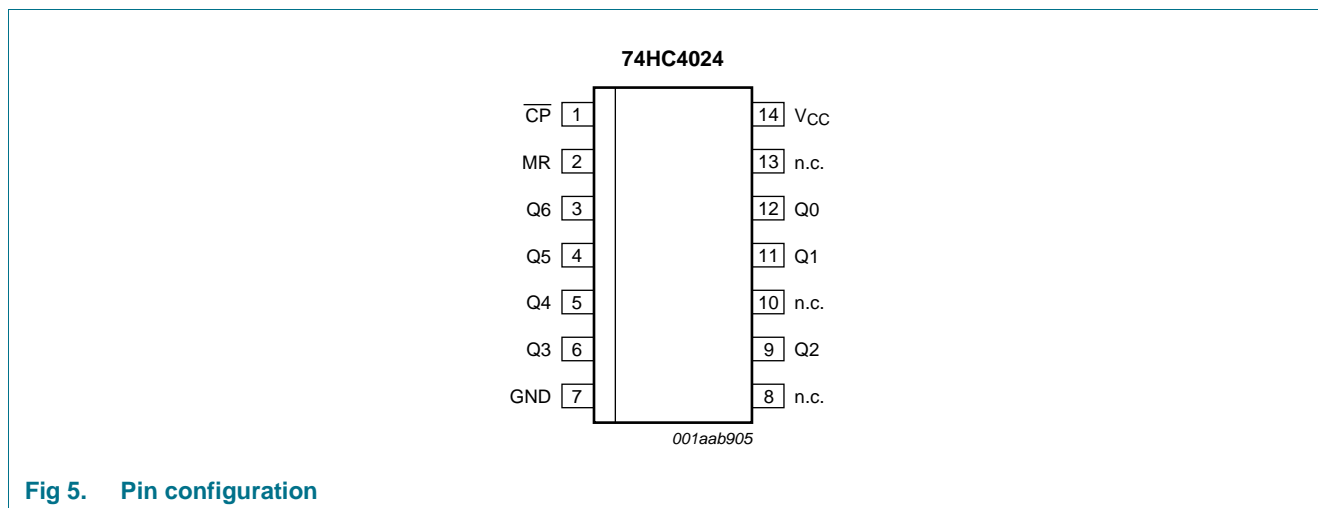


Fig 5. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
CP	1	clock input (HIGH-to-LOW, edge-triggered)
MR	2	master reset input (active HIGH)
Q6, Q5, Q4, Q3, Q2, Q1, Q0	3, 4, 5, 6, 9, 11, 12	parallel output
GND	7	ground (0 V)
n.c.	8, 10, 13	not connected
V _{CC}	14	positive supply voltage

7. Functional description

Table 3. Function table^[1]

Input		Output
MR	$\overline{\text{CP}}$	Q _n
H	X	L
L	↑	no change
	↓	count

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition;
 ↓ = HIGH-to-LOW clock transition.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	DIP14 package	[1] -	750	mW
		SO14 package	[2] -	500	mW
		SSOP14 and TSSOP14 package	[3] -	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For (T)SSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns/V
T_{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	μA
		V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	μA
C _I	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.84	-	-	V
I _O = -5.2 mA; V _{CC} = 6.0 V		5.34	-	-	V	

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.33	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	80	μA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	160	μA

11. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25\text{ °C}$						
t_{pd}	propagation delay	\overline{CP} to Q0; see Figure 6	[1]			
		$V_{CC} = 2.0\text{ V}$	-	47	175	ns
		$V_{CC} = 4.5\text{ V}$	-	17	35	ns
		$V_{CC} = 6.0\text{ V}$	-	14	30	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	14	-	ns
		Qn to Qn+1; see Figure 6	[1]			
		$V_{CC} = 2.0\text{ V}$	-	25	80	ns
		$V_{CC} = 4.5\text{ V}$	-	9	16	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Q0; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	-	63	200	ns
		$V_{CC} = 4.5\text{ V}$	-	23	40	ns
t_t	transition time	see Figure 6	[2]			
		$V_{CC} = 2.0\text{ V}$	-	19	75	ns
		$V_{CC} = 4.5\text{ V}$	-	7	15	ns
t_w	pulse width	\overline{CP} HIGH or LOW; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	80	17	-	ns
		$V_{CC} = 4.5\text{ V}$	16	6	-	ns
		$V_{CC} = 6.0\text{ V}$	14	5	-	ns
		MR HIGH; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	80	22	-	ns
		$V_{CC} = 4.5\text{ V}$	16	8	-	ns
		$V_{CC} = 6.0\text{ V}$	14	6	-	ns
t_{rec}	recovery time	MR to \overline{CP} ; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	50	6	-	ns
		$V_{CC} = 4.5\text{ V}$	10	2	-	ns
f_{max}	maximum frequency	CP; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	6.0	27	-	MHz
		$V_{CC} = 4.5\text{ V}$	30	82	-	MHz
		$V_{CC} = 6.0\text{ V}$	35	98	-	MHz
C_{PD}	power dissipation capacitance	$V_I = GND$ to V_{CC}	[3]	25	-	pF

Table 7. Dynamic characteristics ...continued
 GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
T_{amb} = -40 °C to +85 °C								
t _{pd}	propagation delay	\overline{CP} to Q0; see Figure 6	[1]					
		V _{CC} = 2.0 V	-	-	220	ns		
		V _{CC} = 4.5 V	-	-	44	ns		
		V _{CC} = 6.0 V	-	-	37	ns		
		Qn to Qn+1; see Figure 6	[1]					
		V _{CC} = 2.0 V	-	-	100	ns		
		V _{CC} = 4.5 V	-	-	20	ns		
		V _{CC} = 6.0 V	-	-	17	ns		
		t _{PHL}	HIGH to LOW propagation delay	MR to Q0; see Figure 6				
V _{CC} = 2.0 V	-			-	250	ns		
V _{CC} = 4.5 V	-			-	50	ns		
V _{CC} = 6.0 V	-			-	43	ns		
t _t	transition time	see Figure 6	[2]					
		V _{CC} = 2.0 V	-	-	95	ns		
		V _{CC} = 4.5 V	-	-	19	ns		
		V _{CC} = 6.0 V	-	-	16	ns		
t _w	pulse width	\overline{CP} HIGH or LOW; see Figure 6						
		V _{CC} = 2.0 V	100	-	-	ns		
		V _{CC} = 4.5 V	20	-	-	ns		
		V _{CC} = 6.0 V	17	-	-	ns		
		MR HIGH; see Figure 6						
		V _{CC} = 2.0 V	100	-	-	ns		
		V _{CC} = 4.5 V	20	-	-	ns		
		V _{CC} = 6.0 V	17	-	-	ns		
		t _{rec}	recovery time	MR to \overline{CP} ; see Figure 6				
				V _{CC} = 2.0 V	65	-	-	ns
V _{CC} = 4.5 V	13			-	-	ns		
V _{CC} = 6.0 V	11			-	-	ns		
f _{max}	maximum frequency	CP; see Figure 6						
		V _{CC} = 2.0 V	4.8	-	-	MHz		
		V _{CC} = 4.5 V	24	-	-	MHz		
		V _{CC} = 6.0 V	28	-	-	MHz		

Table 7. Dynamic characteristics ...continued
 $GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; see [Figure 7](#).

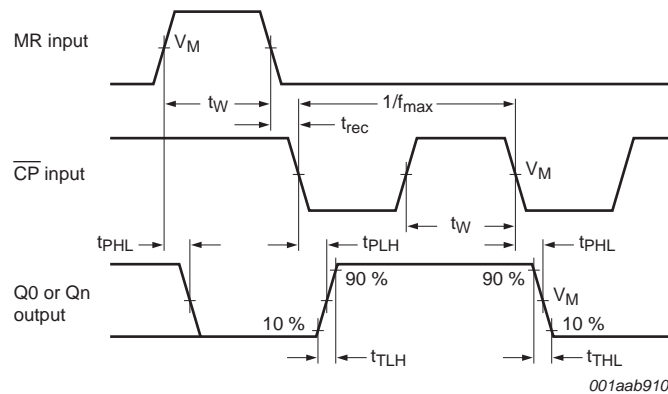
Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$								
t_{pd}	propagation delay	$\overline{\text{CP}}$ to Q0; see Figure 6	[1]					
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	265	ns		
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	53	ns		
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	45	ns		
		Qn to Qn+1; see Figure 6	[1]					
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	120	ns		
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	24	ns		
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	20	ns		
		t_{PHL}	HIGH to LOW propagation delay	MR to Q0; see Figure 6				
$V_{\text{CC}} = 2.0\text{ V}$	-			-	300	ns		
$V_{\text{CC}} = 4.5\text{ V}$	-			-	60	ns		
$V_{\text{CC}} = 6.0\text{ V}$	-			-	51	ns		
t_t	transition time	see Figure 6	[2]					
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	110	ns		
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	22	ns		
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	19	ns		
t_w	pulse width	$\overline{\text{CP}}$ HIGH or LOW; see Figure 6						
		$V_{\text{CC}} = 2.0\text{ V}$	120	-	-	ns		
		$V_{\text{CC}} = 4.5\text{ V}$	24	-	-	ns		
		$V_{\text{CC}} = 6.0\text{ V}$	20	-	-	ns		
		MR HIGH; see Figure 6						
		$V_{\text{CC}} = 2.0\text{ V}$	120	-	-	ns		
		$V_{\text{CC}} = 4.5\text{ V}$	24	-	-	ns		
		$V_{\text{CC}} = 6.0\text{ V}$	20	-	-	ns		
		t_{rec}	recovery time	MR to $\overline{\text{CP}}$; see Figure 6				
				$V_{\text{CC}} = 2.0\text{ V}$	75	-	-	ns
$V_{\text{CC}} = 4.5\text{ V}$	15			-	-	ns		
$V_{\text{CC}} = 6.0\text{ V}$	13			-	-	ns		

Table 7. Dynamic characteristics ...continued
GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum frequency	CP; see Figure 6				
		$V_{\text{CC}} = 2.0 \text{ V}$	4.0	-	-	MHz
		$V_{\text{CC}} = 4.5 \text{ V}$	20	-	-	MHz
		$V_{\text{CC}} = 6.0 \text{ V}$	24	-	-	MHz

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \sum(C_L \times V_{\text{CC}}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{\text{CC}}^2 \times f_o)$ = sum of outputs.

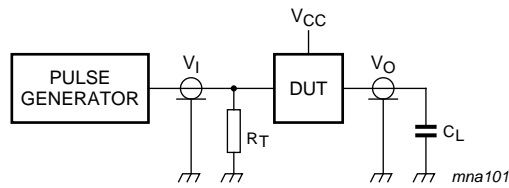
12. Waveforms



Also showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock ($\overline{\text{CP}}$) recovery time.

$$V_M = 0.5 \times V_I.$$

Fig 6. Waveforms showing the clock ($\overline{\text{CP}}$) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



Test data is given in [Table 8](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 8. Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

13. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

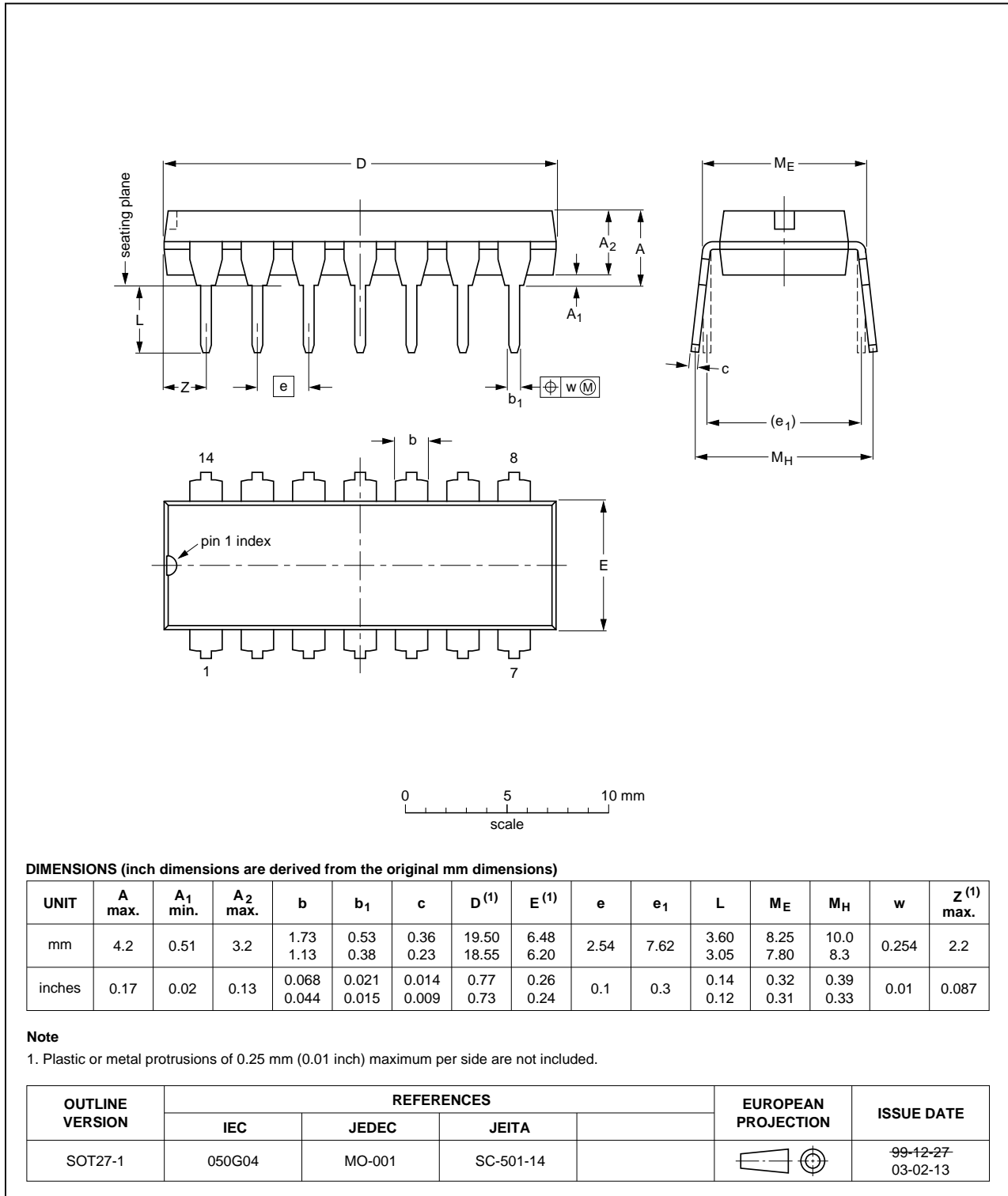


Fig 8. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

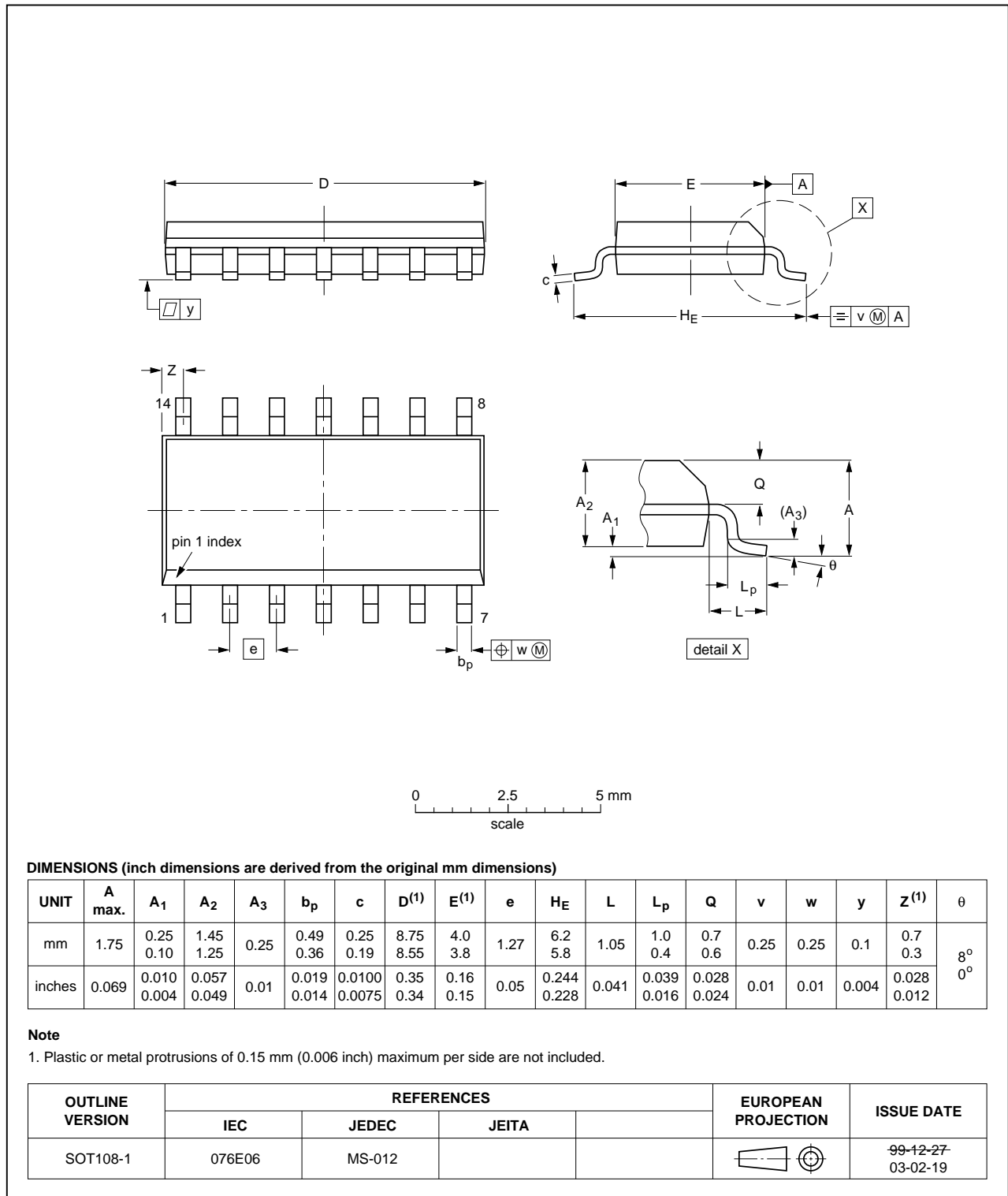


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

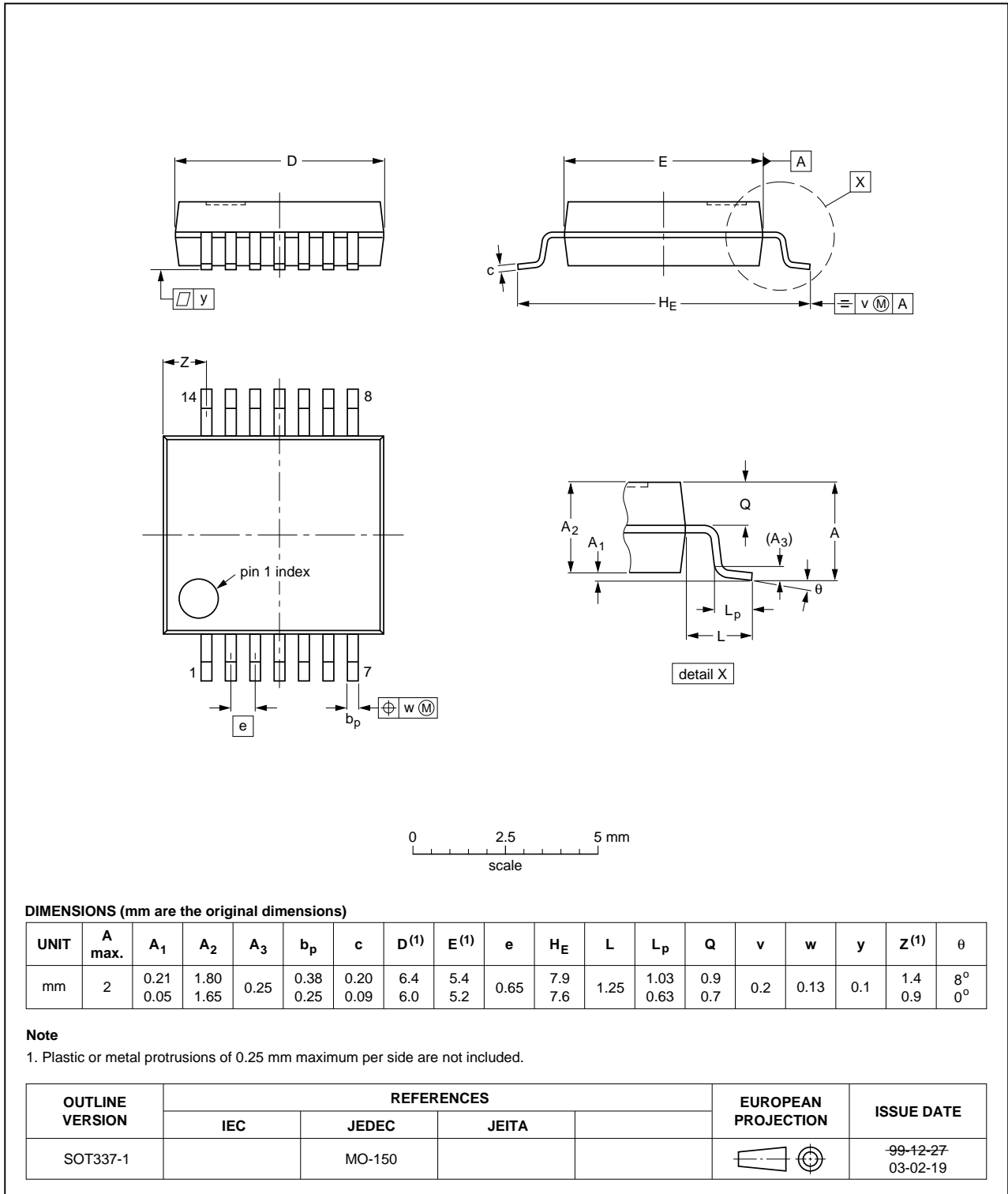


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

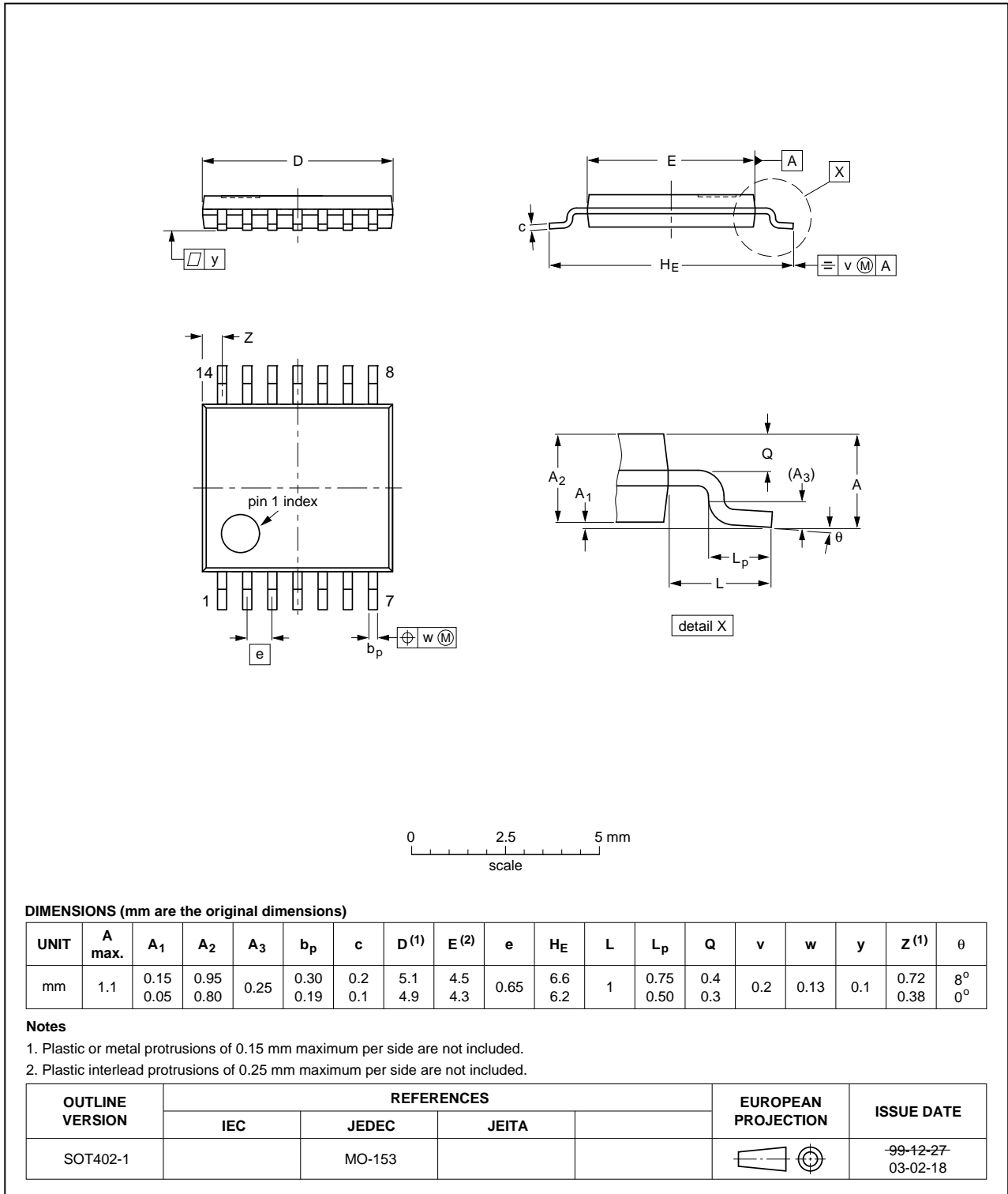


Fig 11. Package outline SOT402-1 (TSSOP14)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4024 v.7	20131031	Product data sheet	-	74HC4024 v.6
Modifications:	<ul style="list-style-type: none"> General description updated. 			
74HC4024 v.6	20120823	Product data sheet	-	74HC4024 v.5
74HC4024 v.4	20100929	Product data sheet	-	74HC4024 v.3
74HC4024 v.3	20041112	Product data sheet	-	74HC_HCT4024_CNV v.2
74HC_HCT4024_CNV v.2	19970901	Product specification	-	74HC_HCT4024 v.1
74HC_HCT4024 v.1	19901201	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	3
8	Limiting values	4
9	Recommended operating conditions	4
10	Static characteristics	5
11	Dynamic characteristics	7
12	Waveforms	10
13	Package outline	12
14	Abbreviations	16
15	Revision history	16
16	Legal information	17
16.1	Data sheet status	17
16.2	Definitions	17
16.3	Disclaimers	17
16.4	Trademarks	18
17	Contact information	18
18	Contents	19

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 31 October 2013

Document identifier: 74HC4024