

74HCT534

5 V octal D-type flip-flop; positive-edge trigger; inverting;
3-state

Rev. 03 — 18 October 2004

Product data sheet

1. General description

The 74HCT534 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HCT534 is specified in compliance with JEDEC standard no. 7A.

The 74HCT534 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 74HCT534 is functionally identical to the 74HCT374, but has inverted outputs.

2. Features

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input.

3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Q_n}$	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	13	-	ns
f_{max}	maximum clock frequency	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	-	40	-	MHz
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance per flip-flop	$C_L = 50\text{ pF}$; $V_{CC} = 4.5\text{ V}$ [1] [2]	-	19	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

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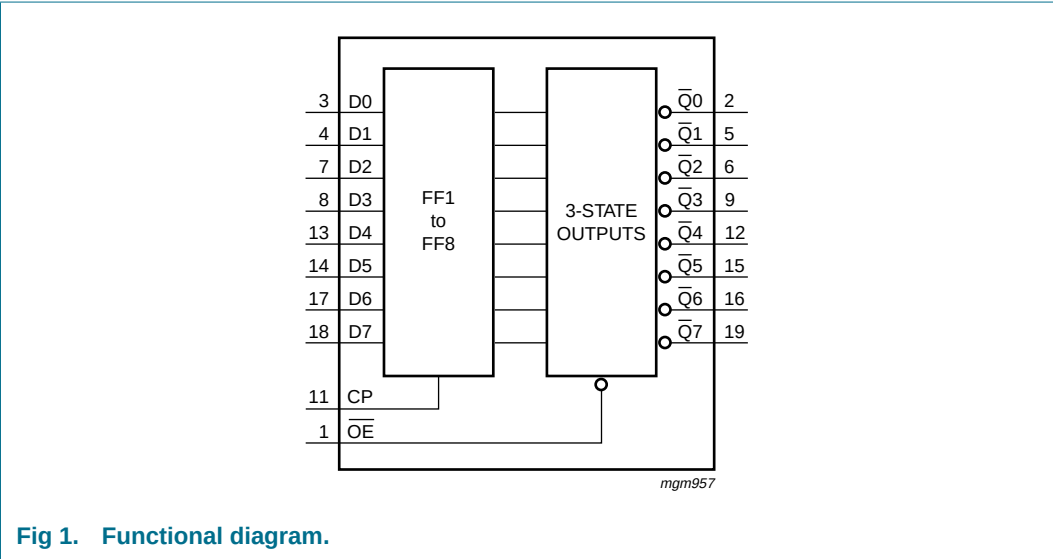
V_{CC} = supply voltage in Volts;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
 [2] The condition is $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCT534N	−40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT534D	−40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

5. Functional diagram



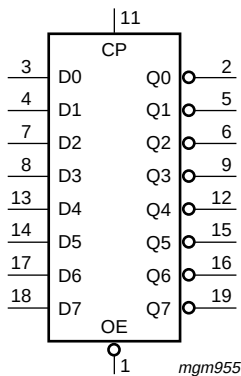


Fig 2. Logic symbol.

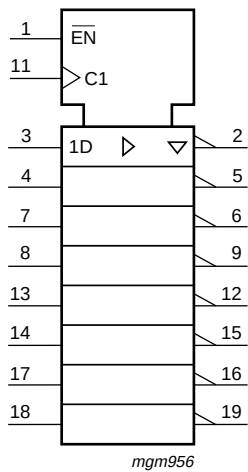


Fig 3. IEC logic symbol.

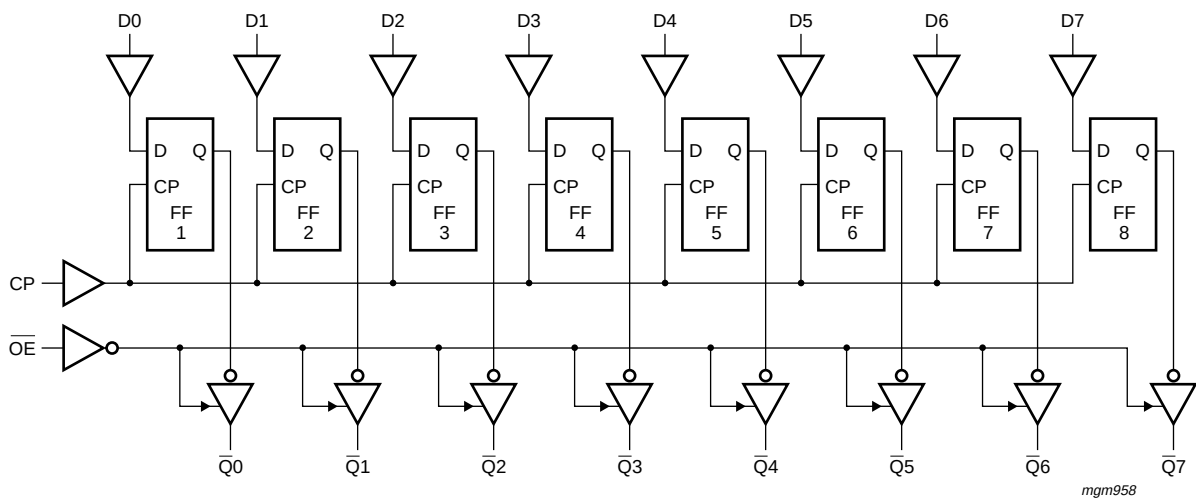
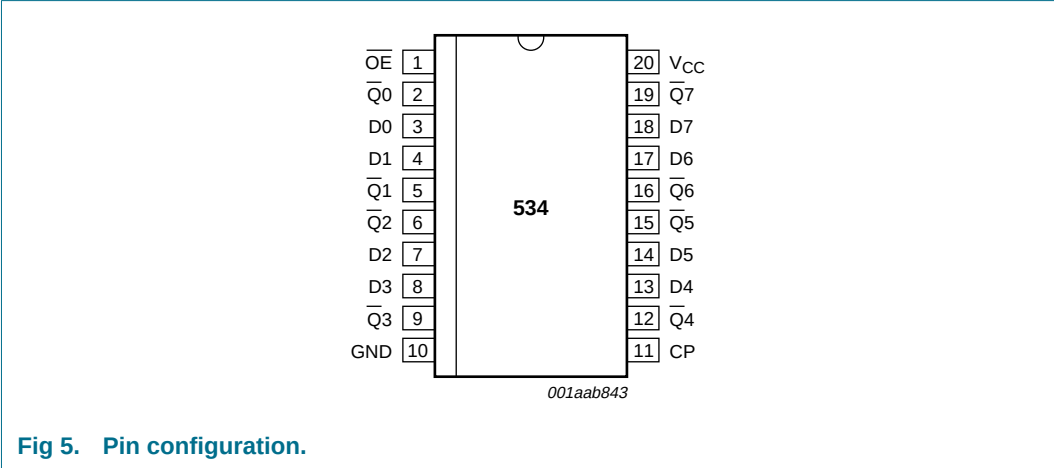


Fig 4. Logic diagram.



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
$\overline{Q0}$	2	3-state output
D0	3	data input
D1	4	data input
$\overline{Q1}$	5	3-state output
$\overline{Q2}$	6	3-state output
D2	7	data input
D3	8	data input
$\overline{Q3}$	9	3-state output
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge-triggered)
$\overline{Q4}$	12	3-state output
D4	13	data input
D5	14	data input
$\overline{Q5}$	15	3-state output
$\overline{Q6}$	16	3-state output
D6	17	data input
D7	18	data input
$\overline{Q7}$	19	3-state output
V _{CC}	20	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table ^[1]

Operating mode	Input			Internal flip-flops	Output $\bar{Q}_n$
	$\overline{OE}$	CP	Dn		
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
 Z = high-impedance OFF-state;
 ↑ = LOW-to-HIGH clock transition.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	±20	mA
I_{OK}	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	±20	mA
I_O	output source or sink current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	±35	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±70	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	power dissipation				
	DIP20 package		^[1] -	750	mW
	SO20 package		^[2] -	500	mW

- [1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.
 [2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V

Table 6: Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times	$V_{CC} = 4.5$ V	-	6.0	500	ns
T_{amb}	ambient temperature	see Section 10 and 11	-40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V				
		$I_O = -20$ μ A	4.4	4.5	-	V
		$I_O = -6$ mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V				
		$I_O = 20$ μ A	-	0	0.1	V
		$I_O = 6.0$ mA	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	± 0.1	μ A
I_{OZ}	3-state OFF current	$V_I = V_{IH}$ or V_{IL} ; other inputs V_{CC} or GND; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	± 0.5	μ A
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	μ A
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V; other inputs $V_I = V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		pin $\overline{OE}$	-	125	450	μ A
		pin CP	-	90	325	μ A
		pins Dn	-	35	125	μ A
C_I	input capacitance		-	3.5	-	pF
$T_{amb} = -40$ °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V				
		$I_O = -20$ μ A	4.4	-	-	V
		$I_O = -6$ mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V				
		$I_O = 20$ μ A	-	-	0.1	V
		$I_O = 6.0$ mA	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	± 1.0	μ A

Table 7: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	3-state OFF current	$V_I = V_{IH}$ or V_{IL} ; other inputs V_{CC} or GND; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	± 5	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V; other inputs $V_I = V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
	pin $\overline{OE}$		-	-	560	μA
	pin CP		-	-	405	μA
	pins Dn		-	-	155	μA
$T_{amb} = -40$ °C to $+125$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V				
	$I_O = -20$ μA		4.4	-	-	V
	$I_O = -6$ mA		3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V				
	$I_O = 20$ μA		-	-	0.1	V
	$I_O = 6.0$ mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	± 1.0	μA
I_{OZ}	3-state OFF current	$V_I = V_{IH}$ or V_{IL} ; other inputs V_{CC} or GND; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	± 10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V; other inputs $V_I = V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
	pin $\overline{OE}$		-	-	610	μA
	pin CP		-	-	440	μA
	pins Dn		-	-	170	μA

11. Dynamic characteristics

Table 8: Dynamic characteristicsGND = 0 V; $V_{CC} = 4.5$ V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; see [Figure 9](#)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL} , t_{PLH}	propagation delay CP to $\overline{Qn}$	see Figure 6				
		$C_L = 50$ pF; $V_{CC} = 4.5$ V	-	16	30	ns
		$C_L = 15$ pF; $V_{CC} = 5$ V	-	13	-	
t_{PZH} , t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Qn}$	see Figure 7	-	16	30	ns

Table 8: Dynamic characteristics ...continuedGND = 0 V; $V_{CC} = 4.5$ V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; see [Figure 9](#)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Qn}$	see Figure 7	-	18	30	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6	-	5	12	ns
t_W	clock pulse width HIGH or LOW	see Figure 6	23	14	-	ns
t_{su}	set-up time Dn to CP	see Figure 8	12	4	-	ns
t_h	hold time Dn to CP	see Figure 8	5	-1	-	ns
f_{max}	maximum clock pulse frequency	see Figure 6				
		$C_L = 50$ pF; $V_{CC} = 4.5$ V	22	36	-	MHz
		$C_L = 15$ pF; $V_{CC} = 5$ V	-	40	-	MHz
C_{PD}	power dissipation capacitance per flip-flop	[1] [2]	-	19	-	pF

 $T_{amb} = -40$ °C to $+85$ °C

t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Qn}$	see Figure 6	-	-	38	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Qn}$	see Figure 7	-	-	38	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Qn}$	see Figure 7	-	-	38	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6	-	-	15	ns
t_W	clock pulse width HIGH or LOW	see Figure 6	29	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 8	15	-	-	ns
t_h	hold time Dn to CP	see Figure 8	5	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 6	18	-	-	MHz

 $T_{amb} = -40$ °C to $+125$ °C

t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Qn}$	see Figure 6	-	-	45	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Qn}$	see Figure 7	-	-	45	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Qn}$	see Figure 7	-	-	45	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6	-	-	18	ns
t_W	clock pulse width HIGH or LOW	see Figure 6	35	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 8	18	-	-	ns
t_h	hold time Dn to CP	see Figure 8	5	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 6	15	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

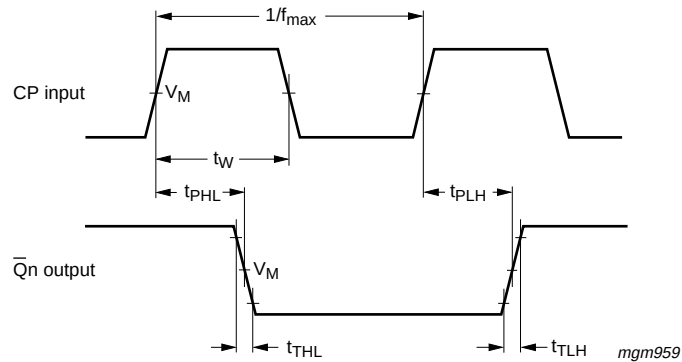
V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

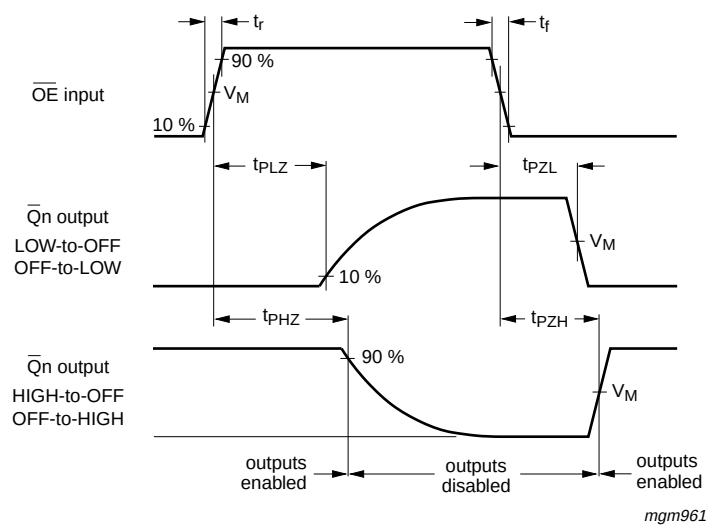
[2] The condition is $V_i = \text{GND to } V_{CC} - 1.5$ V.

12. Waveforms



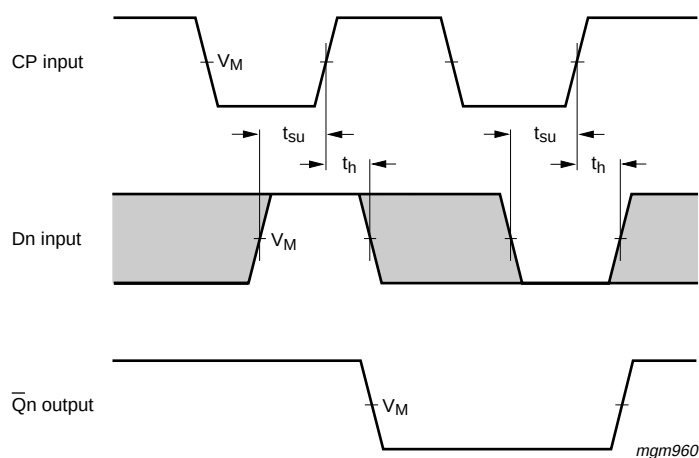
$V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig 6. Waveforms showing the clock (CP) to output ($\bar{Q}_n$) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.



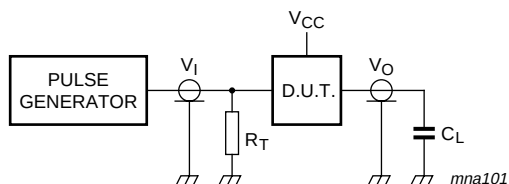
$V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig 7. Waveforms showing the 3-state enable and disable times.



$V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig 8. Waveforms showing the data set-up and hold times for Dn input.



Definitions test circuits:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance (See [Section 11](#) for the value).

Fig 9. Load circuitry for switching times.

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

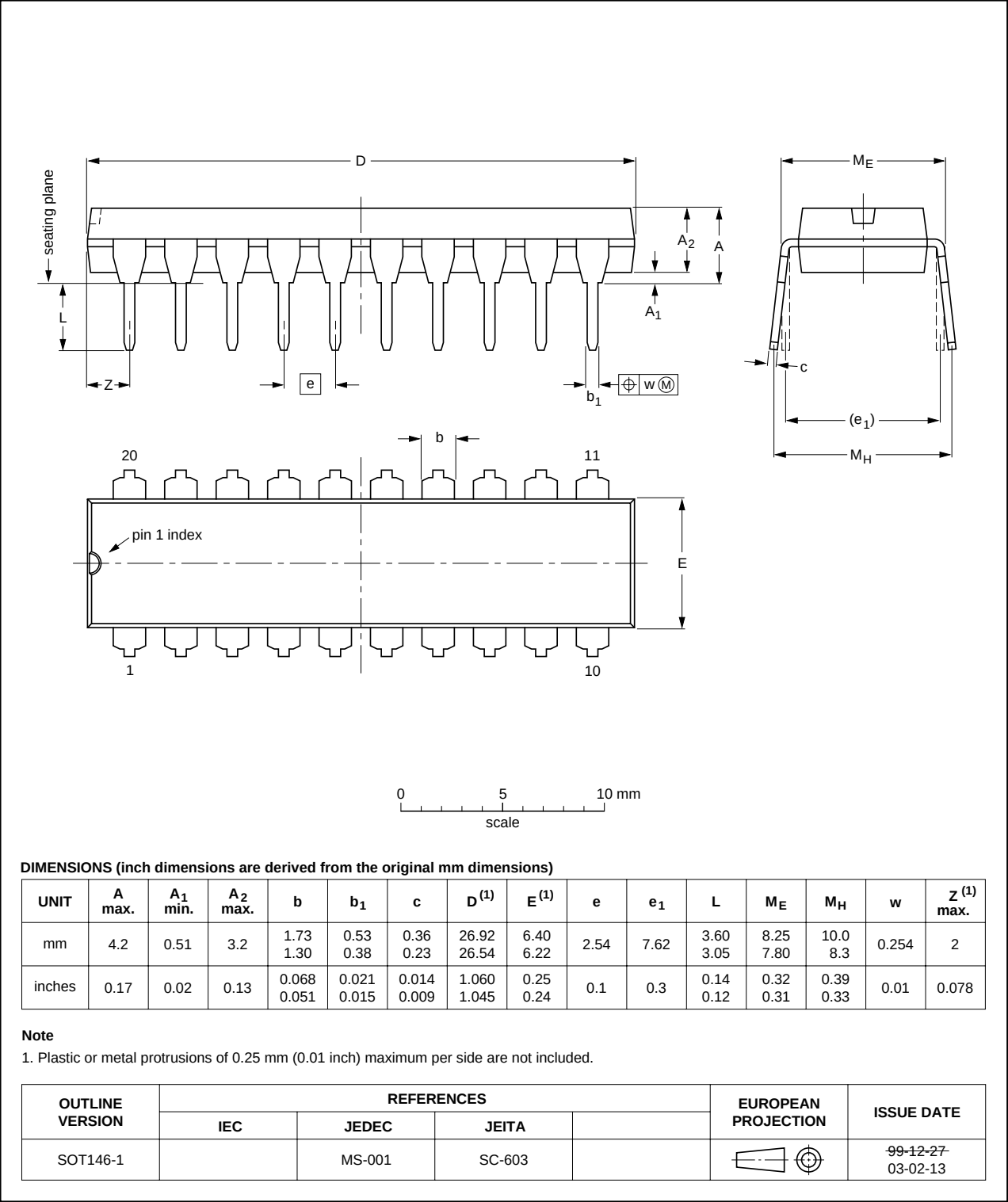


Fig 10. Package outline SOT146 (DIP20).

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

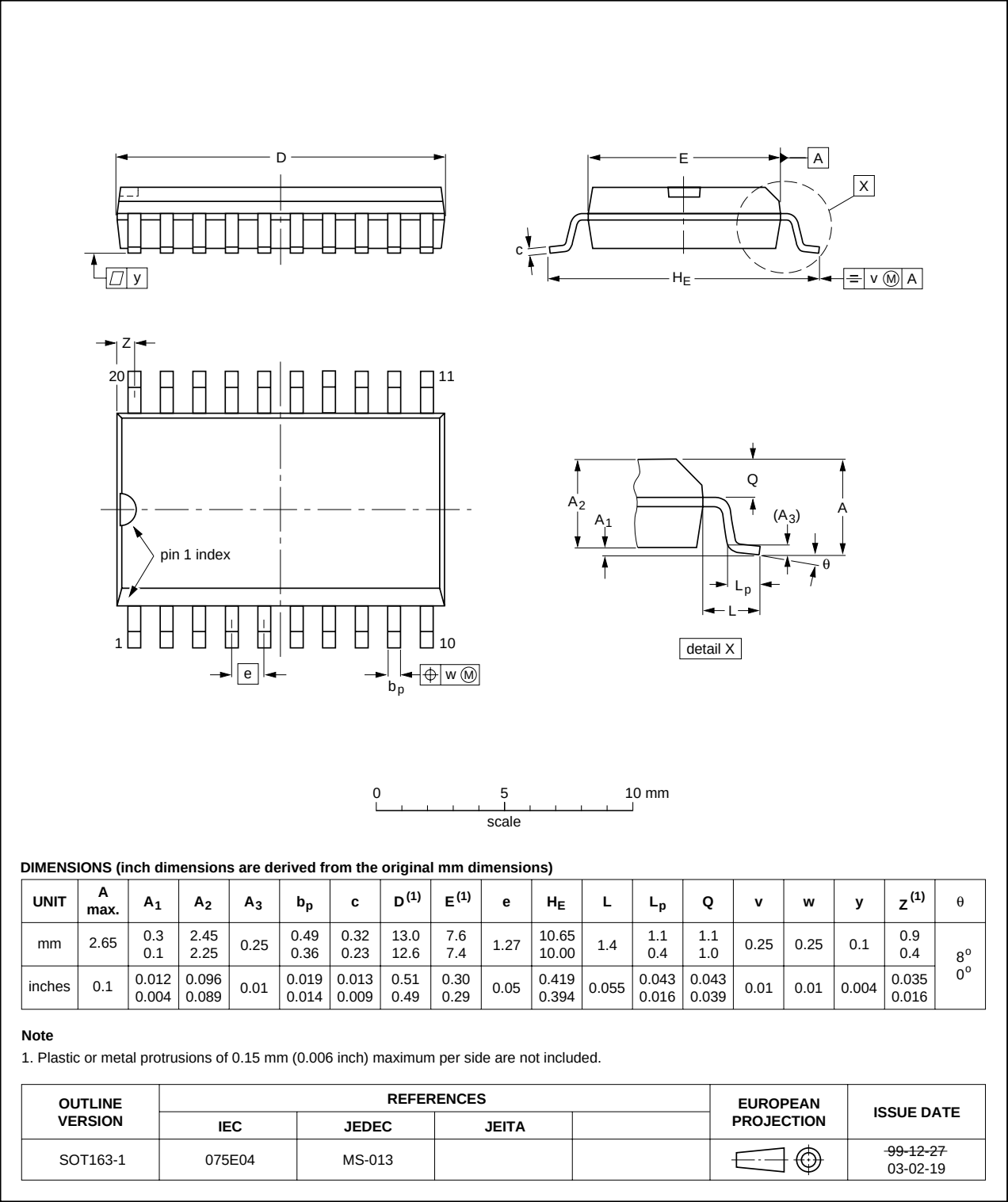


Fig 11. Package outline SOT163 (SO20).

14. Revision history

Table 9: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HCT534_3	20041018	Product data sheet	-	9397 750 13817	74HC_HCT534_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Information related to 74HC534 type is deleted • Reference to family specifications is replaced by the actual information.				
74HC_HCT534_CNV_2	19980410	Product specification	-	-	74HC_HCT534_1

15. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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