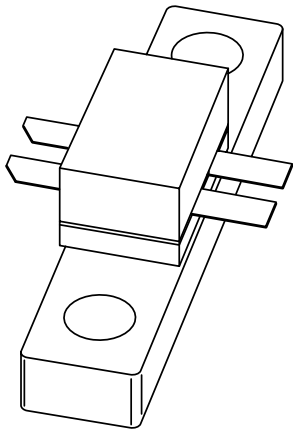


DATA SHEET



BLF245B

VHF push-pull power MOS
transistor

Product specification
Supersedes data of 2000 Oct 17

2003 Aug 04

VHF push-pull power MOS transistor

BLF245B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

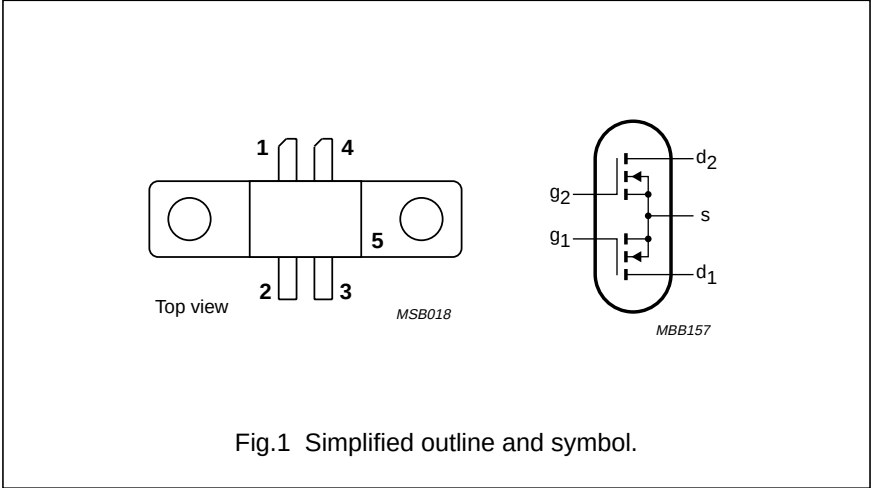
Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT279A balanced flange package, with a ceramic cap. The mounting flange provides the common source connection for the transistors.

PINNING - SOT279A

PIN	DESCRIPTION
1	drain 1
2	gate 1
3	gate 2
4	drain 2
5	source

PIN CONFIGURATION



CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ }^{\circ}\text{C}$ in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η _D (%)
CW, class-B	175	28	30	>14	>55

VHF push-pull power MOS transistor

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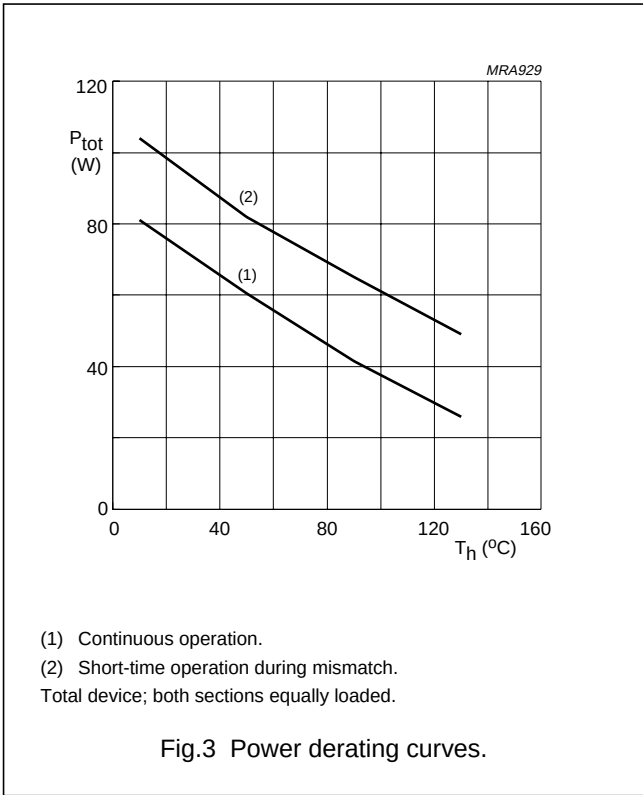
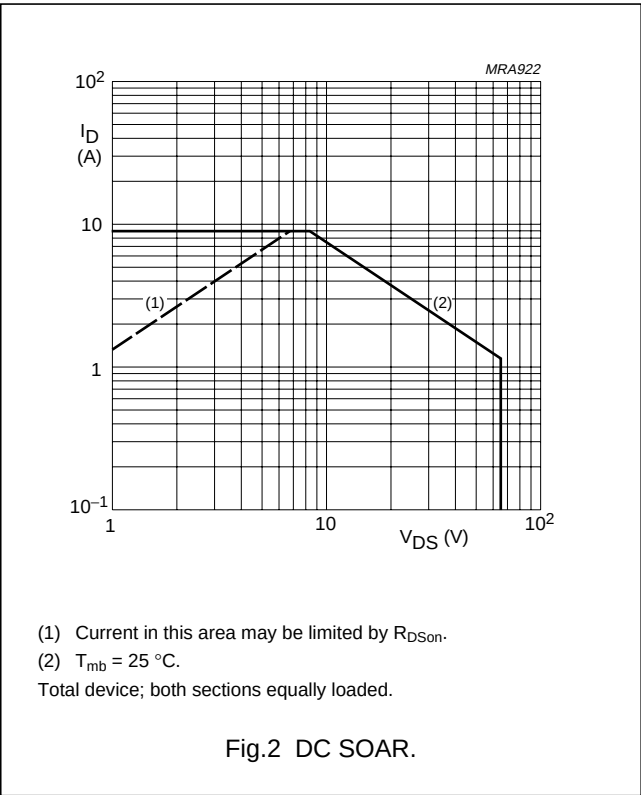
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section unless otherwise specified					
V _{DS}	drain-source voltage		–	65	V
±V _{GS}	gate-source voltage		–	20	V
I _D	DC drain current		–	4.5	A
P _{tot}	total power dissipation	T _{mb} ≤ 25 °C; total device; both sections equally loaded	–	75	W
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-mb}	thermal resistance from junction to mounting base	total device; both sections equally loaded	2.3	K/W
R _{th mb-h}	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.3	K/W



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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

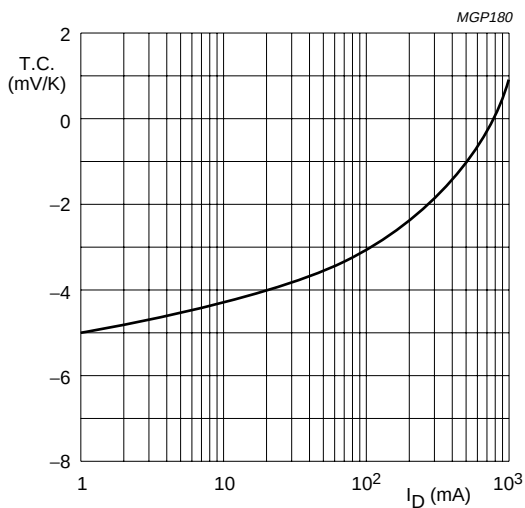
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 5\text{ mA}$; $V_{GS} = 0$	65	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 28\text{ V}$	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS} = 20\text{ V}$; $V_{DS} = 0$	–	–	1	μA
V_{GSth}	gate-source threshold voltage	$I_D = 5\text{ mA}$; $V_{DS} = 10\text{ V}$	2	–	4.5	V
g_{fs}	forward transconductance	$I_D = 0.75\text{ A}$; $V_{DS} = 10\text{ V}$	600	850	–	mS
R_{DSon}	drain-source on-state resistance	$I_D = 0.75\text{ A}$; $V_{GS} = 10\text{ V}$	–	0.8	1.5	Ω
I_{DSX}	on-state drain current	$V_{GS} = 10\text{ V}$; $V_{DS} = 10\text{ V}$	–	5	–	A
C_{is}	input capacitance	$V_{GS} = 0$; $V_{DS} = 28\text{ V}$; $f = 1\text{ MHz}$	–	60	–	pF
C_{os}	output capacitance	$V_{GS} = 0$; $V_{DS} = 28\text{ V}$; $f = 1\text{ MHz}$	–	40	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 28\text{ V}$; $f = 1\text{ MHz}$	–	4.5	–	pF

 V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			

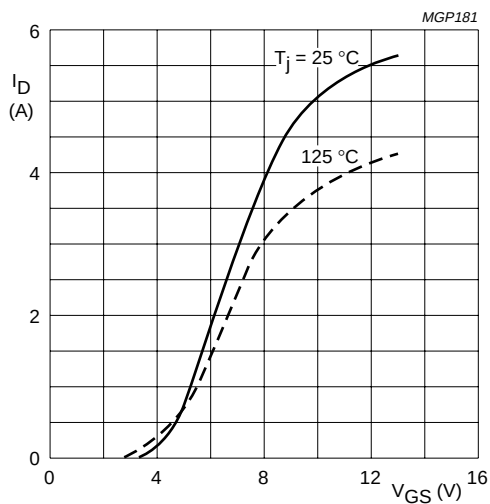
VHF push-pull power MOS transistor

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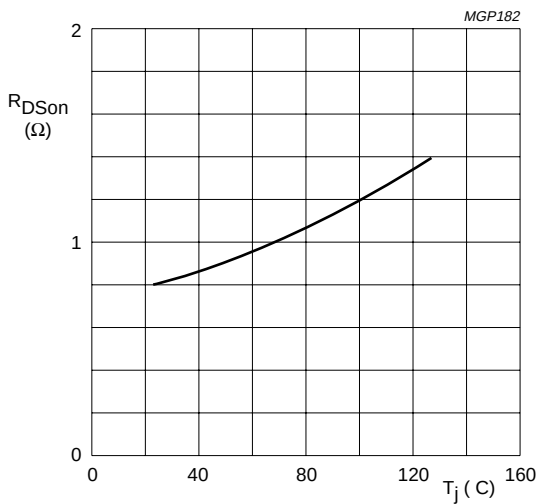
$V_{DS} = 10\text{ V}$.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values per section.



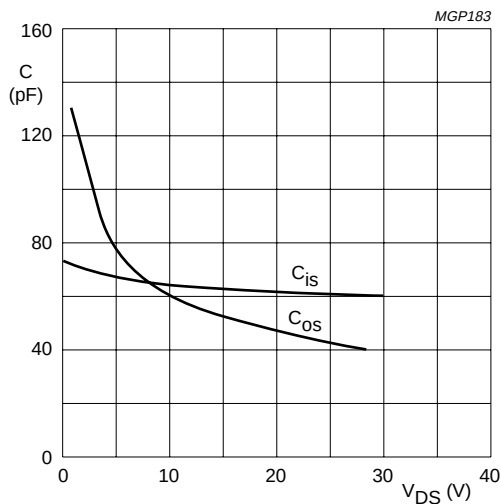
$V_{DS} = 10\text{ V}$.

Fig.5 Drain current as a function of gate-source voltage; typical values per section.



$I_D = 0.75\text{ A}$; $V_{GS} = 10\text{ V}$.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values per section.

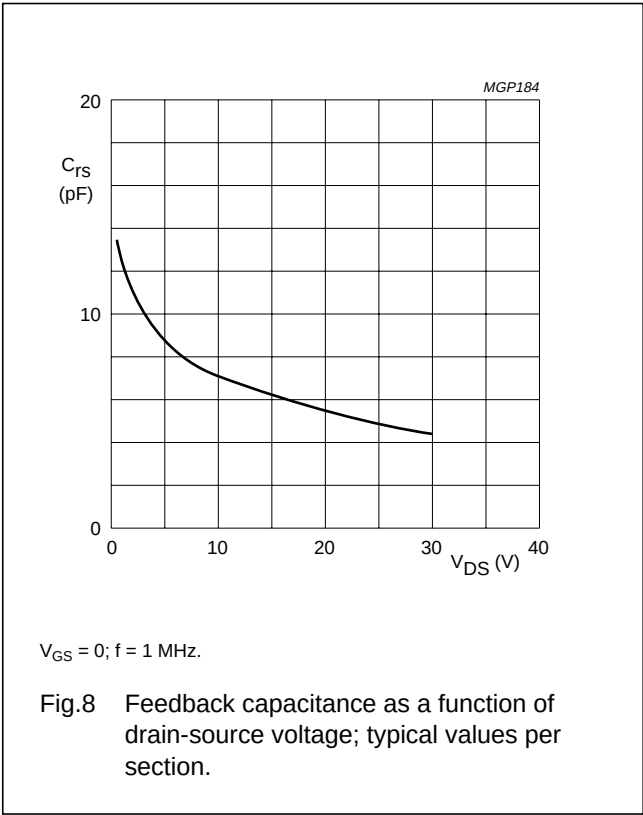


$V_{GS} = 0$; $f = 1\text{ MHz}$.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values per section.

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APPLICATION INFORMATION FOR CLASS-B OPERATION

$T_h = 25\text{ }^{\circ}\text{C}$; $R_{th\text{ mb-h}} = 0.3\text{ K/W}$; unless otherwise specified.
RF performance in a push-pull, common source, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	2×25	30	>14 typ. 18	>55 typ. 65

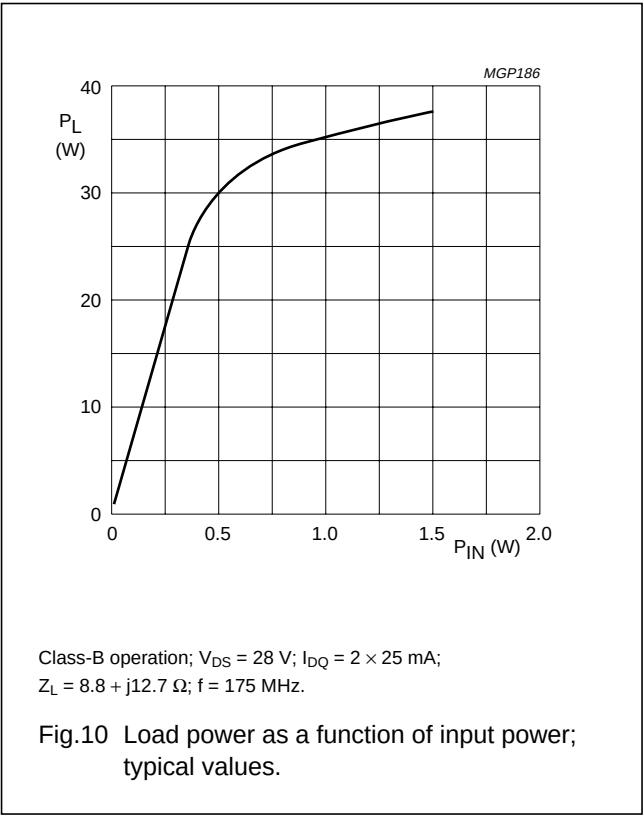
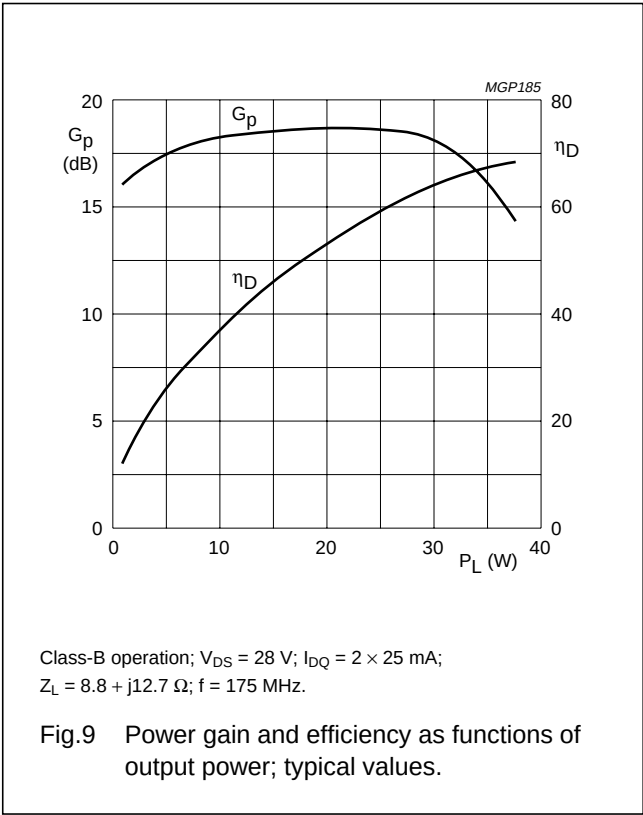
Ruggedness in class-B operation

The BLF245B is capable of withstanding a load mismatch corresponding to $V_{SWR} = 50$ through all phases, under the following conditions:

$V_{DS} = 28\text{ V}$, $f = 175\text{ MHz}$ at rated output power.

VHF push-pull power MOS transistor

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VHF push-pull power MOS transistor

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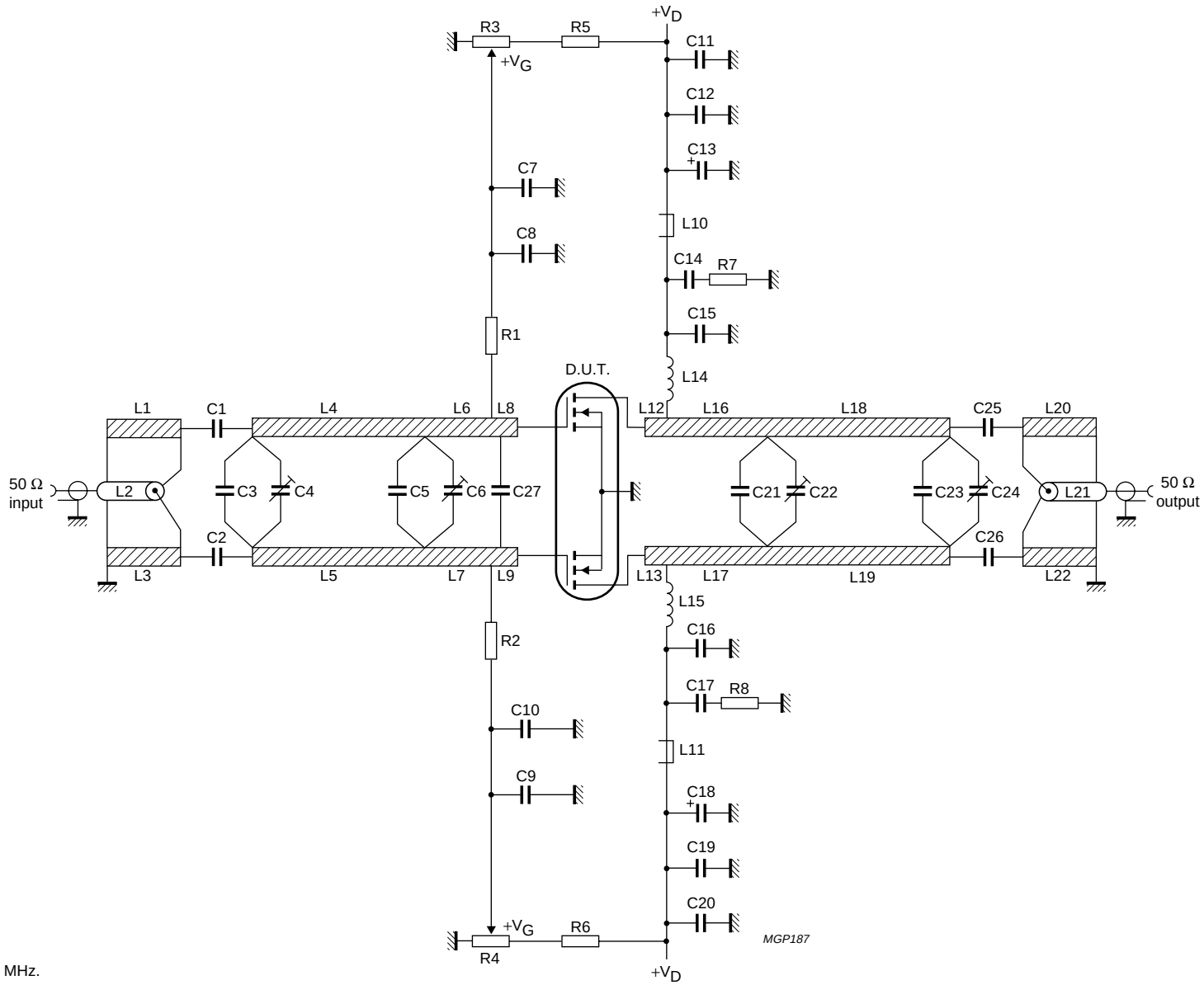


Fig.11 Test circuit for class-B operation.

VHF push-pull power MOS transistor

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List of components (see Fig.11)

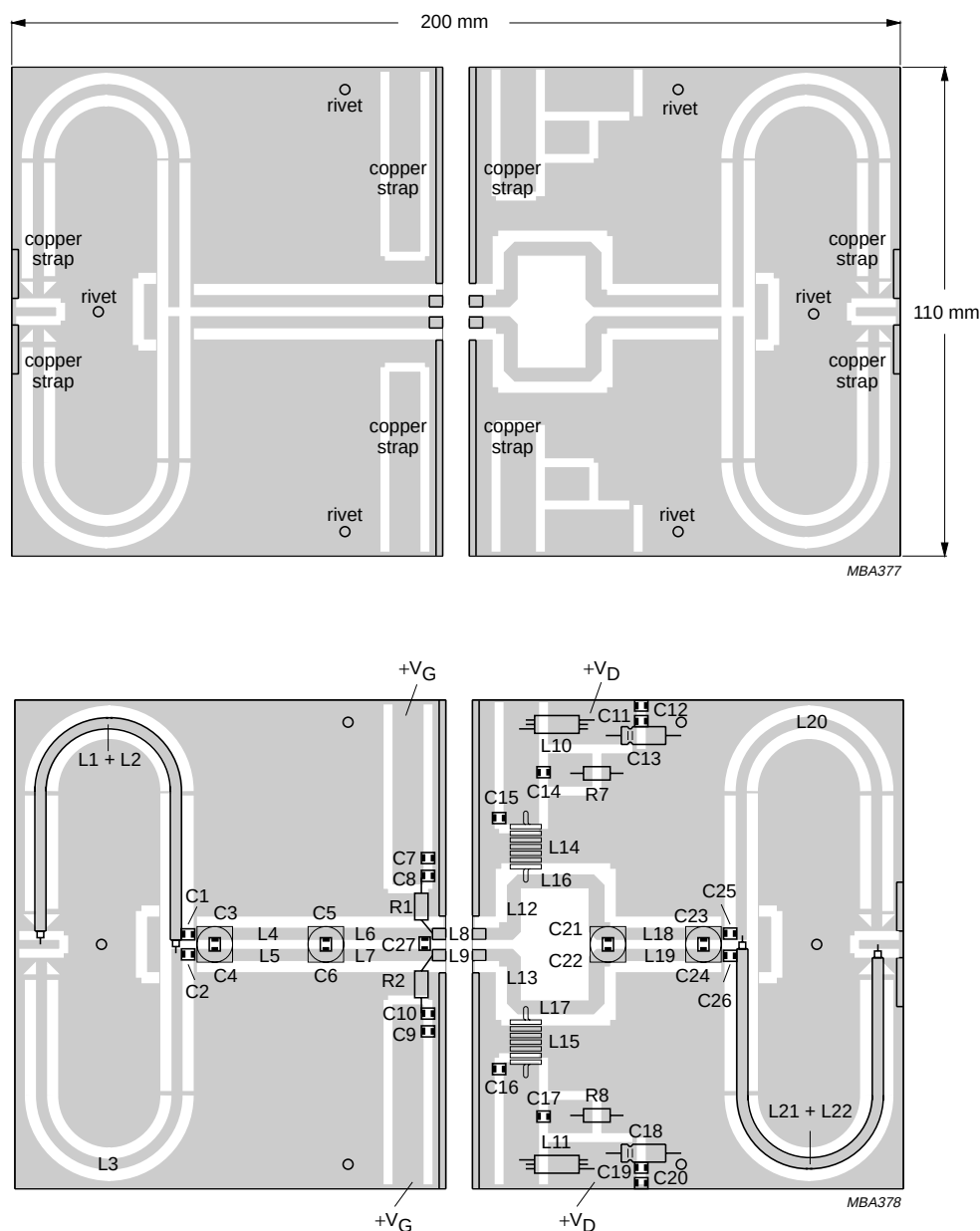
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1,C2	multilayer ceramic chip capacitor; note 1	270 pF		
C3	multilayer ceramic chip capacitor; note 1	24 pF		
C4	film dielectric trimmer	4 to 60 pF		2222 809 08002
C5, C25, C26	multilayer ceramic chip capacitor; note 1	91 pF		
C6, C22, C24	film dielectric trimmer	5 to 60 pF		2222 809 08003
C7, C9, C12, C14, C17, C19	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C8, C10	multilayer ceramic chip capacitor; note 1	680 pF		
C11, C20	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C13, C18	electrolytic capacitor	10 μ F, 63 V		
C15, C16	multilayer ceramic chip capacitor; note 1	100 pF		
C21, C27	multilayer ceramic chip capacitor; note 1	75 pF		
C23	multilayer ceramic chip capacitor; note 1	36 pF		
L1, L3, L20, L22	stripline; note 2	55 Ω	length 111 mm width 2.5 mm	
L2, L21	semi-rigid cable	50 Ω	length 111 mm ext. dia. 2.2 mm	
L4, L5	stripline; note 2	49.5 Ω	length 28 mm width 3 mm	
L6, L7	stripline; note 2	49.5 Ω	length 22.5 mm width 3 mm	
L8, L9	stripline; note 2	49.5 Ω	length 4.5 mm width 3 mm	
L10, L11	grade 3B Ferroxcube RF choke			4312 020 36642
L12, L13	stripline; note 2	49.5 Ω	length 21 mm width 3 mm	
L14, L15	4 turns enamelled 1 mm copper wire	70 nH	length 9 mm int. dia. 6 mm leads 2 $\times$ 5 mm	
L16, L17	stripline; note 2	49.5 Ω	length 30 mm width 3 mm	
L18, L19	stripline; note 2	49.5 Ω	length 26 mm width 3 mm	
R1, R2	0.4 W metal film resistor	10 Ω		
R3, R4	10 turns potentiometer	50 Ω		
R5, R6	0.4 W metal film resistor	205 k Ω		
R7, R8	0.4 W metal film resistor	10 Ω		

Notes

- American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
- The striplines are on a double copper-clad printed circuit board, with epoxy glass dielectric ($\epsilon_r = 4.5$), thickness $\frac{1}{16}$ inch. The other side of the board is fully metallized and used as a ground plane. The ground planes on each side of the board are connected together by means of copper straps and hollow rivets.

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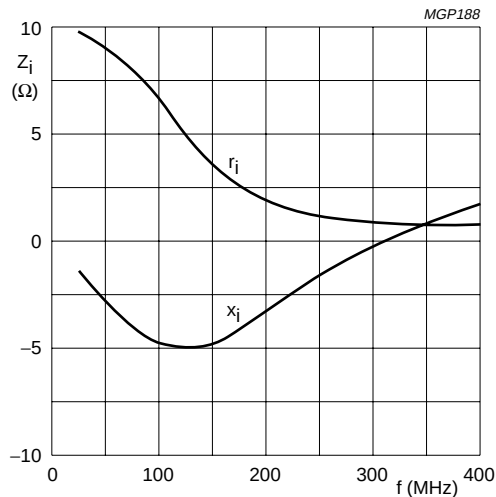


The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of copper straps and hollow rivets for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 175 MHz test circuit.

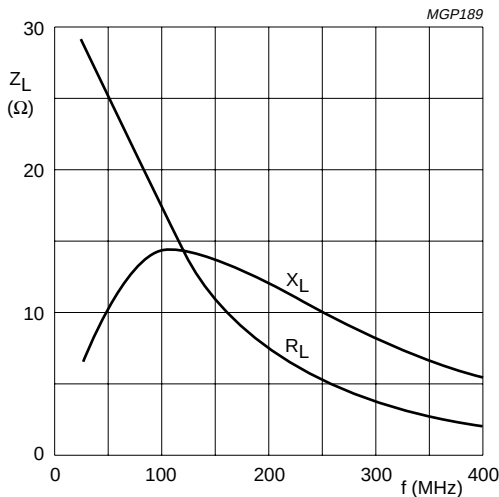
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Class-B operation; $V_{DS} = 28\text{ V}$; $I_{DQ} = 2 \times 25\text{ mA}$;
 $R_{GS} = 10\ \Omega$; $P_L = 30\text{ W}$ (total device).

Fig.13 Input impedance as a function of frequency (series components); typical values per section.



Class-B operation; $V_{DS} = 28\text{ V}$; $I_{DQ} = 2 \times 25\text{ mA}$;
 $R_{GS} = 10\ \Omega$; $P_L = 30\text{ W}$ (total device).

Fig.14 Load impedance as a function of frequency (series components); typical values per section.

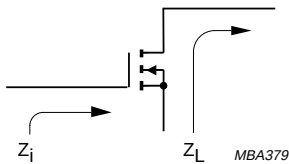
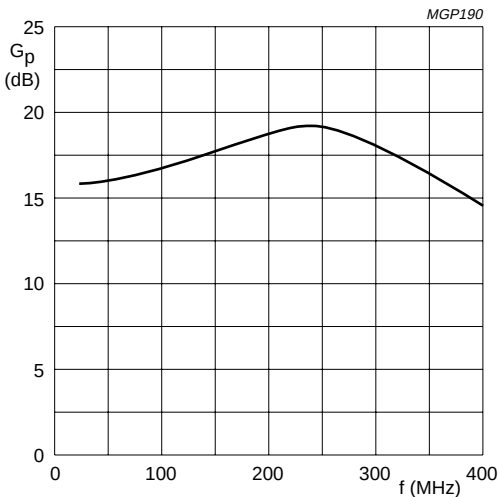


Fig.15 Definition of MOS impedance.



Class-B operation; $V_{DS} = 28\text{ V}$; $I_{DQ} = 2 \times 25\text{ mA}$;
 $R_{GS} = 10\ \Omega$; $P_L = 30\text{ W}$ (total device).

Fig.16 Power gain as a function of frequency; typical values per section.

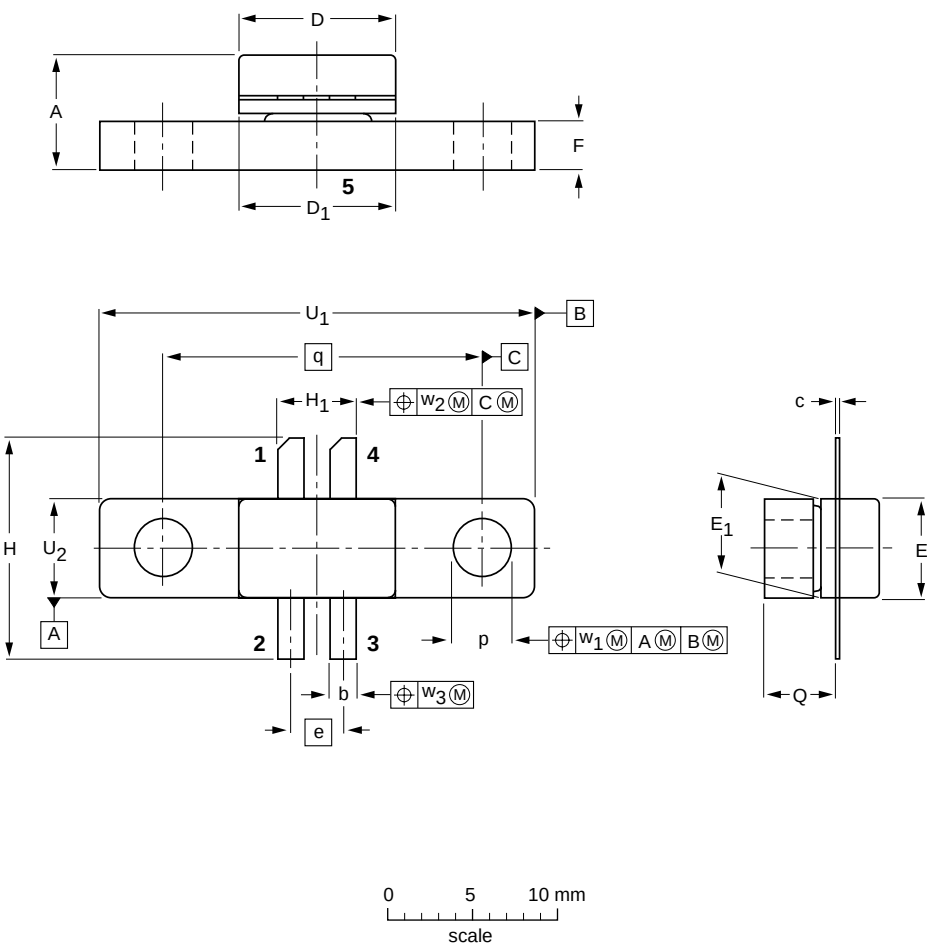
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PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT279A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	e	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	6.84 6.01	1.65 1.40	0.15 0.10	9.25 9.04	9.27 9.02	5.94 5.74	5.97 5.72	3.05	3.05 2.54	12.96 11.94	4.96 4.19	3.48 3.23	4.34 4.04	18.42	24.90 24.64	5.97 5.72	0.25	0.51	0.25
inches	0.269 0.237	0.065 0.055	0.006 0.004	0.364 0.356	0.365 0.355	0.234 0.226	0.235 0.225	0.120	0.120 0.100	0.510 0.470	0.195 0.165	0.137 0.127	0.171 0.159	0.725	0.980 0.970	0.235 0.225	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT279A						99-03-29

VHF push-pull power MOS transistor

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Printed in The Netherlands

613524/06/pp14

Date of release: 2003 Aug 04

Document order number: 9397 750 11596

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