



# BUK9605-30A

## N-channel TrenchMOS logic level FET

Rev. 03 — 19 April 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance

### 1.3 Applications

- Automotive and general purpose power switching

### 1.4 Quick reference data

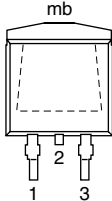
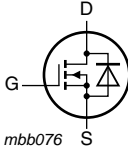
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$	-	-	75	A
$P_{tot}$	total power dissipation		-	-	230	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	4.3	5	m $\Omega$
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	3.9	4.6	m $\Omega$
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}; V_{sup} \leq 25\text{ V}; R_{GS} = 50\text{ }\Omega; V_{GS} = 5\text{ V}; T_{j(init)} = 25\text{ °C}; \text{unclamped}$	-	-	500	mJ



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT404 (D2PAK)**

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

**Table 3. Ordering information**

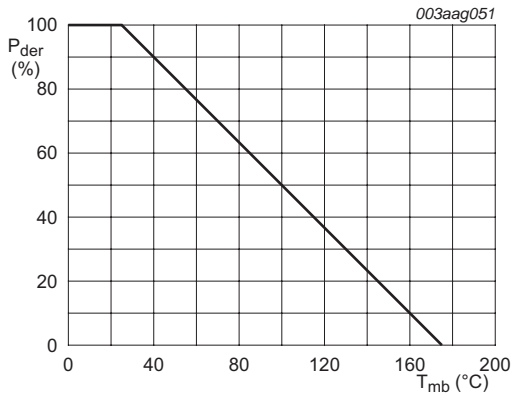
Type number	Package		
	Name	Description	Version
BUK9605-30A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

**Table 4. Limiting values**

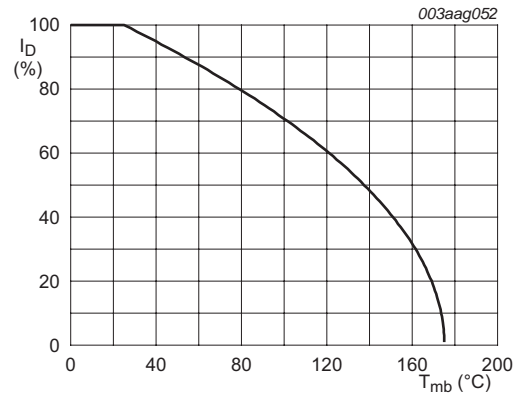
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-10	10	V
$I_D$	drain current	$T_{mb} = 100\text{ °C}$	-	75	A
		$T_{mb} = 25\text{ °C}$	-	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed	-	400	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	230	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$V_{GSM}$	peak gate-source voltage	pulsed; $t_p \leq 50\text{ }\mu\text{s}$	-15	15	V
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	75	A
$I_{SM}$	peak source current	pulsed; $T_{mb} = 25\text{ °C}$	-	240	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}; V_{sup} \leq 25\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 5\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped	-	500	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

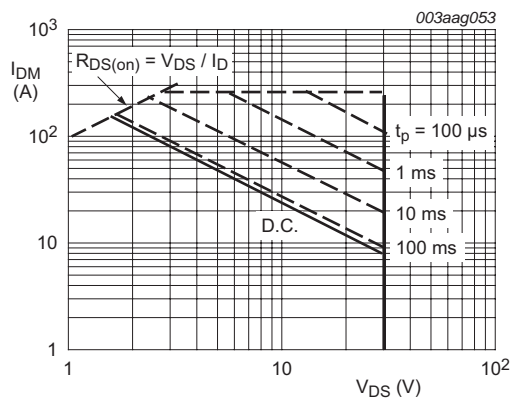
**Fig 1. Normalized total power dissipation as a function of mounting base temperature**



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

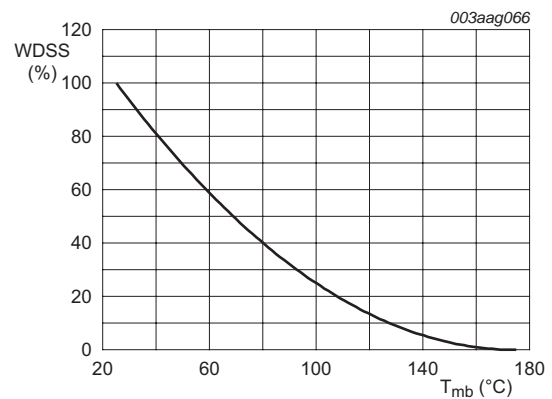
$V_{GS} \geq 5\text{ V}$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature**



$T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $I_{DM}$  is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**



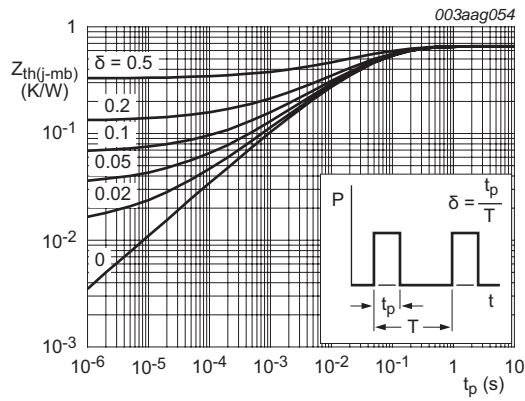
$I_D = 75\text{ A}$

**Fig 4. Normalised drain-source non-repetitive avalanche energy as a function of mounting-base temperature**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.65	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint ; FR4 board	-	50	-	K/W

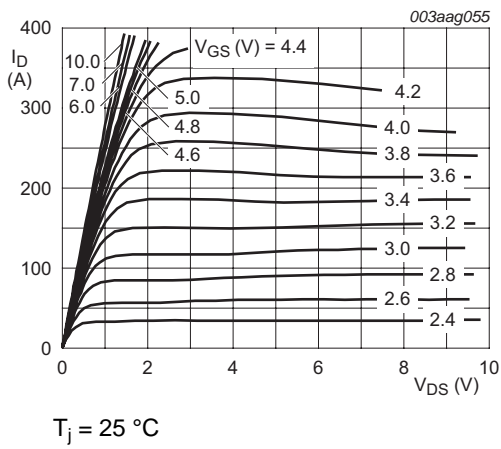


**Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

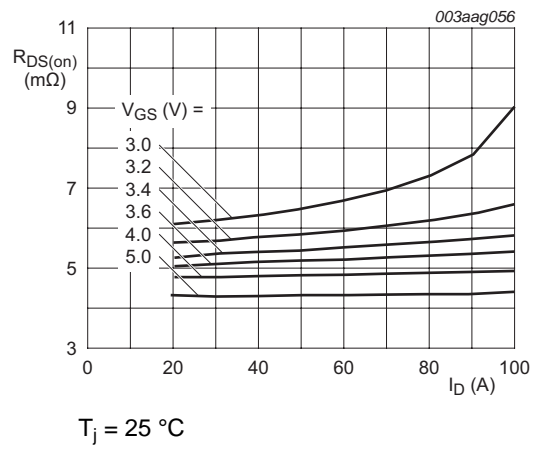
## 6. Characteristics

Table 6. Characteristics

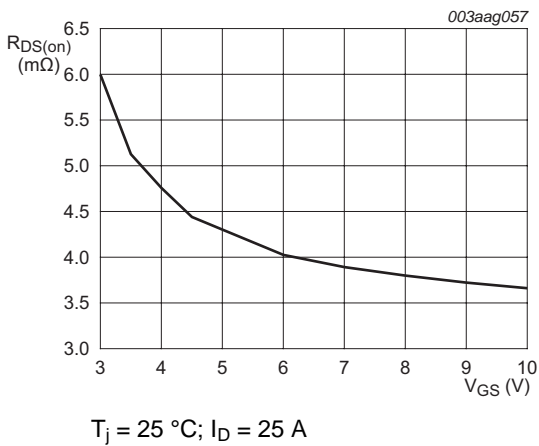
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	2.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	4.3	5	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	3.9	4.6	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	-	5.4	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	-	9.3	m $\Omega$
<b>Dynamic characteristics</b>						
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	6500	8600	pF
$C_{oss}$	output capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = nk \text{ }^\circ\text{C}$	-	1500	1800	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	1000	1350	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	45	65	ns
$t_r$	rise time		-	220	330	ns
$t_{d(off)}$	turn-off delay time		-	435	600	ns
$t_f$	fall time		-	320	450	ns
$L_D$	internal drain inductance	measured from upper edge of drain tab to centre of die ; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
$L_S$	internal source inductance	from source lead soldering point to source bond pad ; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.85	1.2	V
		$I_S = 75 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	1.1	-	V
$t_{rr}$	reverse recovery time	$I_S = 75 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	400	-	ns
$Q_r$	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	1	-	$\mu\text{C}$



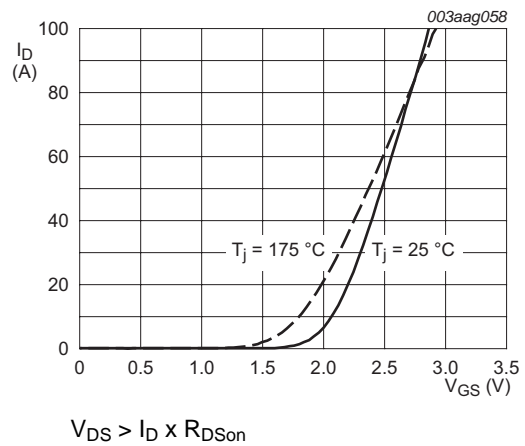
**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



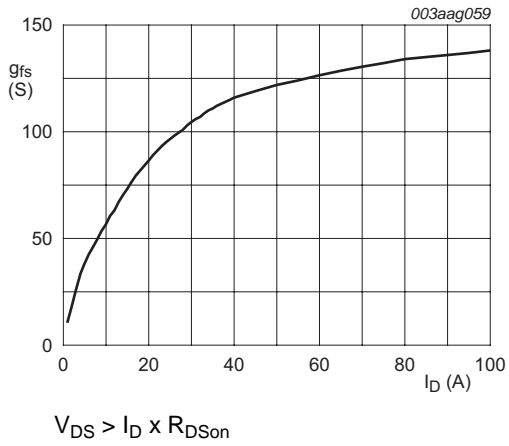
**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**



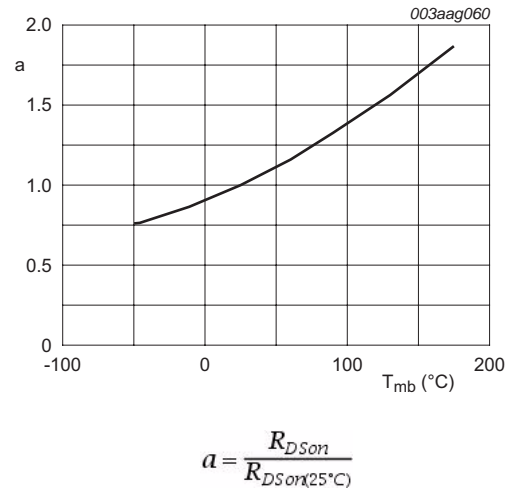
**Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**



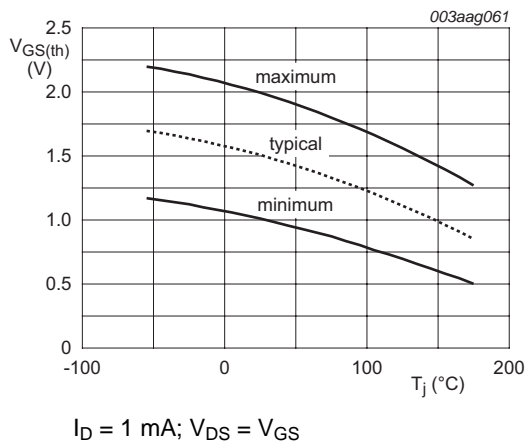
**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



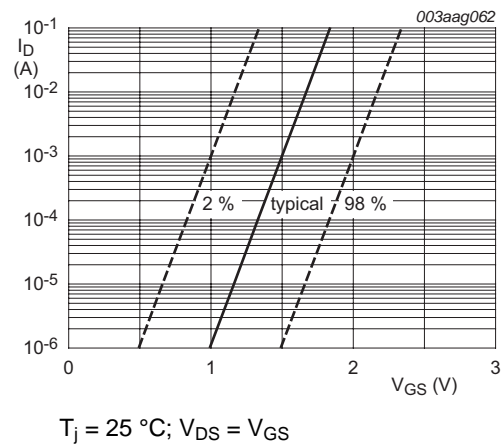
**Fig 10. Forward transconductance as a function of drain current; typical values**



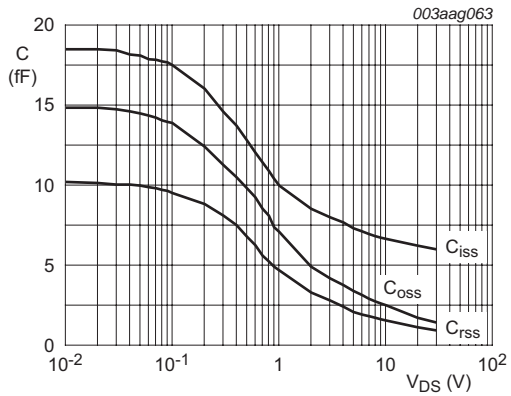
**Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature**



**Fig 12. Gate-source threshold voltage as a function of junction temperature**

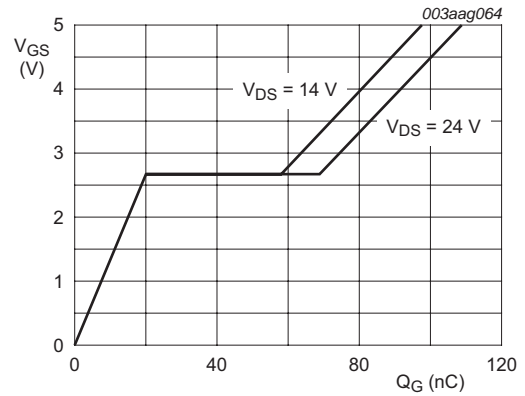


**Fig 13. Sub-threshold drain current as a function of gate-source voltage**



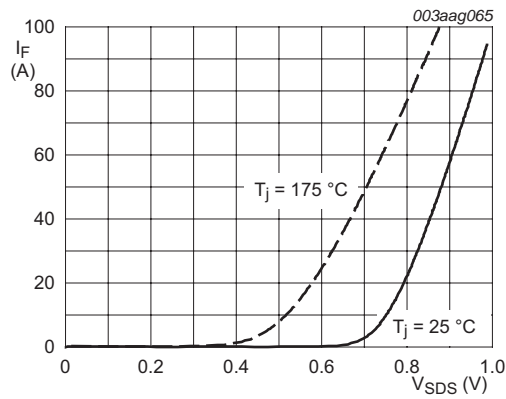
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$T_j = 25\text{ }^\circ\text{C}; I_D = 50\text{ A}$

**Fig 15. Gate-source voltage as a function of gate charge; typical values**



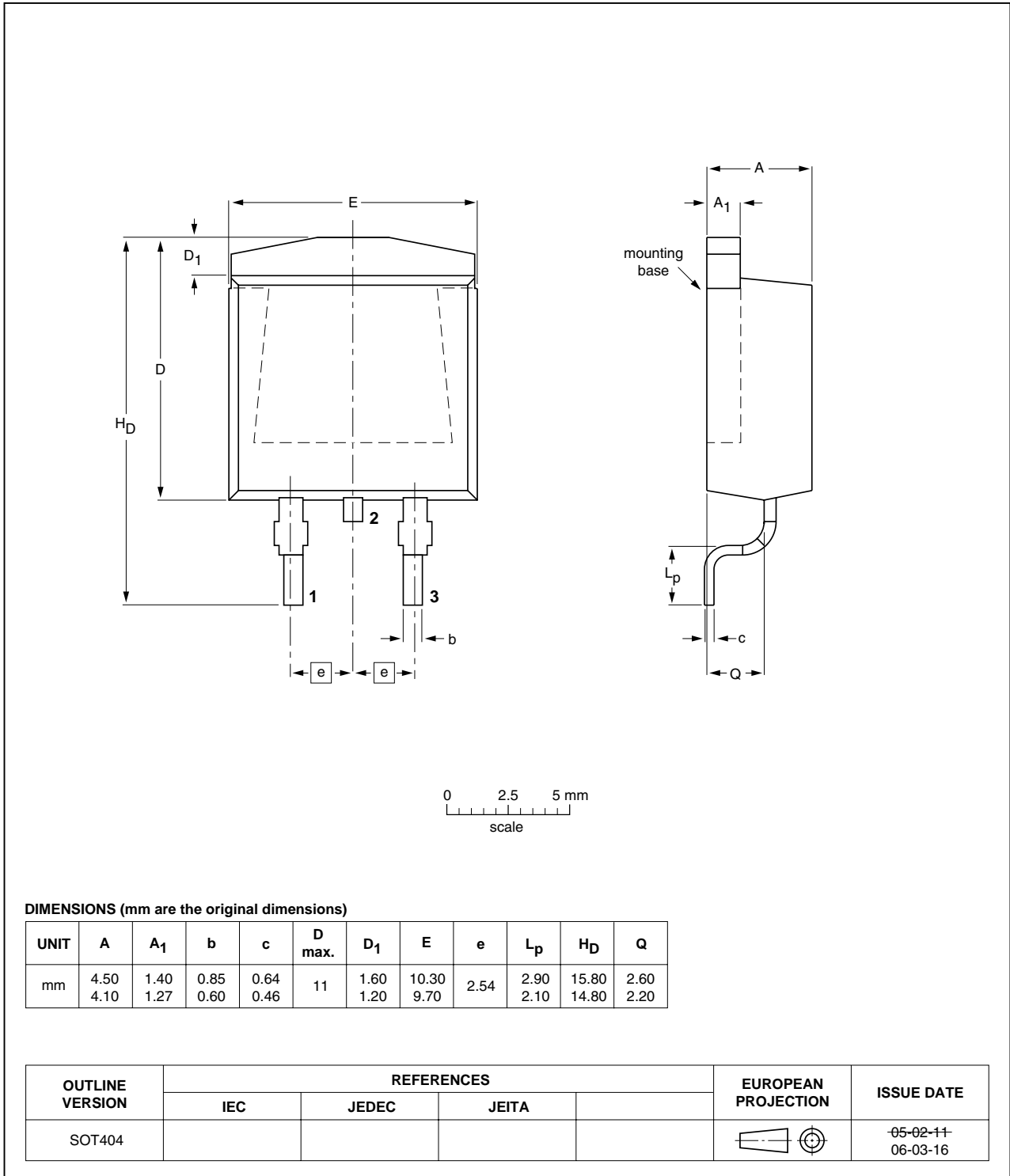
$V_{GS} = 0\text{ V}$

**Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

**SOT404**



**Fig 17. Package outline SOT404 (D2PAK)**

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9605-30A v.3	20110419	Product data sheet	-	BUK9605-30A v.2
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>			
BUK9605-30A v.2	19990801	Product specification	-	BUK9605-30A v.1

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### 9.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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