

DATA SHEET

PDTA144W series

PNP resistor-equipped transistors;

R1 = 47 k Ω , R2 = 22 k Ω

Product data sheet
Supersedes data of 2004 Mar 23

2004 Aug 05

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FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	–50	V
I _O	output current (DC)	–	–100	mA
R1	bias resistor	47	–	k Ω
R2	bias resistor	22	–	k Ω

DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA144WE	SOT416	SC-75	5D	PDTC144WE
PDTA144WEF	SOT490	SC-89	2E	PDTC144WEF
PDTA144WK	SOT346	SC-59	46	PDTC144WK
PDTA144WM	SOT883	SC-101	F8	PDTC144WM
PDTA144WS	SOT54 (TO-92)	SC-43	TA144W	PDTC144WS
PDTA144WT	SOT23	–	*43 ⁽¹⁾	PDTC144WT
PDTA144WU	SOT323	SC-70	*28 ⁽¹⁾	PDTC144WU

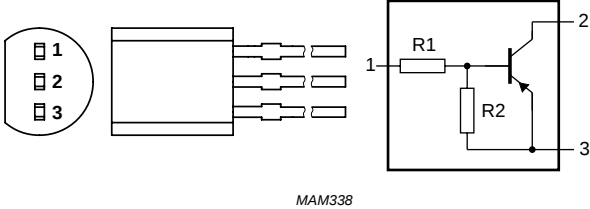
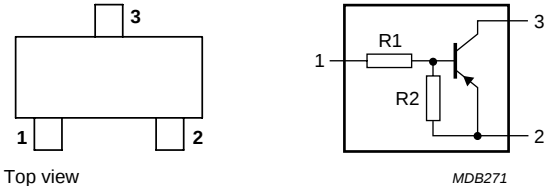
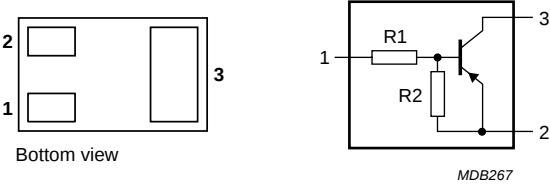
Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA144WS		1 2 3	base collector emitter
PDTA144WE PDTA144WEF PDTA144WK PDTA144WT PDTA144WU		1 2 3	base emitter collector
PDTA144WM		1 2 3	base emitter collector

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTA144WE	–	plastic surface mounted package; 3 leads	SOT416
PDTA144WEF	–	plastic surface mounted package; 3 leads	SOT490
PDTA144WK	–	plastic surface mounted package; 3 leads	SOT346
PDTA144WM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm	SOT883
PDTA144WS	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA144WT	–	plastic surface mounted package; 3 leads	SOT23
PDTA144WU	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	–50	V
V _{CEO}	collector-emitter voltage	open base	–	–50	V
V _{EBO}	emitter-base voltage	open collector	–	–10	V
V _I	input voltage				
	positive		–	+10	V
	negative		–	–40	V
I _O	output current (DC)		–	–100	mA
I _{CM}	peak collector current		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C;			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	T _{amb} ≤ 25 °C		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	830	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

Note

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions.; FR4 with 60 μ m copper strip line.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = -50 V; I _E = 0 A	–	–	-100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = -30 V; I _B = 0 A	–	–	-1	μ A
		V _{CE} = -30 V; I _B = 0 A; T _j = 150 °C	–	–	-50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A	–	–	-110	μ A
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -5 mA	60	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = -10 mA; I _B = -0.5 mA	–	–	-150	mV
V _{i(off)}	input-off voltage	I _C = -100 μ A; V _{CE} = -5 V	–	-1.7	-1.2	V
V _{i(on)}	input-on voltage	I _C = -2 mA; V _{CE} = -0.3 V	-4	-2.7	–	V
R1	input resistor		33	47	61	k Ω
$\frac{R2}{R1}$	resistor ratio		0.37	0.47	0.57	
C _c	collector capacitance	I _E = I _e = 0 A; V _{CB} = -10 V; f = 1 MHz	–	–	3	pF

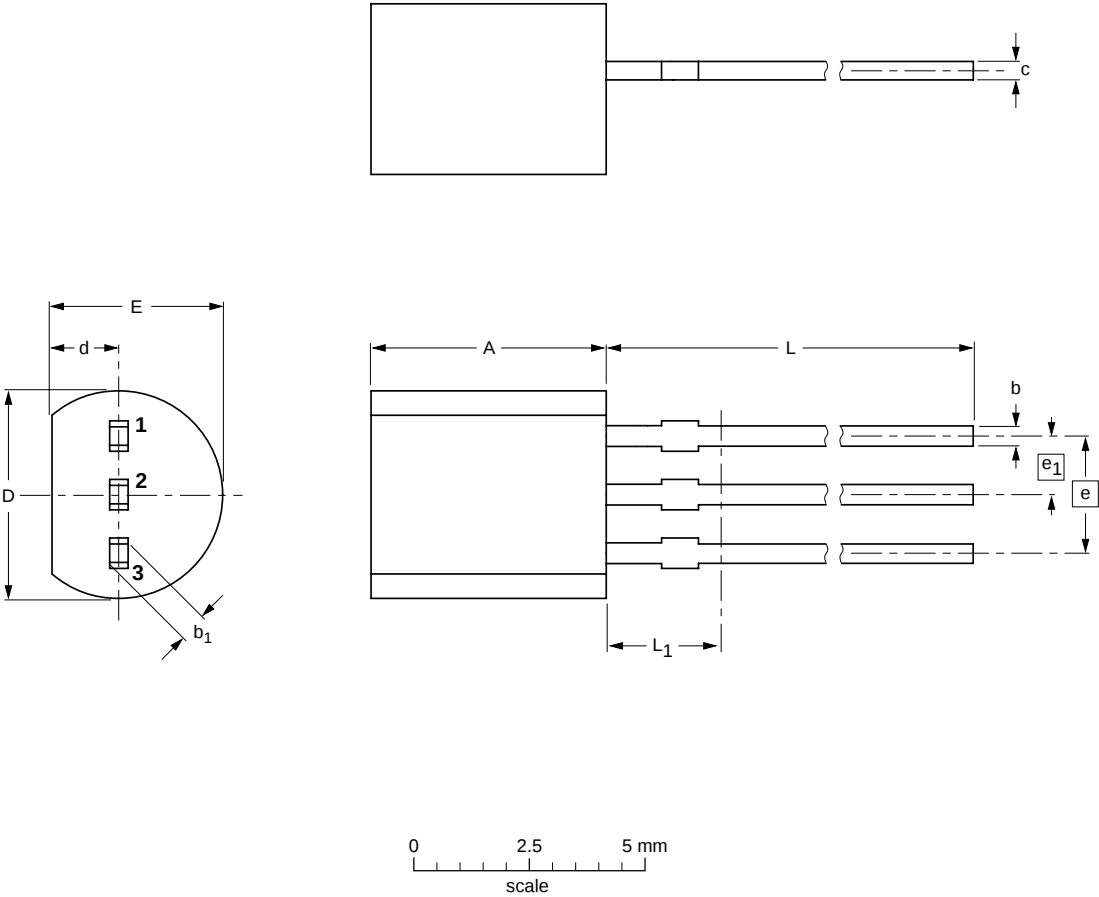
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PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

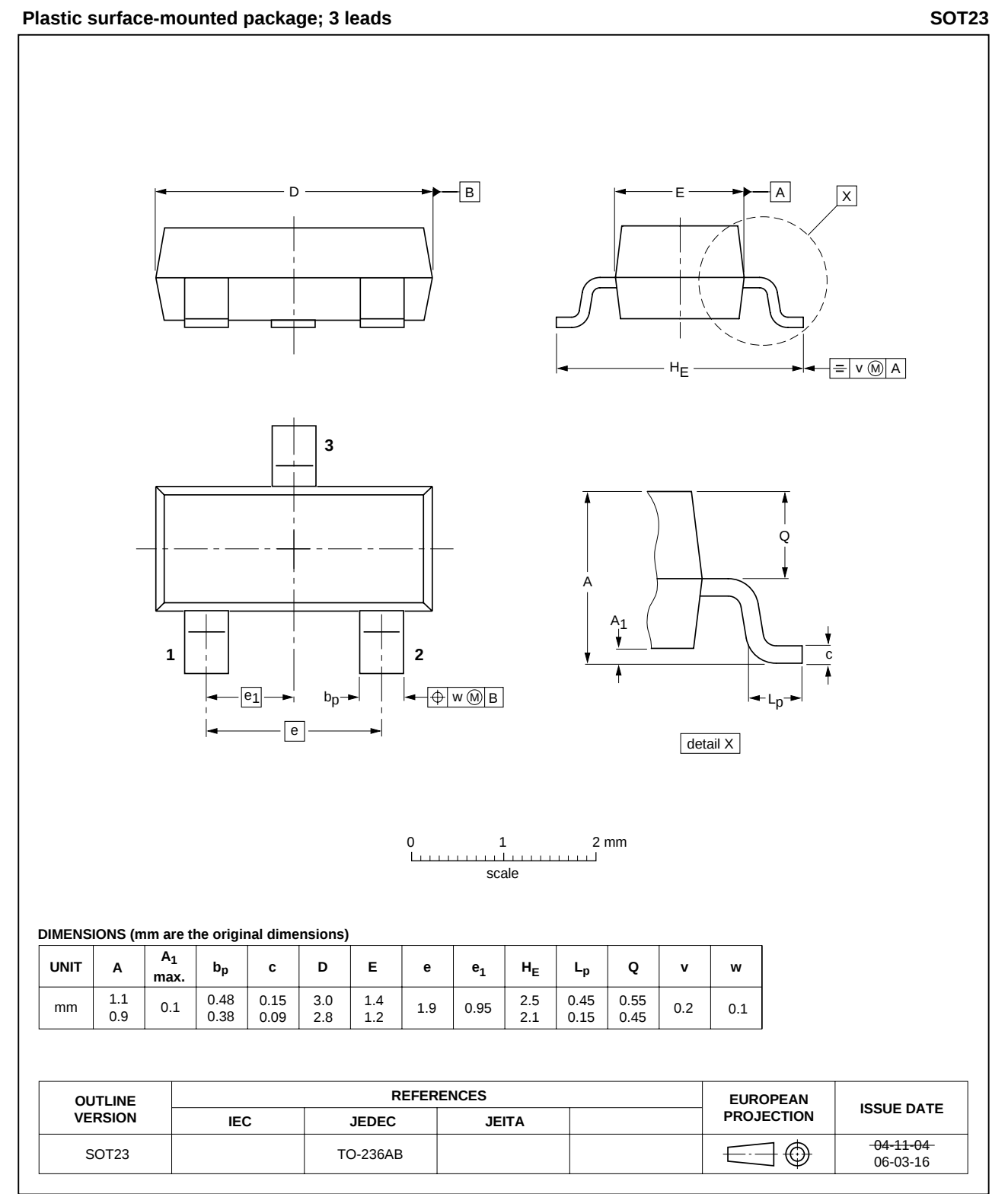
Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			04-06-28 04-11-16

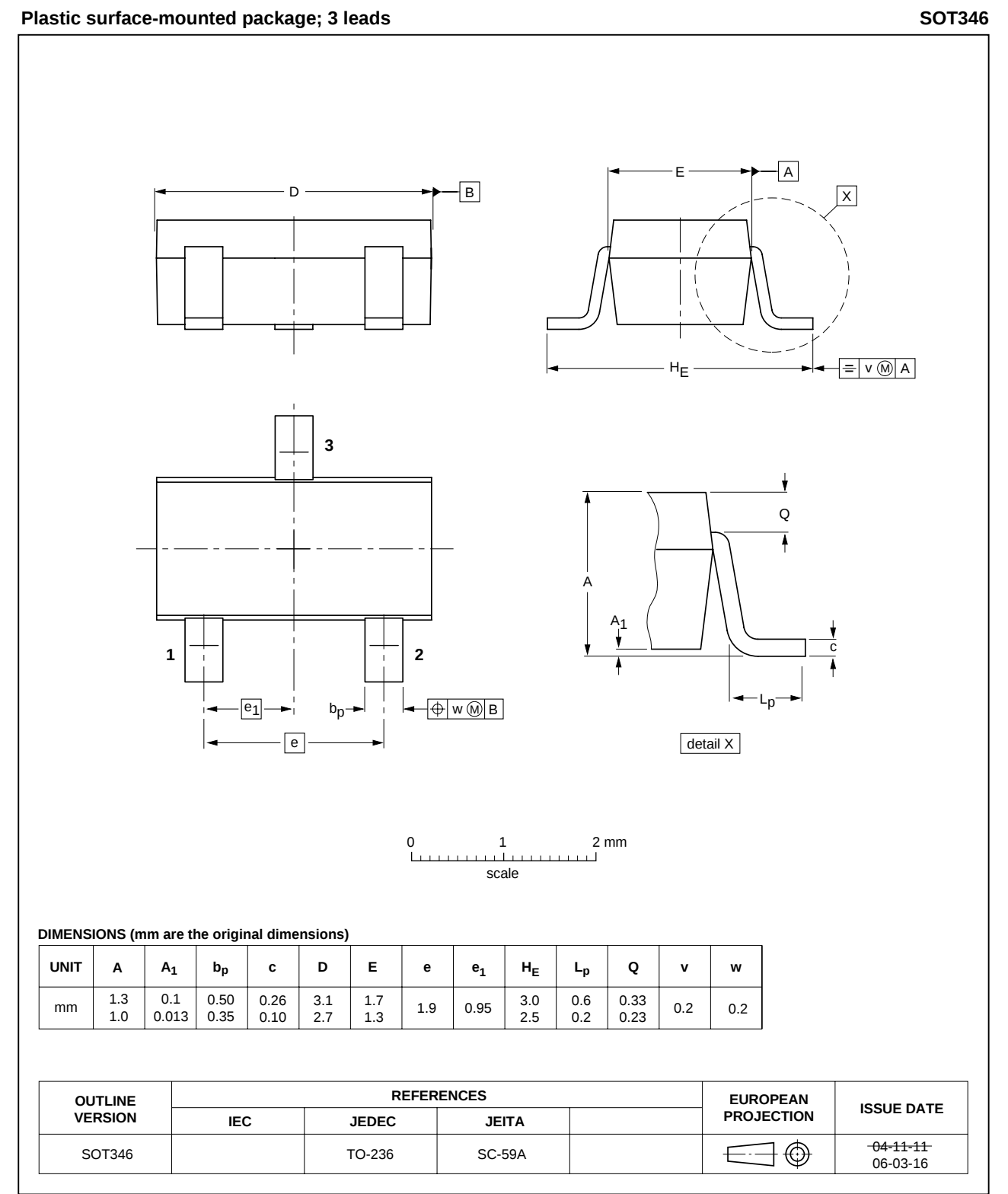
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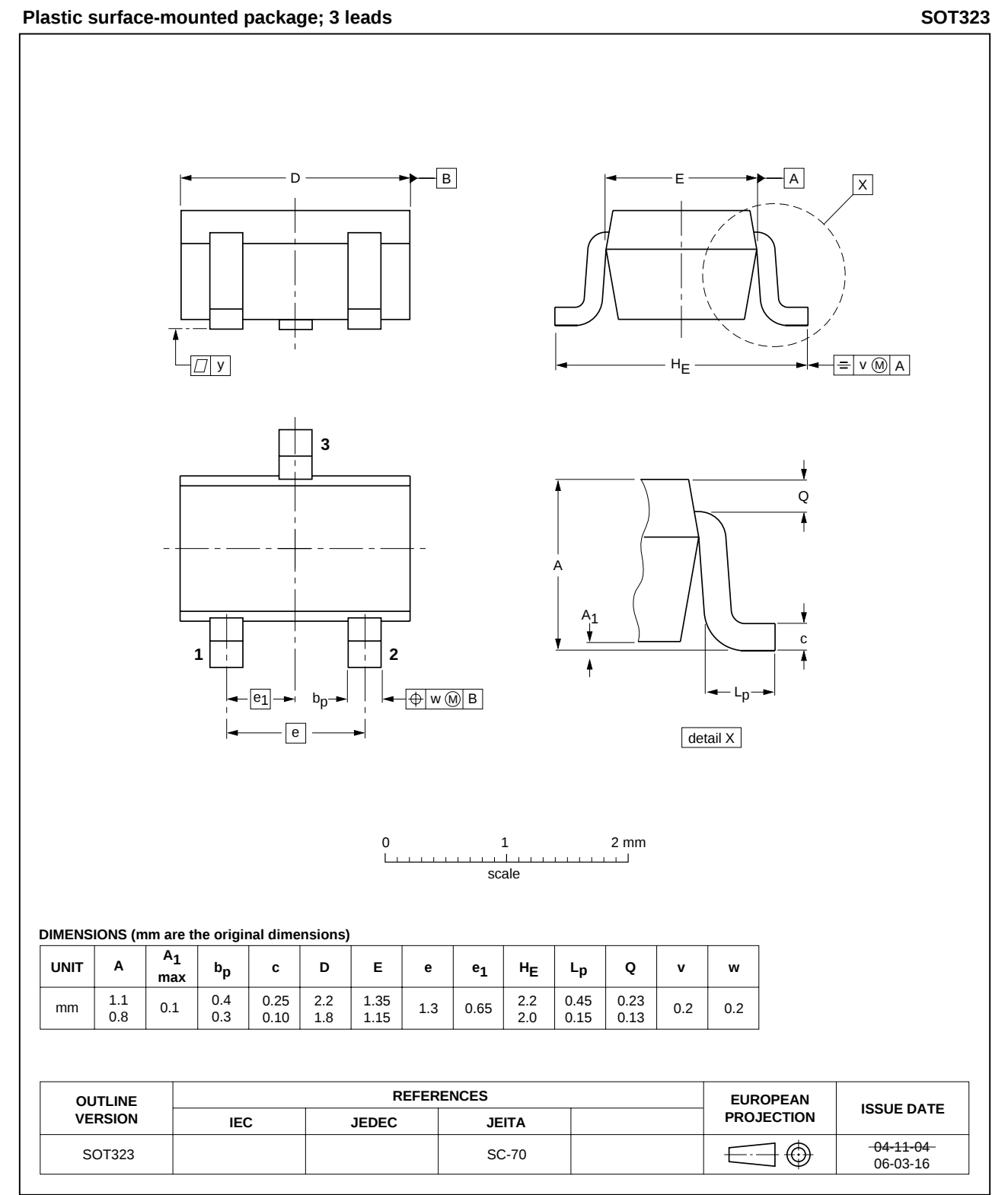
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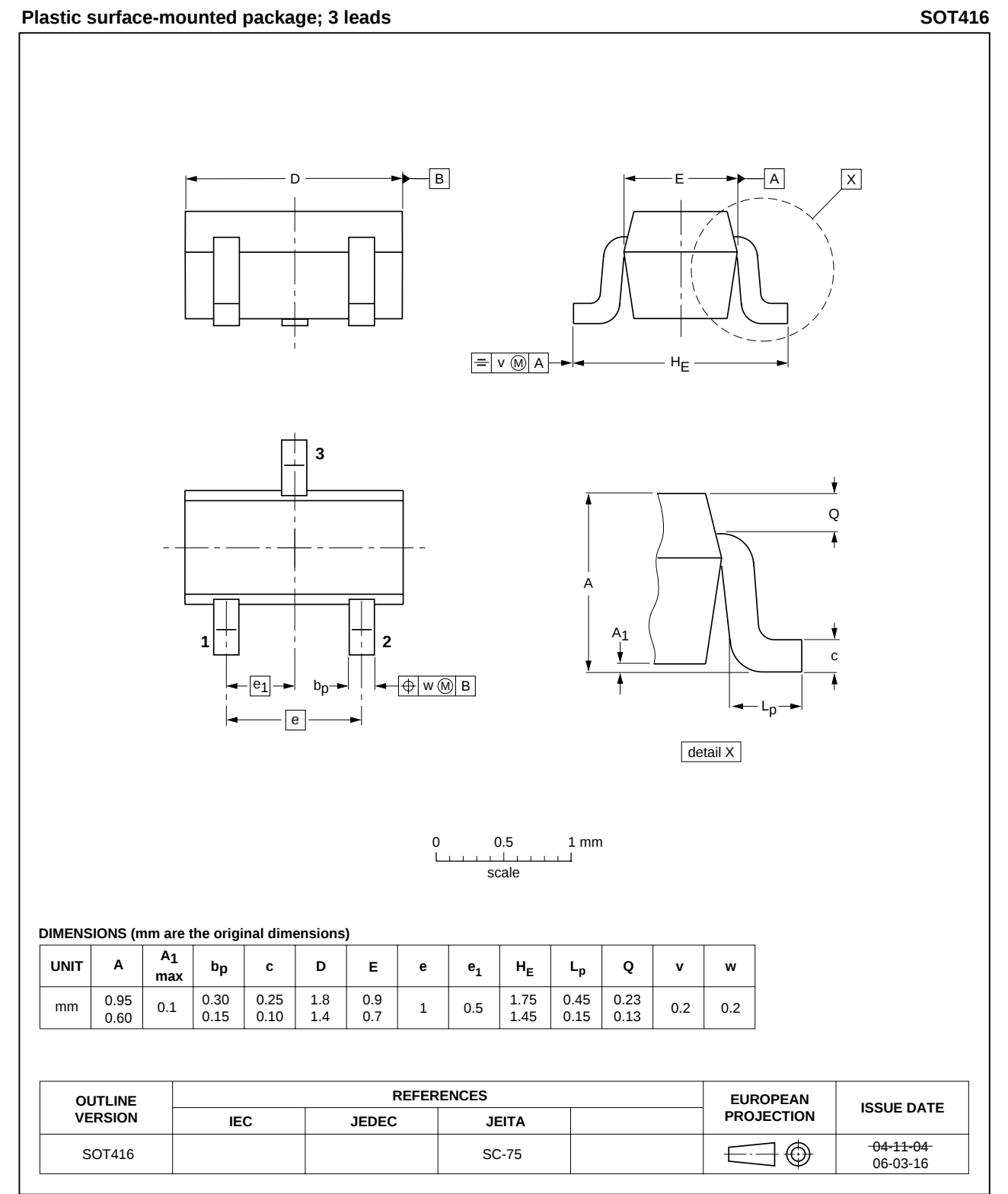
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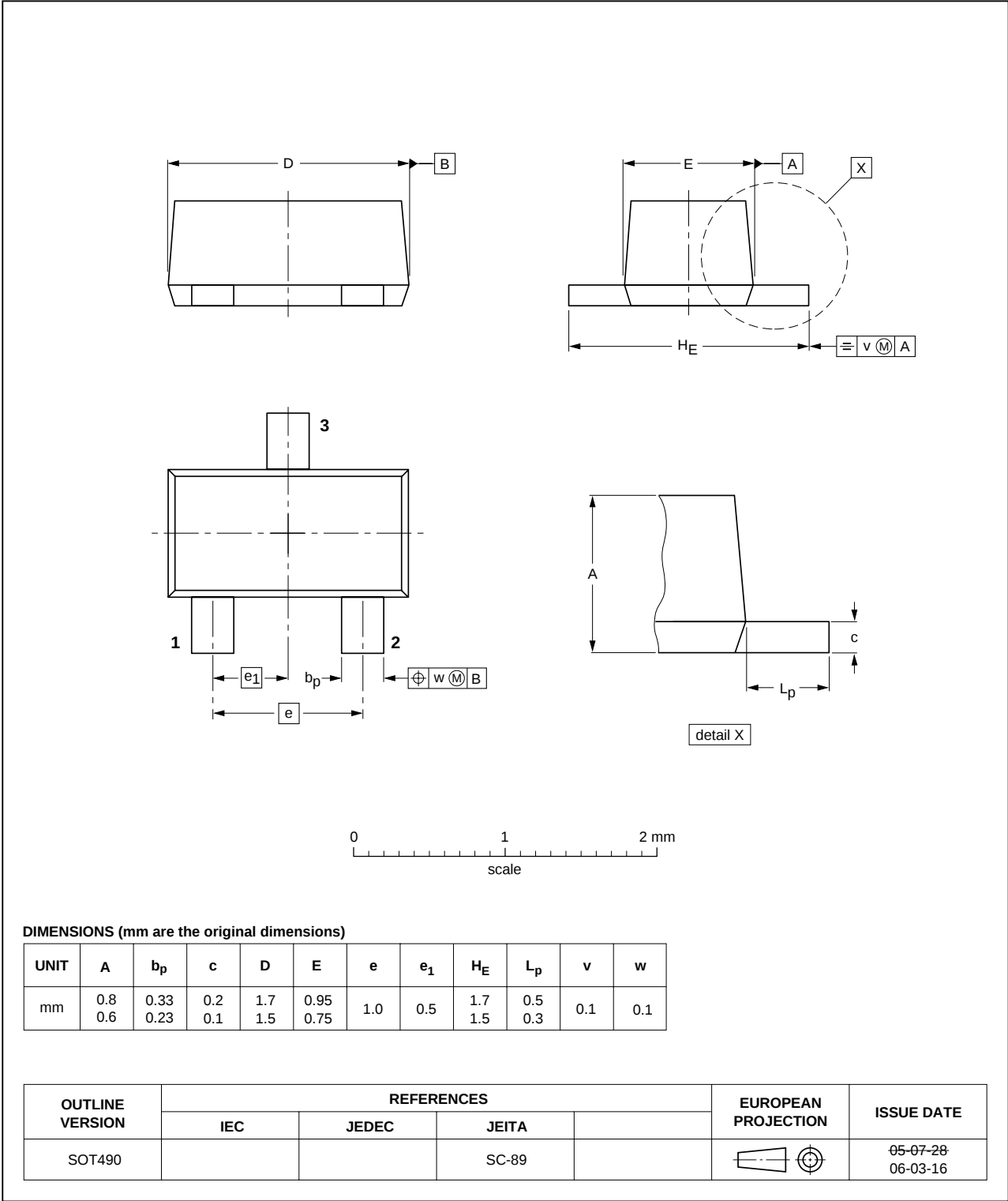


PNP resistor-equipped transistors;
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Plastic surface-mounted package; 3 leads

SOT490

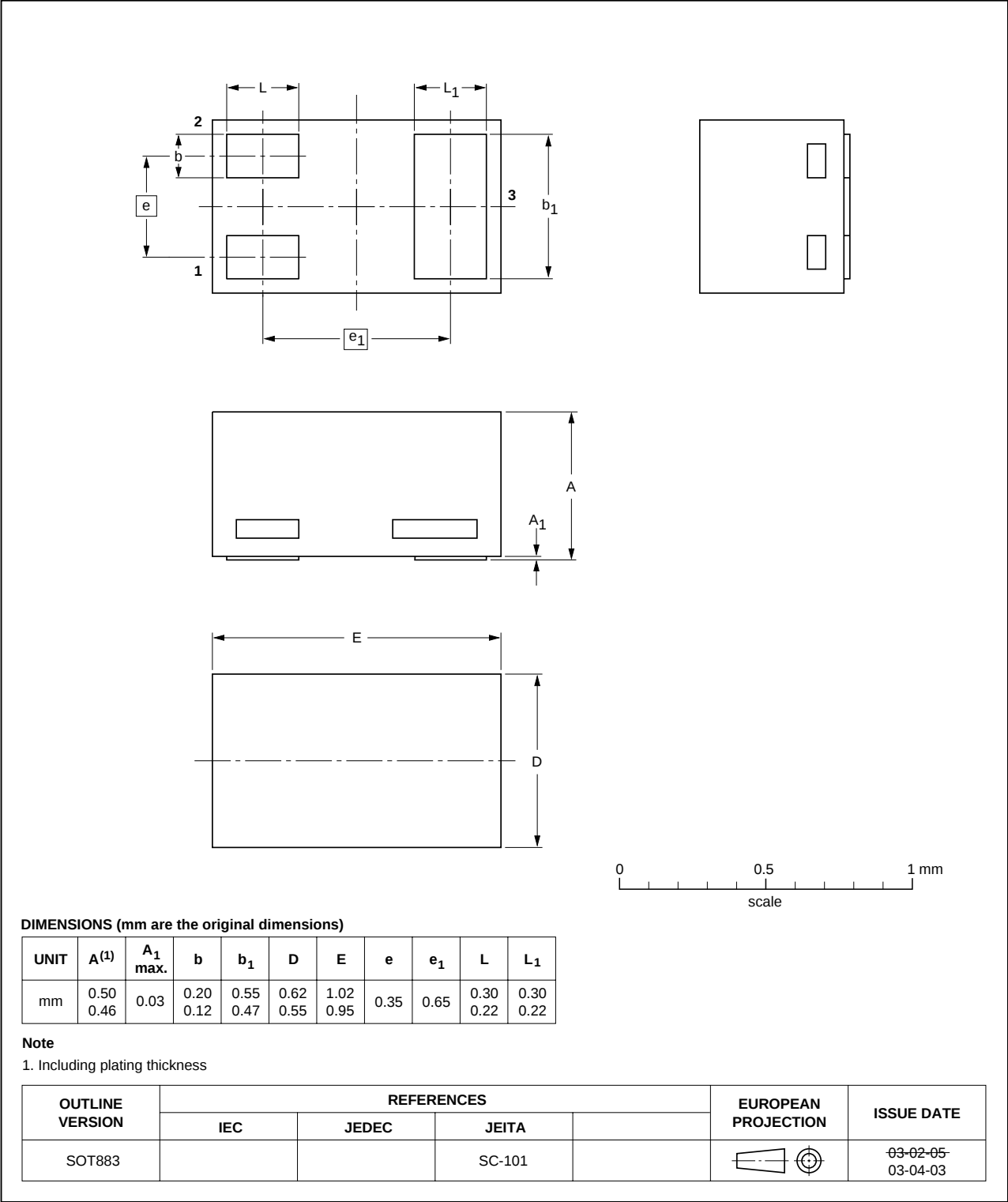


PNP resistor-equipped transistors;
R1 = 47 kΩ, R2 = 22 kΩ

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Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

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NXP Semiconductors

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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