

MOS FIELD EFFECT TRANSISTOR

μ PA1731

SWITCHING

P-CHANNEL POWER MOS FET

INDUSTRIAL USE

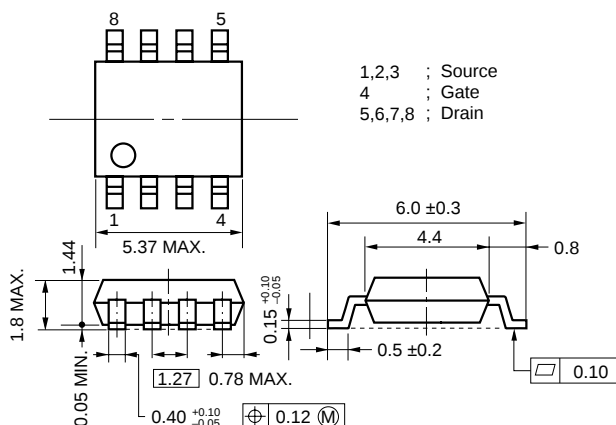
DESCRIPTION

The μ PA1731 is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

FEATURES

- Low on-resistance
 $R_{DS(on)1} = 10.3 \text{ m}\Omega$ TYP. ($V_{GS} = -10 \text{ V}$, $I_D = -5.0 \text{ A}$)
 $R_{DS(on)2} = 14.6 \text{ m}\Omega$ TYP. ($V_{GS} = -4.5 \text{ V}$, $I_D = -5.0 \text{ A}$)
 $R_{DS(on)3} = 16.5 \text{ m}\Omega$ TYP. ($V_{GS} = -4.0 \text{ V}$, $I_D = -5.0 \text{ A}$)
- ★ • Low C_{iss} : $C_{iss} = 2600 \text{ pF}$ TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1731G	Power SOP8

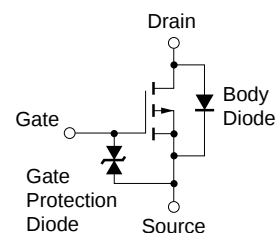
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 10	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 40	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$

2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$

EQUIVALENT CIRCUIT



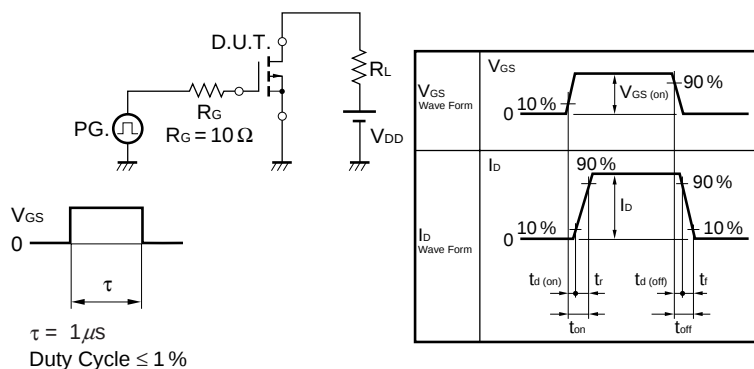
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

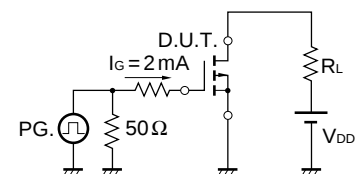
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = -10 V, I _D = -5.0 A		10.3	13.0	mΩ
	R _{DS(on)2}	V _{GS} = -4.5 V, I _D = -5.0 A		14.6	19.5	mΩ
	R _{DS(on)3}	V _{GS} = -4.0 V, I _D = -5.0 A		16.5	22.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = -10 V, I _D = -5.0 A	8.0	18.0		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			-1	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ± 20 V, V _{DS} = 0 V			± 10	μA
Input Capacitance	C _{iss}	V _{DS} = -10 V		2600		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		810		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		350		pF
Turn-on Delay Time	t _{d(on)}	I _D = -5.0 A		32		ns
Rise Time	t _r	V _{GS(on)} = -10 V		185		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = -15 V		155		ns
Fall Time	t _f	R _G = 10 Ω		110		ns
Total Gate Charge	Q _G	I _D = -10 A		46		nC
Gate to Source Charge	Q _{GS}	V _{DD} = -24 V		6.5		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = -10 V		12		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 10 A, V _{GS} = 0 V		0.80		V
Reverse Recovery Time	t _{rr}	I _F = 10 A, V _{GS} = 0 V		50		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		46		nC

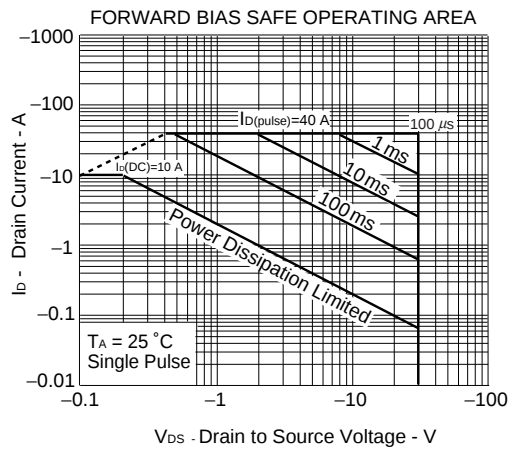
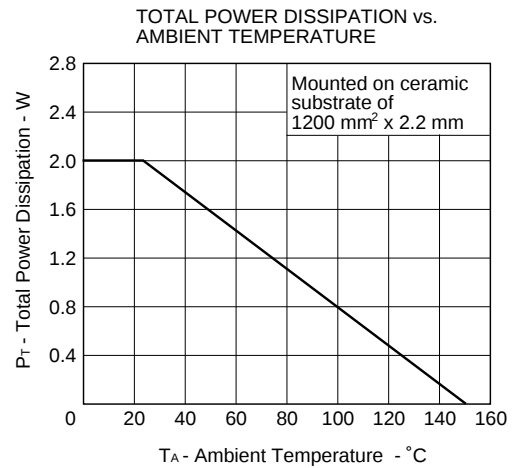
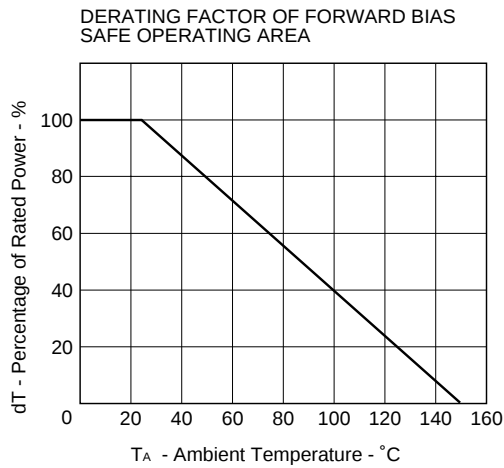
TEST CIRCUIT 1 SWITCHING TIME



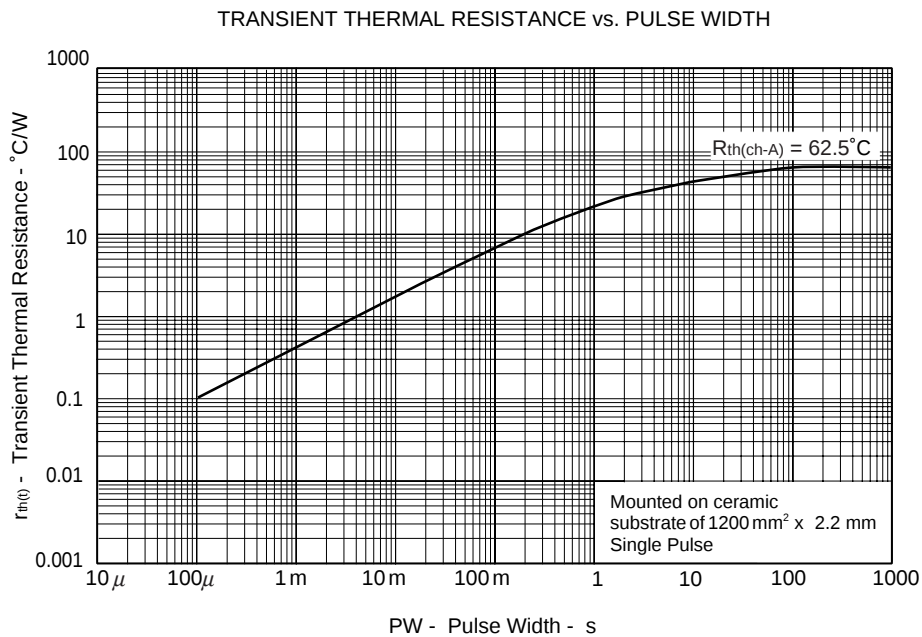
TEST CIRCUIT 2 GATE CHARGE

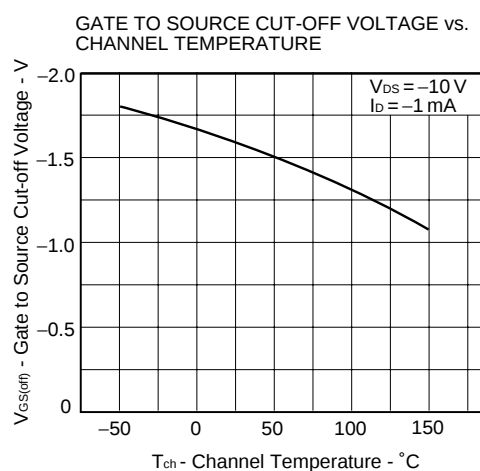
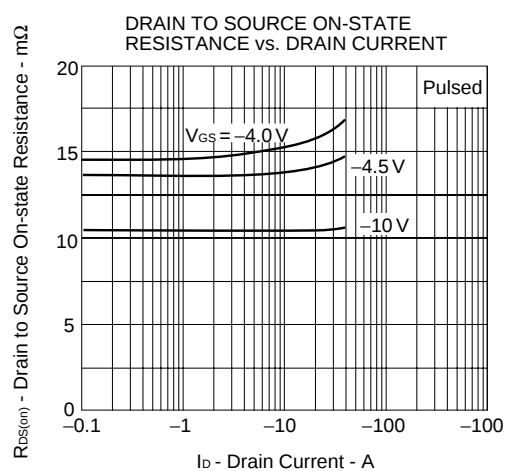
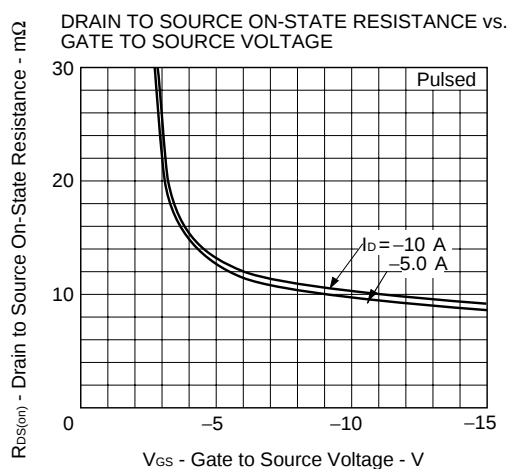
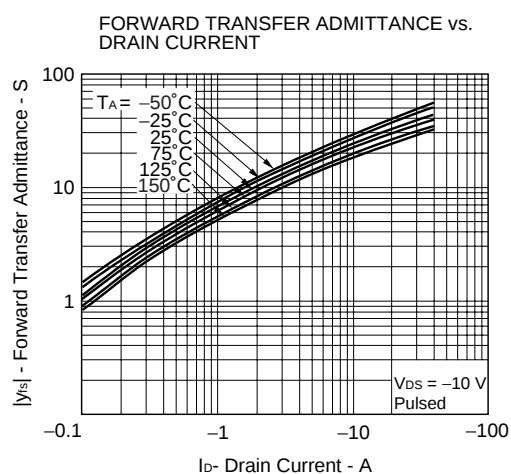
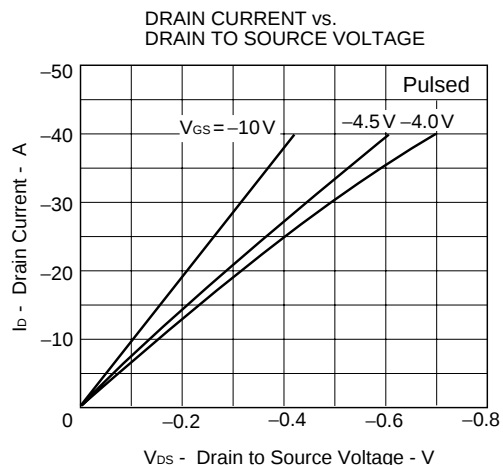
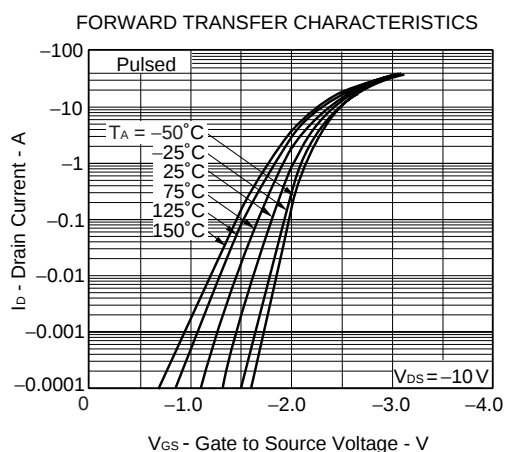


★ TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

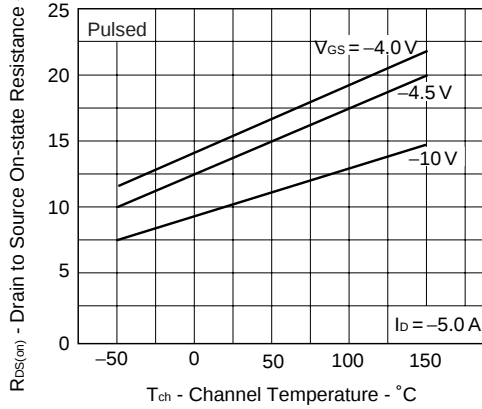


Remark Mounted on ceramic substrate of $1200\text{ mm}^2 \times 2.2\text{ mm}$

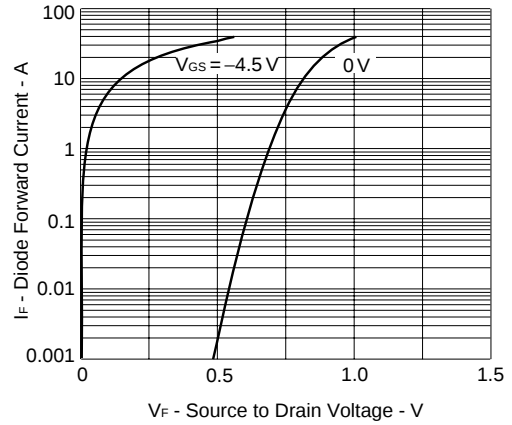




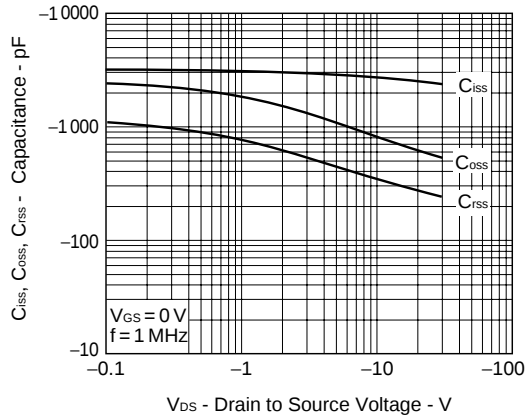
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



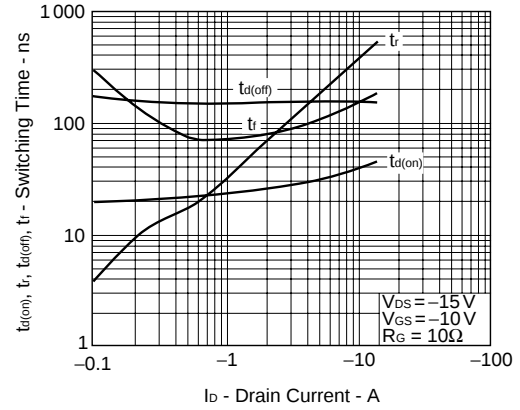
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



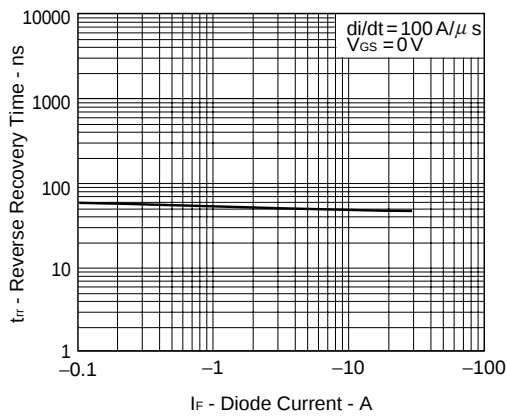
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



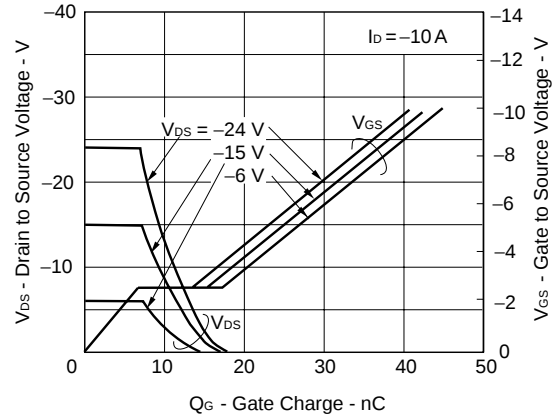
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



[MEMO]

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