

SWITCHING  
DUAL P-CHANNEL POWER MOS FET  
INDUSTRIAL USE

DESCRIPTION

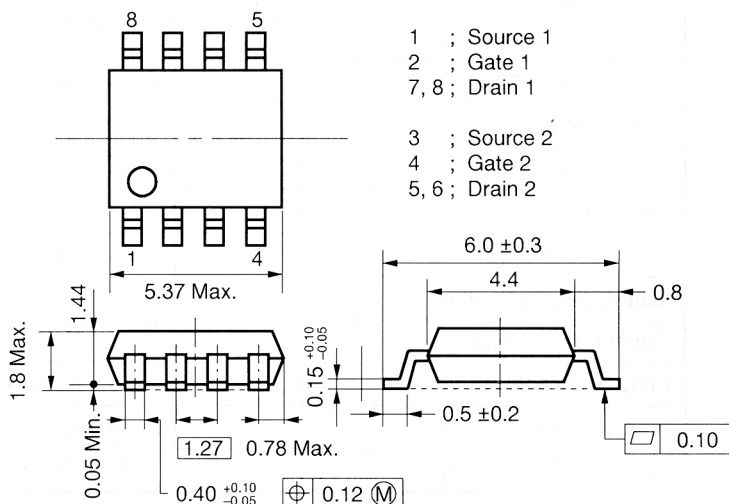
This product is Dual P-Channel MOS Field Effect Transistor designed for power management switch applications of notebook computers and cellur phones.

FEATURES

- Dual MOSFET chips in small package
- 4 V Gate Drive Type and Low On-Resistance  
 $R_{DS(on)1} = 0.09 \Omega$  Max. ( $V_{GS} = -10 V, I_D = -1.8 A$ )  
 $R_{DS(on)2} = 0.18 \Omega$  Max. ( $V_{GS} = -4 V, I_D = -1.8 A$ )
- Low  $C_{iss}$   $C_{iss} = 540 pF$  Typ.
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

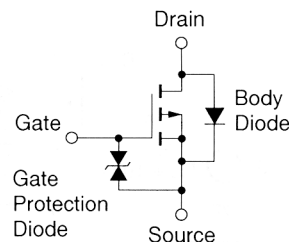
PACKAGE DIMENSIONS

(in millimeter)



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ , all terminals are connected.)

Drain to Source Voltage	$V_{DSS}$	-20	V
Gate to Source Voltage	$V_{GSS}$	±20	V
Drain Current (DC)	$I_{D(DC)}$	±3.5	A
Drain Current (pulse)*	$I_{D(pulse)}$	±14	A
Total Power Dissipation (1 unit)**	$P_T$	1.7	W
Total Power Dissipation (2 unit)**	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C



\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1 \%$

\*\*  $T_A = 25^\circ C$ , Mounted on ceramic substrate of  $2\ 000\ mm^2 \times 1.1\ mm$

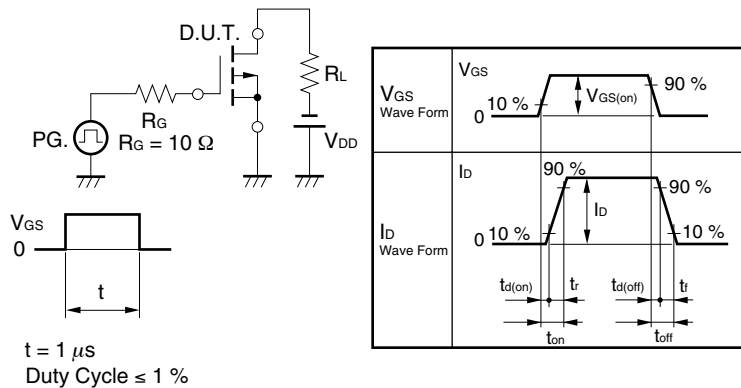
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

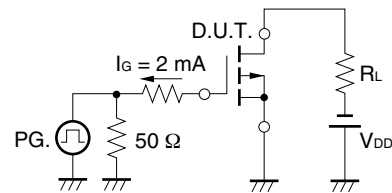
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, all terminals are connected.)**

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.8 A		0.065	0.090	Ω
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4 V, I <sub>D</sub> = -1.8 A		0.125	0.180	Ω
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0	-1.7	-2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.8 A	2.0	4.4		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0			-10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V		540		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0		385		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		105		pF
Turn-On Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = -1.8 A		10		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = -10 V		110		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = -10 V		340		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		230		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = -3.5 A		18		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = -16 V		2.0		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = -10 V		5.1		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 3.5 A, V <sub>GS</sub> = 0		0.8		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 3.5 A, V <sub>GS</sub> = 0		160		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		310		nC

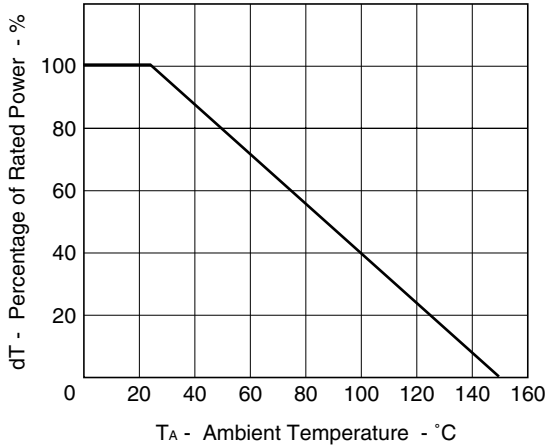
**Test Circuit 1 Switching Time**



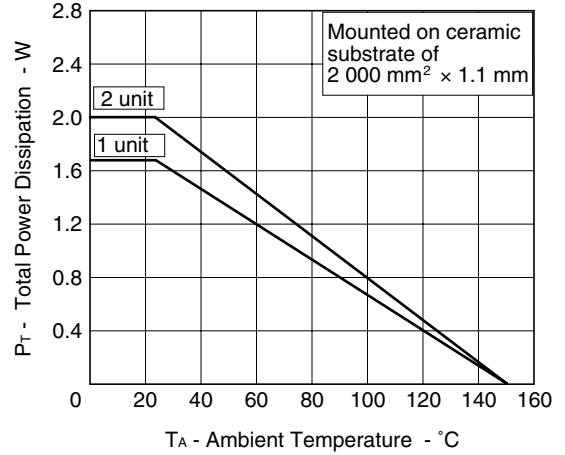
**Test Circuit 2 Gate Charge**



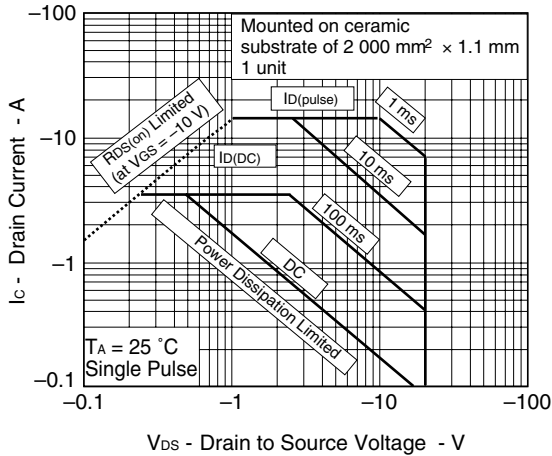
DERATING FACTOR OF FORWARD BIAS  
SAFE OPERATING AREA



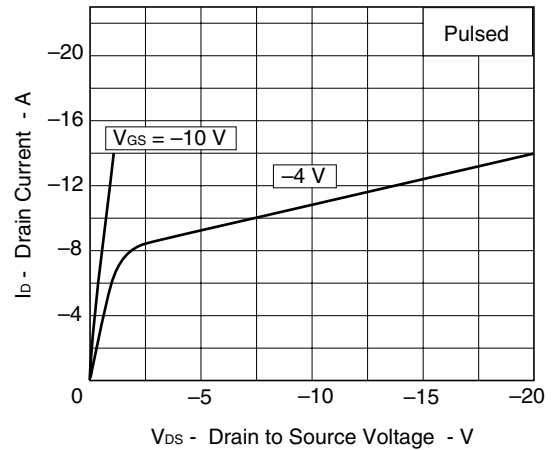
TOTAL POWER DISSIPATION vs.  
AMBIENT TEMPERATURE



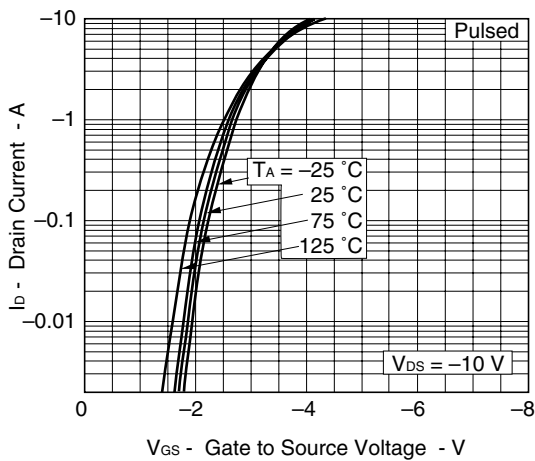
FORWARD BIAS SAFE OPERATING AREA



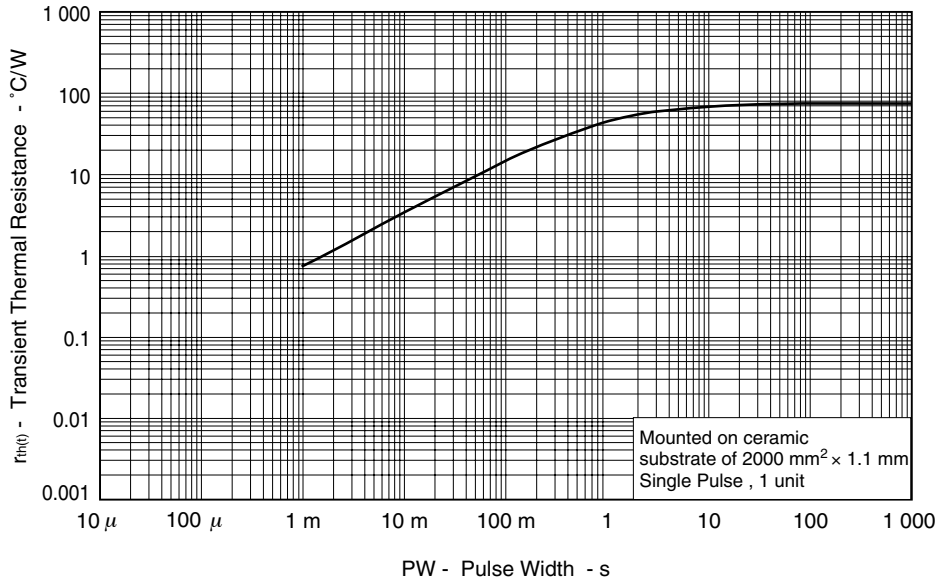
DRAIN CURRENT vs.  
DRAIN TO SOURCE VOLTAGE



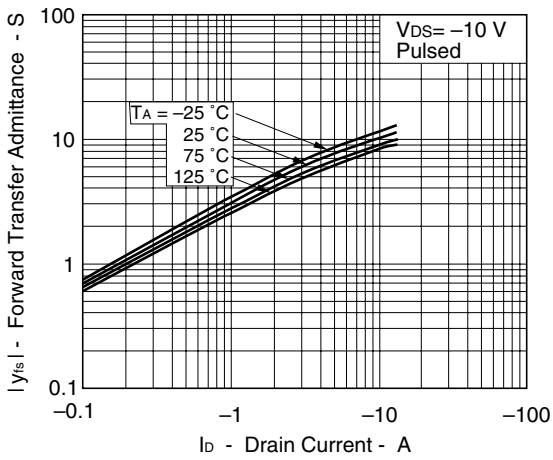
FORWARD TRANSFER CHARACTERISTICS



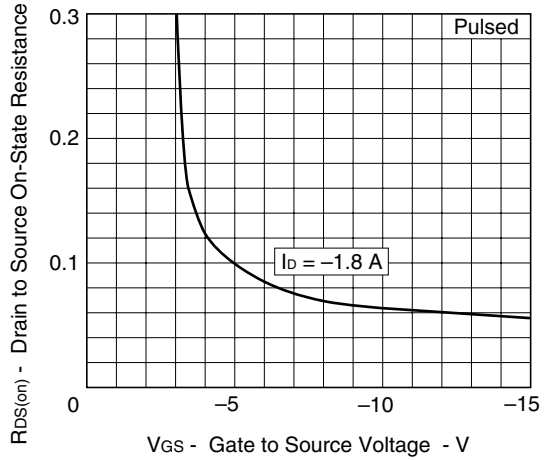
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



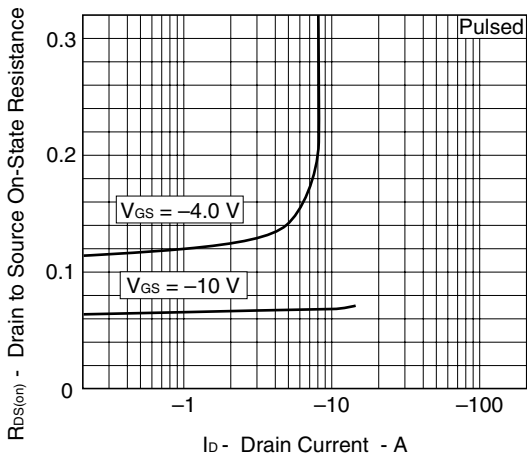
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



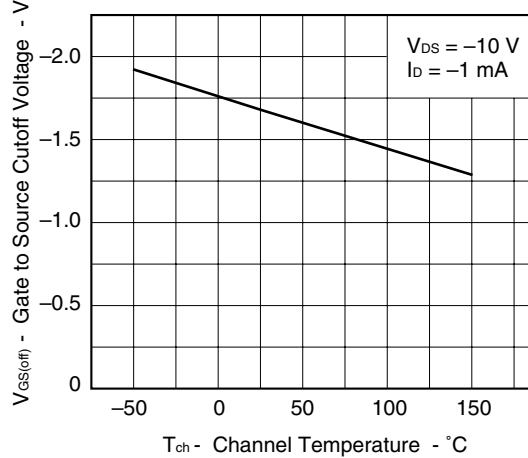
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

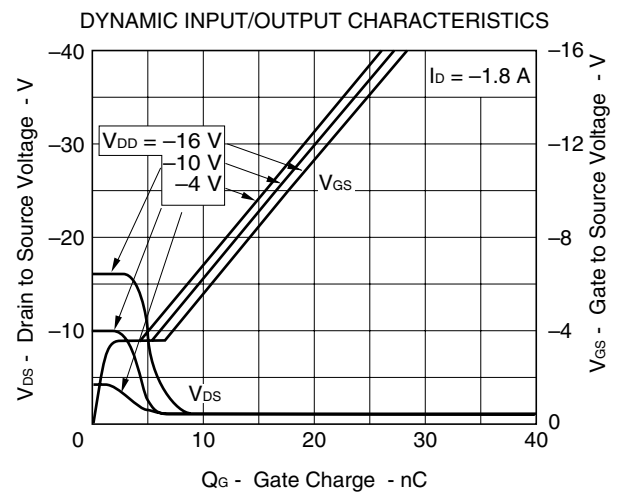
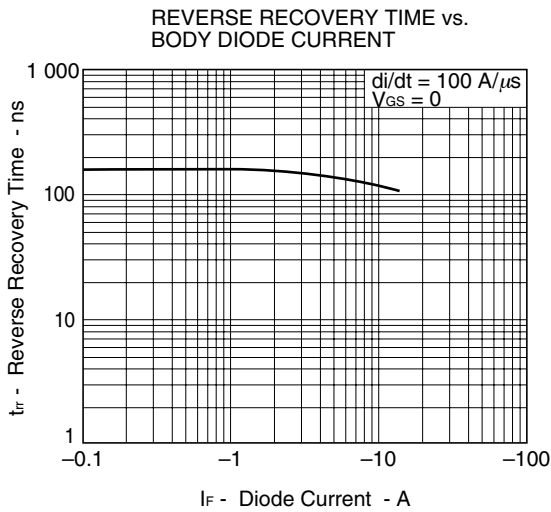
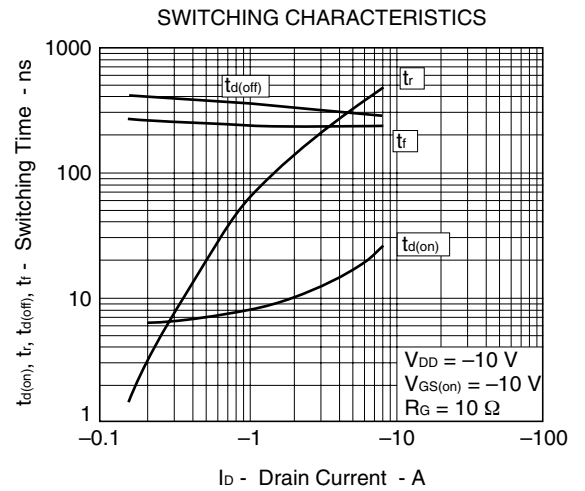
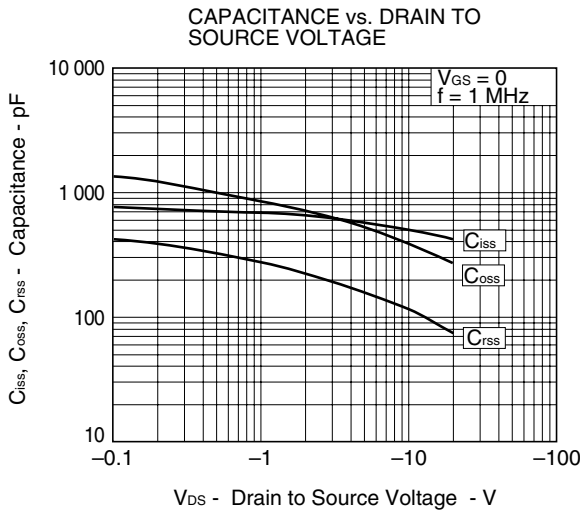
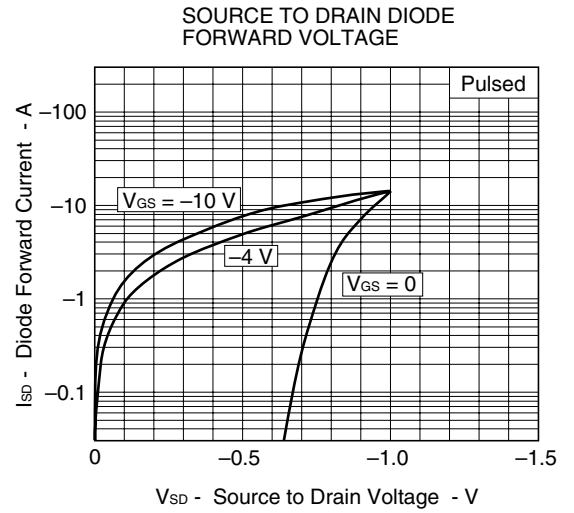
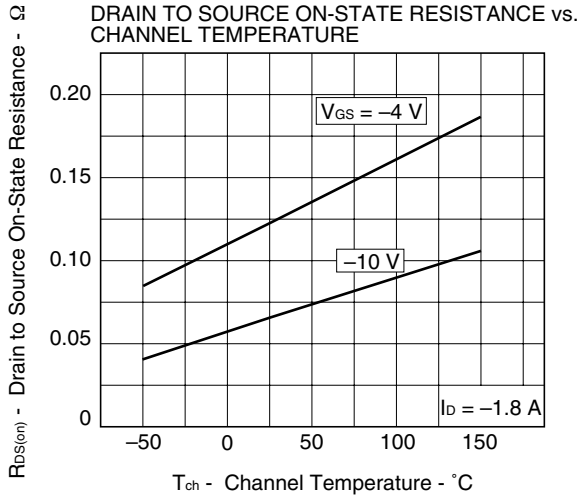


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





## REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.