DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR

μPA1756

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

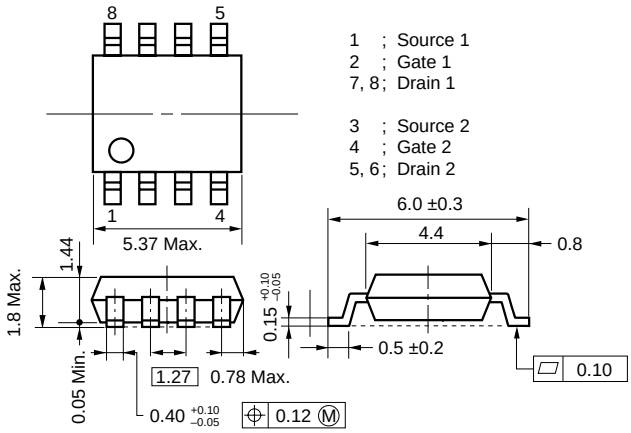
FEATURES

- Dual MOS FET chips in small package
- 2.5-V gate drive type and low on-resistance
  $R_{DS(on)1}$ = 30 mΩ MAX. (V_{GS} = 4.5 V, I_D = 3.0 A)
  $R_{DS(on)2}$ = 40 mΩ MAX. (V_{GS} = 2.5 V, I_D = 3.0 A)
- Low C_{iss} C_{iss} = 800 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1756G	Power SOP8

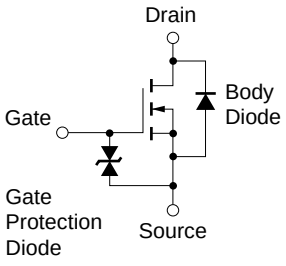
PACKAGE DRAWING (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	20	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±12.0	V
Drain Current (DC)	$I_{D(DC)}$	±6.0	A
Drain Current (Pulse)[Note1]	$I_{D(pulse)}$	±24	A
Total Power Dissipation (1 unit)[Note2]	P_T	1.7	W
Total Power Dissipation (2 unit)[Note2]	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. T_A = 25 °C, Mounted on ceramic substrate of 2000 mm^2 x 1.1 mm

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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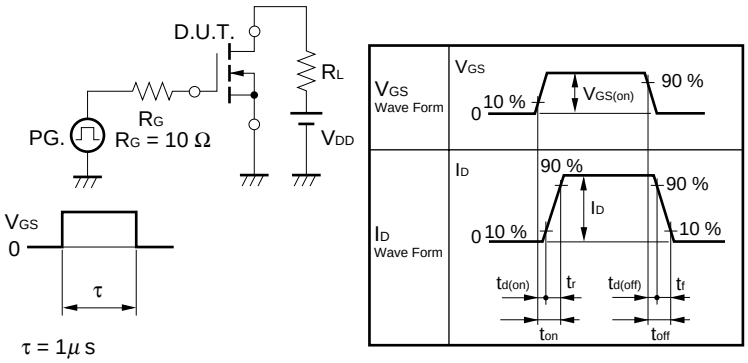
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

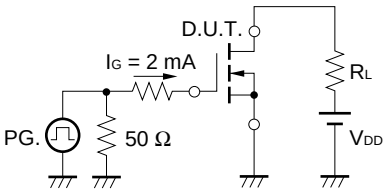
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 4.5 V, I_D = 3.0 A		20.0	30	mΩ
	$R_{DS(on)2}$	V_{GS} = 2.5 V, I_D = 3.0 A		25.8	40	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1.0 mA	0.5	0.7	1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 3.0 A	4.0	12		S
Drain Leakage Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±12.0 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		800		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		360		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		70		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 3.0A		110		ns
Rise Time	t_r	$V_{GS(on)}$ = 4.0 V		425		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 10 V		1050		ns
Fall Time	t_f	R_G = 10 Ω		1200		ns
Total Gate Charge	Q_G	I_D = 6.0 A		11		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 16 V		2.0		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 4.0 V		4.6		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 6.0 A, V_{GS} = 0 V		0.8		V

TEST CIRCUIT 1 SWITCHING TIME



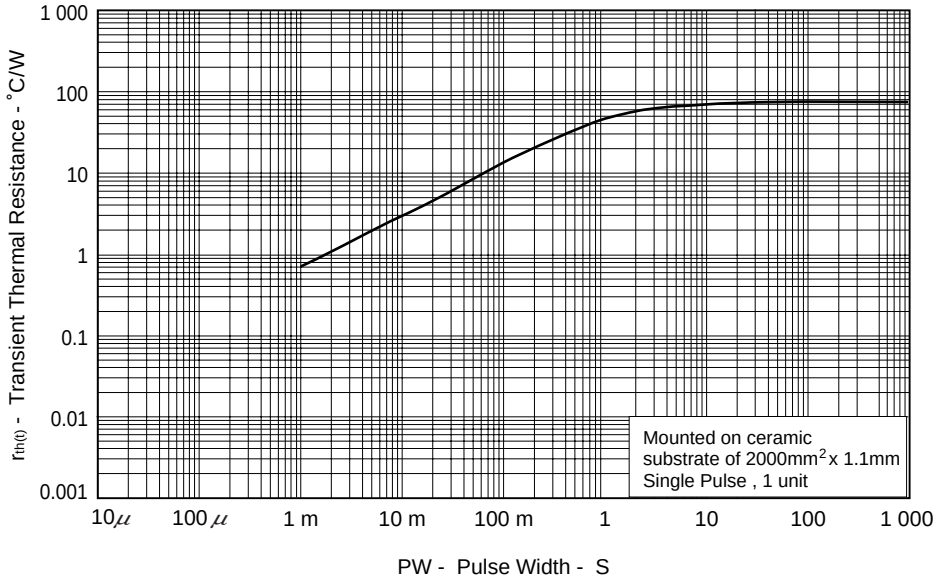
τ = 1μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

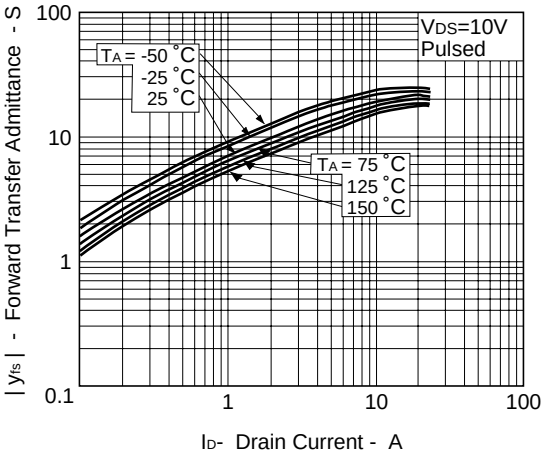


TYPICAL CHARACTERISTICS (T_A = 25 °C)

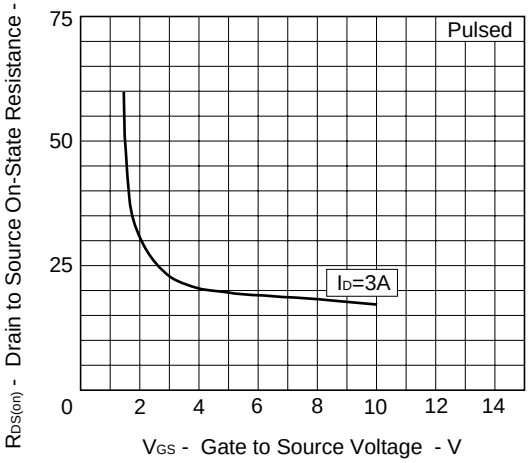
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



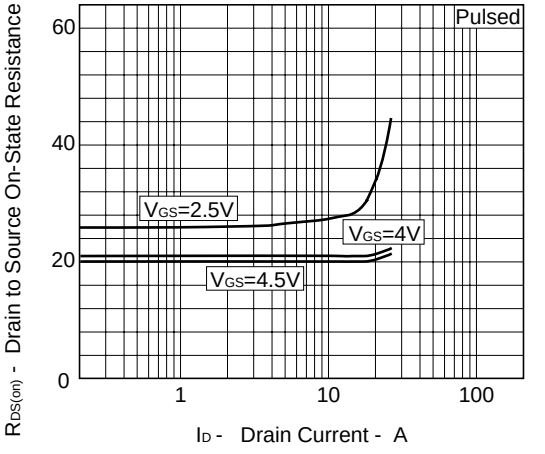
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



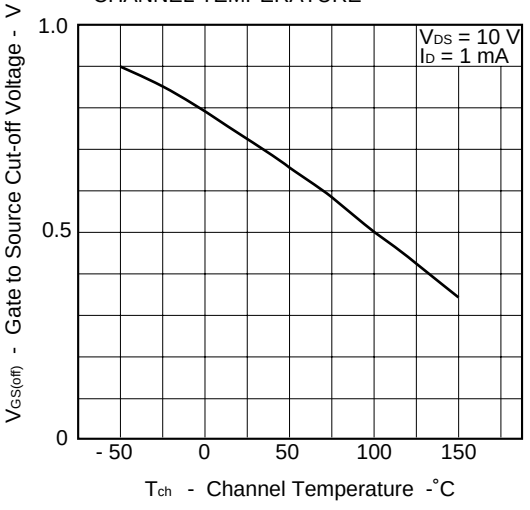
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



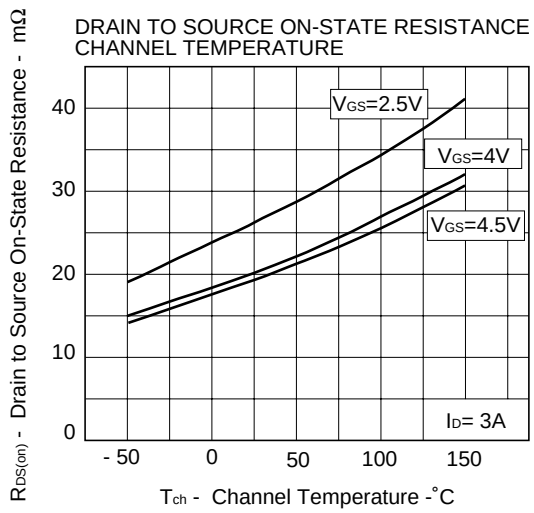
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



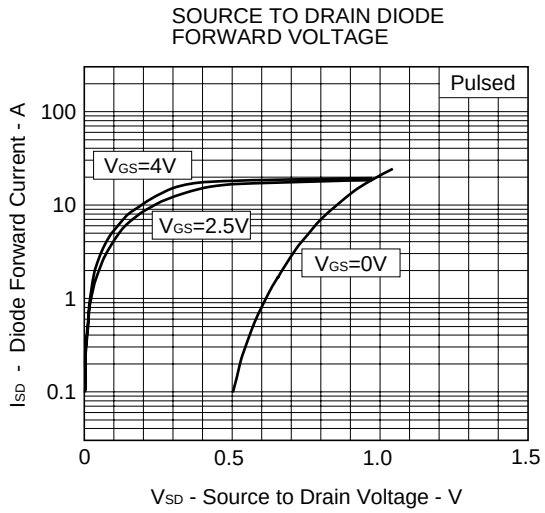
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



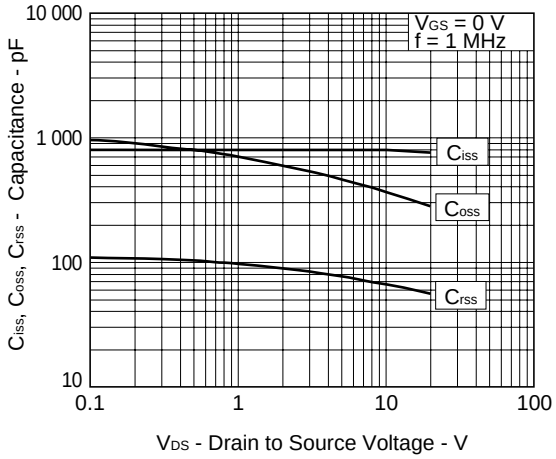
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



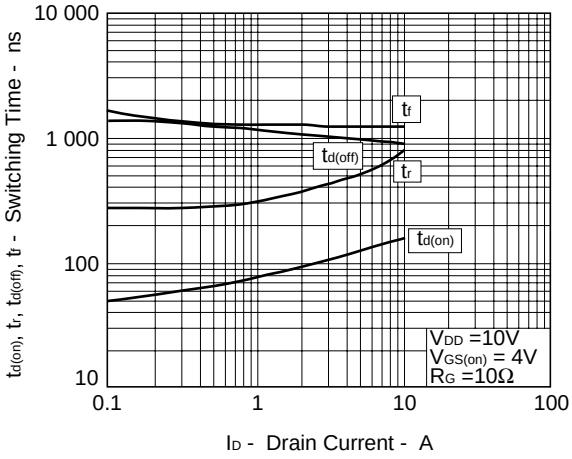
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



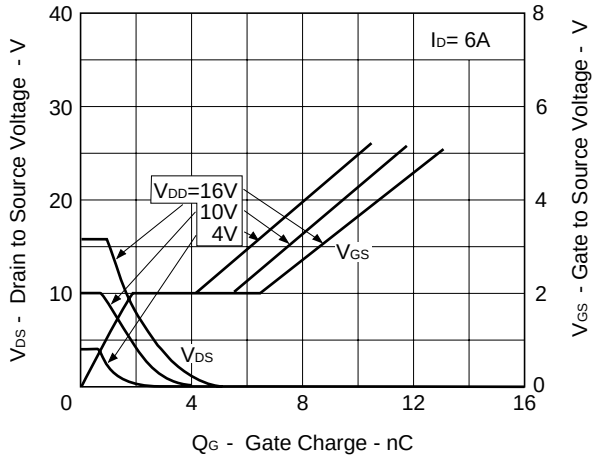
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



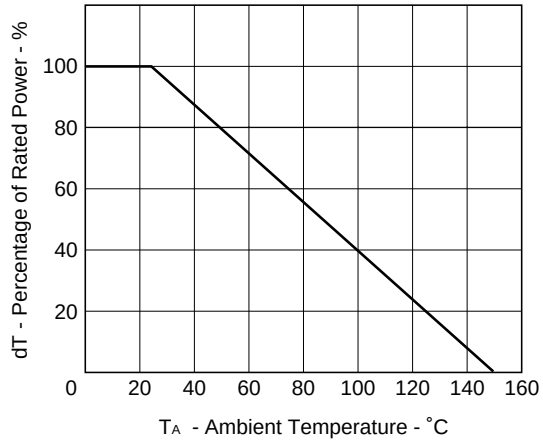
SWITCHING CHARACTERISTICS



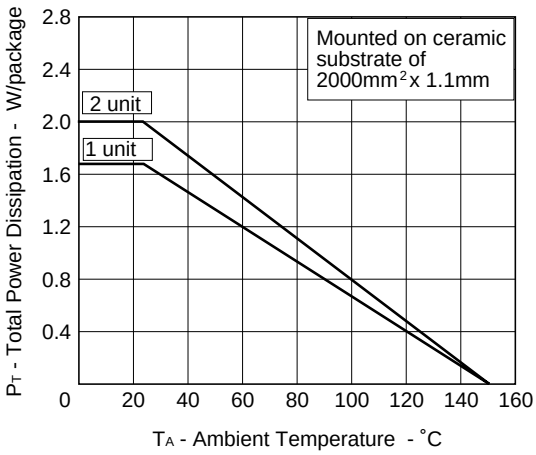
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



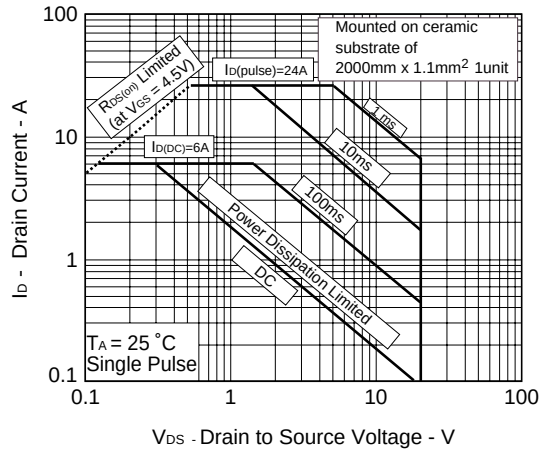
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



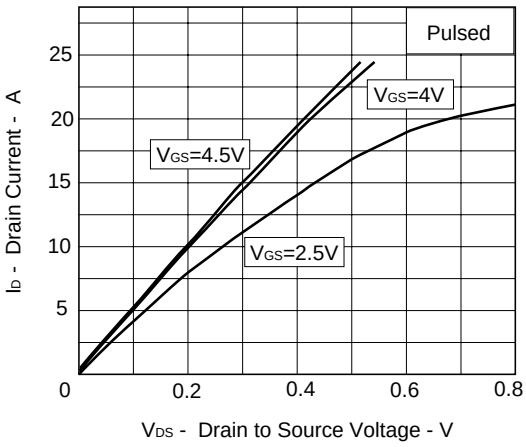
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



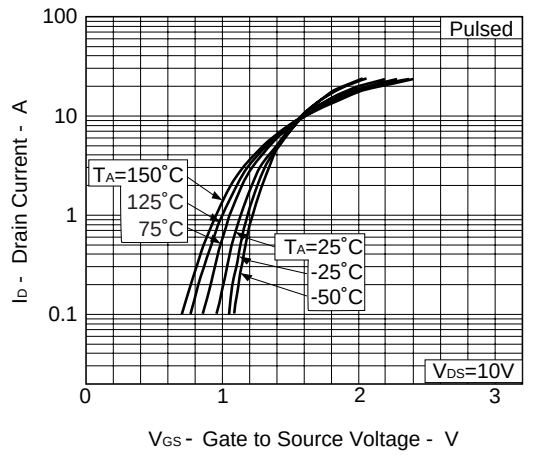
FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS



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