9/27/02

Errata: CS4340A Rev. B

(Reference CS4340A Data Sheet revision DS590PP1 dated JUN' 02)

*All references to the CS4340A mentioned below shall be taken to refer to revision B of the CS4340A product. The hardware revision code can be found in the 10-character field printed below the part number on each chip. The letter that appears as the fifth character from the right is the revision code (e.g. RNAZD**B**0222 is a Revision B part).*

- The device does not function properly during certain phase relationships of MCLK and SCLK in Quad-Speed Mode. MCLK must not transition 0 ns to 8 ns after the rising edge of SCLK. Should a transition occur within this window, the resulting symptom will be severe distortion of the audio signal.

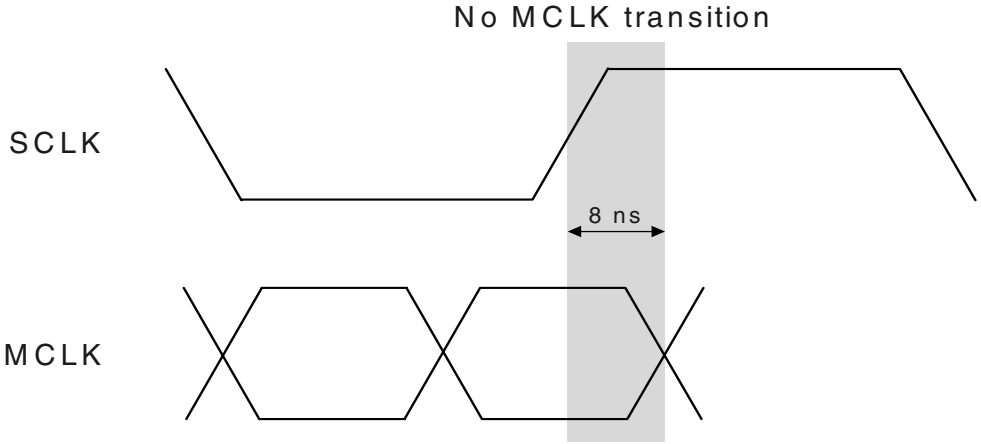

Figure 1. SCLK to MCLK Timing

Note: The timing relationship is limited to a window of less than 1 ns on any individual part. However, the location of this 1 ns window across multiple devices is within the 8 ns window shown in the figure above.

CONTACTING CIRRUS LOGIC SUPPORT

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **<http://www.cirrus.com/corporate/contacts/sales.cfm>**