File Number **582**

2N6354

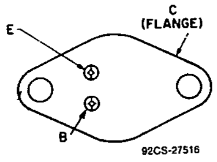
120-V, 10-A, 140-W Silicon N-P-N Planar Transistor

For Switching Applications in Military and Industrial Equipment

Features:

- *High $V_{CEO}(sus)$: 120 V*
- *Maximum safe-area-of operation curves*
- *Low saturation voltage: $V_{CE}(sat) \leq 0.5$ V*
- *Fast switching speeds*
- *High dissipation ratings: P_T = 80 W at 100° C*
  = 140 W at 25° C

TERMINAL DESIGNATIONS



JEDEC TO-204AA

RCA type 2N6354• is an epitaxial silicon n-p-n planar transistor with a multiple-emitter-site structure. The device is supplied in the JEDEC TO-204AA package.

Typical high-speed switching applications for the 2N6354 include switching-control amplifiers operated from a 48-V (nominal) power supply, power gates, switching regulators, dc-dc converters, and power oscillators.

• Formerly RCA Dev. No. TA7534.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

* COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	150 V
COLLECTOR-TO-EMITTER VOLTAGE:	
With base open, sustaining, $V_{CEO}(sus)$	120 V
* With external base-to-emitter resistance (R_{BE}) = 500 Ω, V_{CEX}	130 V
* EMITTER-TO-BASE VOLTAGE, V_{EBO}	6.5 V
* COLLECTOR CURRENT (Continuous), I_C	10 A
COLLECTOR CURRENT (Peak)	12 A
* BASE CURRENT (Continuous), I_B	5 A
* TRANSISTOR DISSIPATION, P_T	
At case temperatures up to 25° C and V_{CE} up to 25 V	140 W
At case temperature of 100° C and V_{CB} of 20 V	80 W
At case temperatures up to 25° C and V_{CE} above 25 V	See Figs. 1 & 3
At case temperatures above 25° C and V_{CE} above 25 V	See Figs. 1, 2, & 3
* TEMPERATURE RANGE:	
Storage & Operating (Junction)	-65 to 200° C
* PIN TEMPERATURE (During Soldering):	
At distance ≥ 1/32 in. (0.8 mm) from case for 10 s max.	230° C

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* In accordance with JEDEC registration data format JS-6 RDF-1.

2N6354

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
		DC VOLTAGE (V)				DC CURRENT (A)		2N6354		
		V_{CE}	V_{CB}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	
* Collector-Cutoff Currentt With emitter open	I_{CBO}		150					–	5	mA
With base open	I_{CEO}	100					0	–	20	
* With base-emitter junction reverse-biased	I_{CEV}	140			0			–	10	
* At T_C = 125°C	I_{CEV}	140			0			–	20	
* Emitter-Cutoff Current	I_{EBO}			6.5		0		–	5	mA
* Emitter-to-Base Voltage	V_{EBO}						0.005	6.5	–	V
* Collector-to-Emitter Voltage: At breakdown, with base open	$V_{(BR)CEO}$					0.2	0	120^b	–	V
With external base-to emitter resistance (R_{BE}) ≤ 100 Ω	$V_{CER(sus)}^f$					0.2	0	130^b	–	
* Saturation Voltage: Collector-to-Emitter	$V_{CE(sat)}$					5^a 10^a	0.5 1.0	– –	0.5 1	V
Base-to-Emitter	$V_{BE(sat)}$					5^a 10^a	0.5 1.0	– –	1.3 2	
* DC Forward Current Transfer Ratio	h_{FE}	2 2				5^a 10^a		20 10	150 100	
Forward-Bias Second-Breakdown Collector Current[d]	$I_{S/b}^c$	25 45						5.5 0.5	– –	A
Second-Breakdown Energy (With base reverse biased, R_{BE}=51 Ω, L = 25 μH)	$E_{S/b}^g$			1		5		0.3	–	mJ
* Magnitude of Common Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 10 MHz)	$\|h_{fe}\|$	10				1		8	–	
* Saturated Switching Time: (See Figs. 11 & 12) Rise Time	t_r	V_{CC} = 30				5 10	0.5^e 1^e	– –	0.3 1	μs
Storage Time	t_{s1}					5 10	0.5^e 1^e	– –	1 0.6	
Storage Time (No Load)	t_{s2}					0.5	0.5^e	–	2	
Fall Time	t_f					5 10	0.5^e 1^e	– –	0.2 0.2	
Output Capacitance (f = 1 MHz)	C_{obo}		10					–	300	pF
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$	20				1		–	1.25	°C/W

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*In accordance with JEDEC registration data format JS-6 RDF-1.

[a] Pulsed: pulse duration ≤350 μs, duty factor = 2%.

[b] CAUTION: The collector-to-emitter voltages, $V_{(BR)CEO}$ and $V_{CER(sus)}$, MUST NOT be measured on a curve tracer. These voltages should be measured by means of the test circuit shown in Fig.5.

[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

[d] Pulsed; 1-s non-repetitive pulse.

[e] $I_{B_1} = I_{B_2}$ = value shown.

[f] L = 15 mH

[g] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = \frac{1}{2}LI^2$ where L is a series load or leakage inductance and I is the peak collector current.

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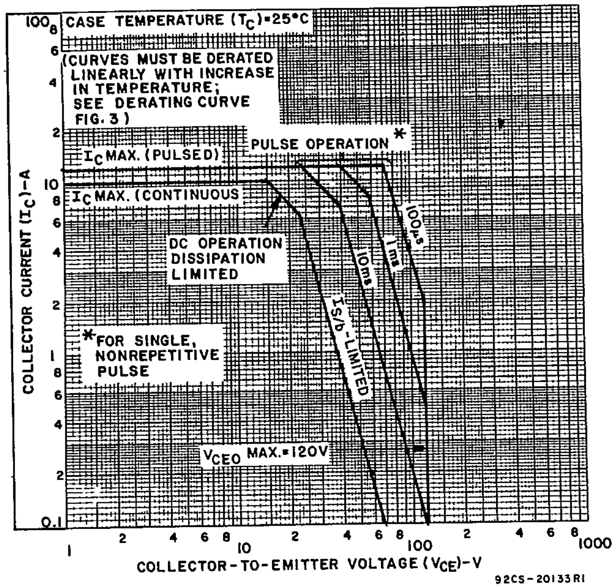

Fig. 1 - Maximum operating areas.

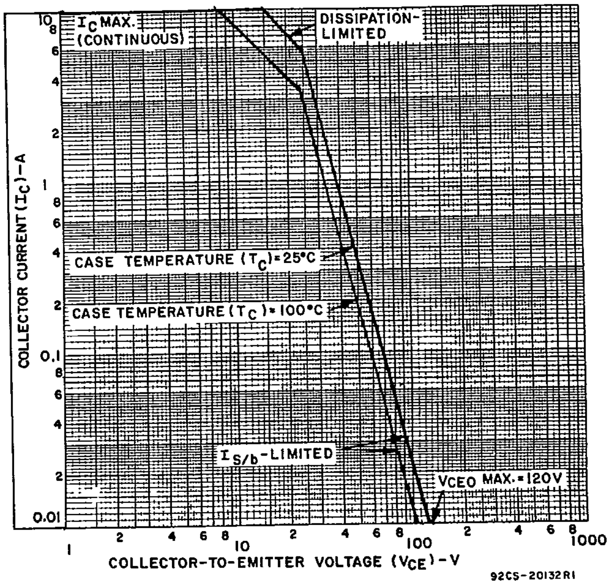

Fig. 2 - Maximum operating areas.

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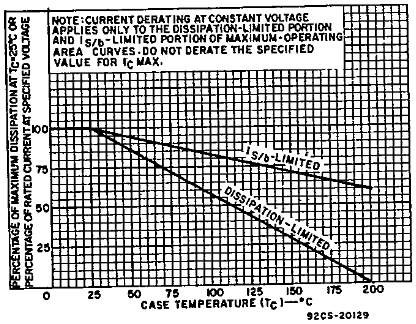


Fig. 3 - Derating curves.

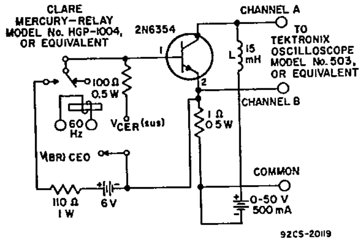
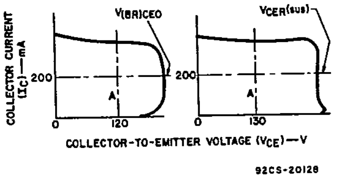


Fig. 4 - Circuit used to measure voltages V(BR)CEO and VCER(sus).



NOTE: The voltages V(BR)CEO and VCER(sus) are acceptable when the trace falls to the right of and above point "A".

Fig. 5 - Oscilloscope display for V(BR)CEO and VCER(sus) measurement (test circuit shown in Fig. 5).

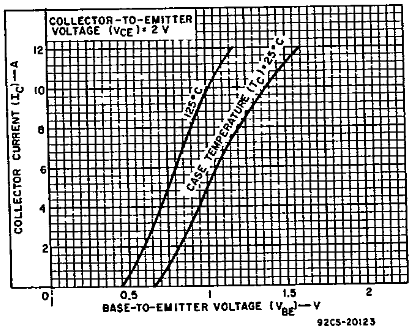


Fig. 6 - Typical transfer characteristics.

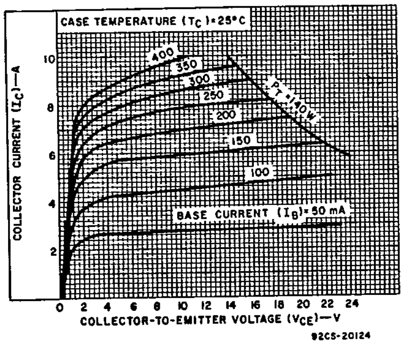


Fig. 7 - Typical output characteristics.

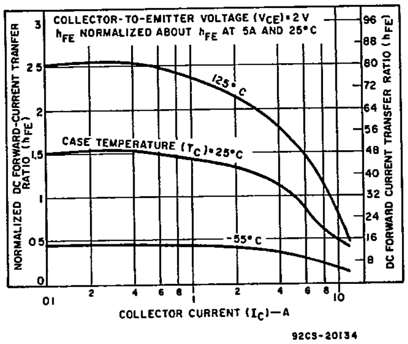


Fig. 8 - Typical normalized dc beta characteristics.

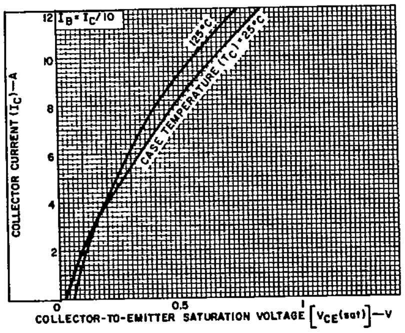


Fig. 9 - Typical saturation voltage characteristics.

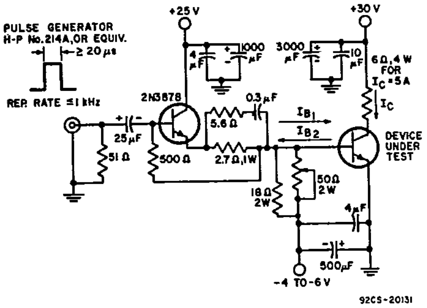


Fig. 10 - Circuit used to measure switching times.

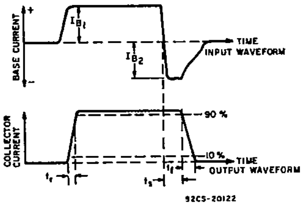


Fig. 11 - Phase relationship between input and output currents showing reference points for specification of switching times (test circuit shown in Fig. 11).

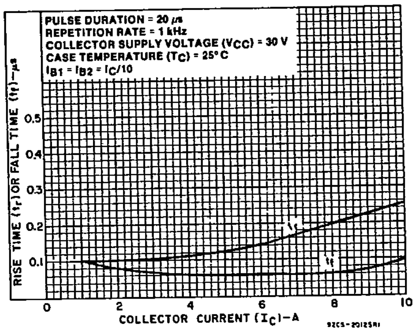


Fig. 12 - Typical rise-and fall-time characteristics.

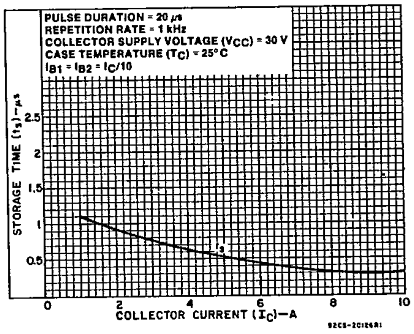


Fig. 13 - Typical storage-time characteristics.