IRF320, IRF321, IRF322, IRF323

File Number **1569**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.5A and 3.0A, 350V-400V

$r_{DS}(on)$ = 1.8 Ω and 2.5 Ω

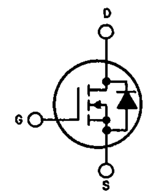
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF320, IRF321, IRF322 and IRF323 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

N-CHANNEL ENHANCEMENT MODE



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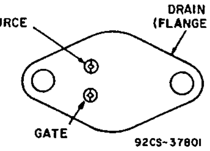
TERMINAL DIAGRAM

TERMINAL DESIGNATION



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JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		IRF320	IRF321	IRF322	IRF323	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0 32 (See Fig 14)				W/°C
I_{LM}	Inductive Current, Clamped (See Fig. 15 and 16) L = 100μH	12	12	10	10	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in (1.6mm) from case for 10s)				°C

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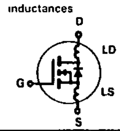
Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF320 IRF322	400	–	–	V	V_{GS} = 0V
		IRF321 IRF323	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4 0	V	$V_{DS} = V_{GS}$, I_D = 250μA
I_{GSS}	Gate Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF320 IRF321	3.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		IRF322 IRF323	2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF320 IRF321	–	1.5	1.8	Ω	V_{GS} = 10V I_D = 1 5A
		IRF322 IRF323	–	1 8	2 5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1 0	2.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max}$, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn On Delay Time	ALL	–	20	40	ns	V_{DD} = 0 5 BV_{DSS}, I_D = 1 5A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4 0A, V_{DS} = 0.8 Max. Rating See Fig 18 for test circuit. (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6 0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5 0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances
L_S	Internal Source Inductance	ALL	–	12 5	–	nH	Measured from the source pin, 6 mm (0.25 in) from header and source bonding pad.

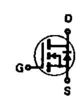


Thermal Resistance

R_{thJC}	Junction to Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0 1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF320 IRF321	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF322 IRF323	–	–	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF320 IRF321	–	–	12	A	
		IRF322 IRF323	–	–	10	A	
V_{SD}	Diode Forward Voltage ②	IRF320 IRF321	–	–	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
		IRF322 IRF323	–	–	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn on Time	ALL	Intrinsic turn-on time is negligible. Turn on speed is substantially controlled by $L_S + L_D$				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2% ③ Repetitive Rating: Pulse width limited by max. junction temperature
See Transient Thermal Impedance Curve (Fig. 5).

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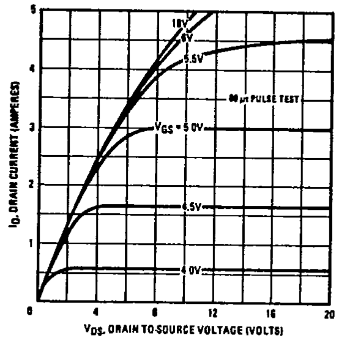

Fig. 1 – Typical Output Characteristics

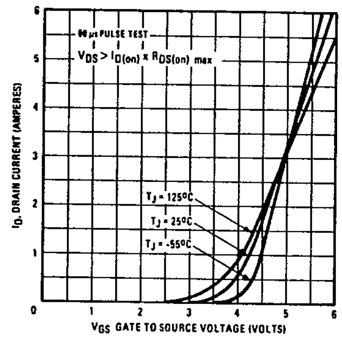

Fig. 2 – Typical Transfer Characteristics

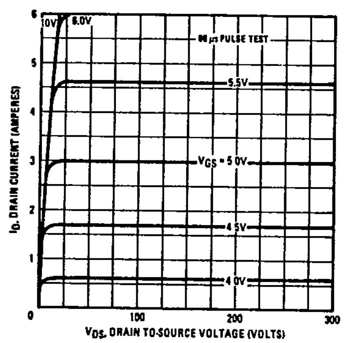

Fig. 3 – Typical Saturation Characteristics

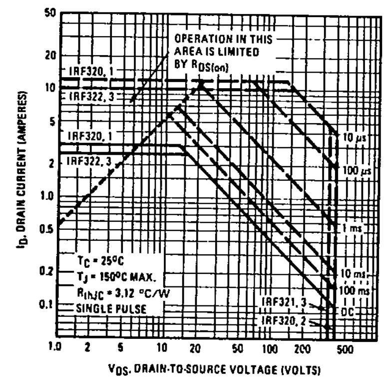

Fig. 4 – Maximum Safe Operating Area

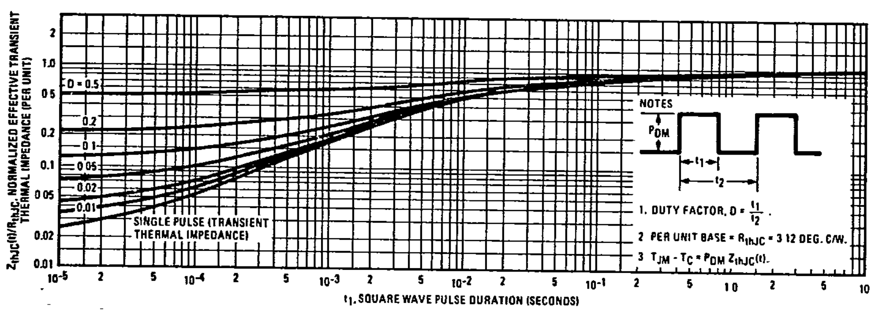

Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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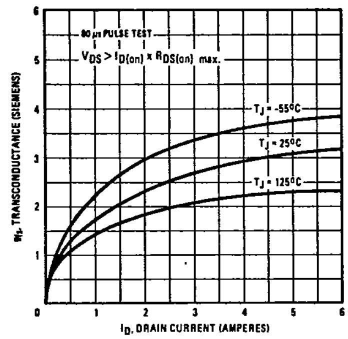

Fig. 6 – Typical Transconductance Vs. Drain Current

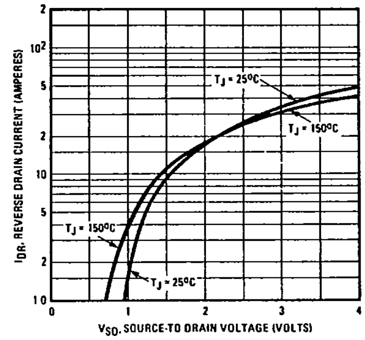

Fig. 7 – Typical Source-Drain Diode Forward Voltage

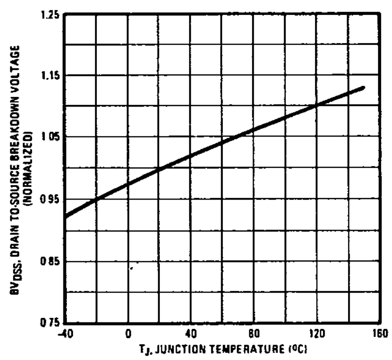

Fig. 8 – Breakdown Voltage Vs. Temperature

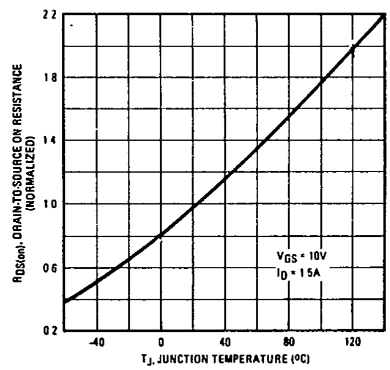

Fig. 9 – Normalized On-Resistance Vs. Temperature

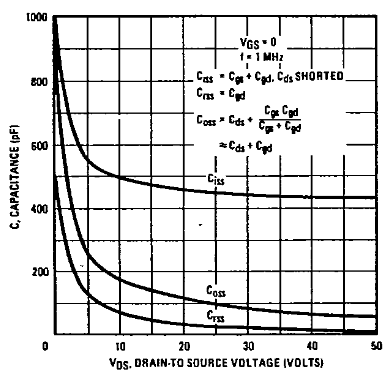

Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

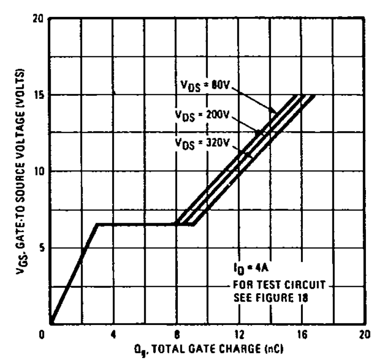

Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

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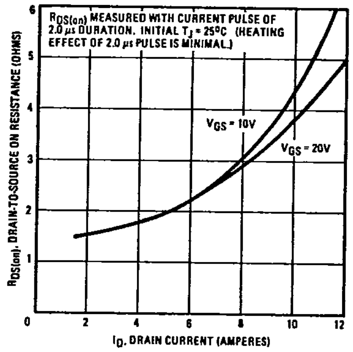

Fig. 12 – Typical On-Resistance Vs. Drain Current

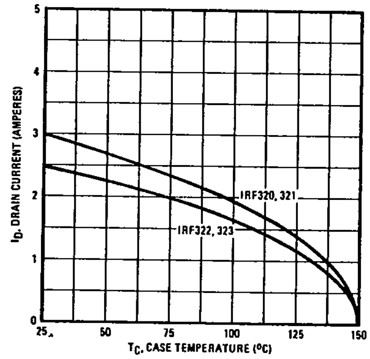

Fig. 13 – Maximum Drain Current Vs. Case Temperature

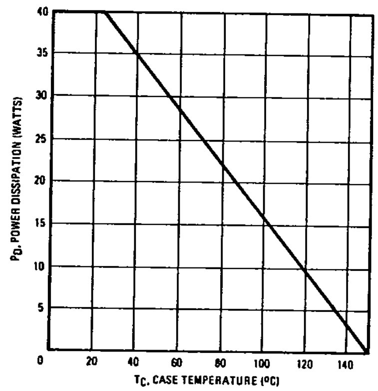

Fig. 14 – Power Vs. Temperature Derating Curve

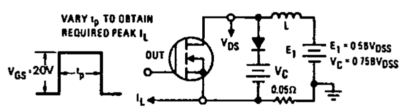

Fig. 15 – Clamped Inductive Test Circuit

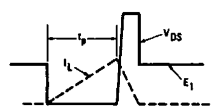

Fig. 16 – Clamped Inductive Waveforms

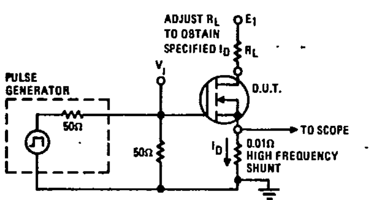

Fig. 17 – Switching Time Test Circuit

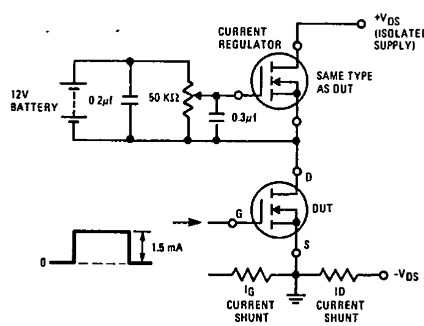

Fig. 18 – Gate Charge Test Circuit