File Number **1827**

IRF450, IRF451, IRF452, IRF453

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

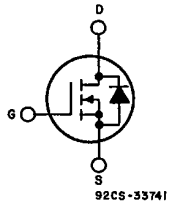
12 A and 13 A, 450 V - 500 V
$r_{DS}(on)$ = 0.4 Ω and 0.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF450, IRF451, IRF452 and IRF453 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

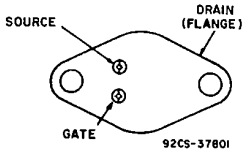
The IRF-types are supplied in the JEDEC TO-204AA metal package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

Absolute Maximum Ratings

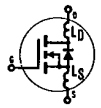
	Parameter	IRF450	IRF451	IRF452	IRF453	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	13	13	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	52	52	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH				A
		52	52	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF450, IRF451, IRF452, IRF453

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF450, IRF452	500	–	–	V	V_{GS} = 0V
		IRF451, IRF453	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF450, IRF451	13	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF452, IRF453	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF450, IRF451	–	0.3	0.4	Ω	V_{GS} = 10V, I_D = 7.0A
		IRF452, IRF453	–	0.4	0.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	11	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 7.0A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	400	600	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 210V, I_D = 7.0A, Z_O = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150	ns	
t_f	Fall Time	ALL	–	–	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	82	120	nC	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentialiv independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	40	–	nC	
Q_{gd}	Gate Drain ("Miller") Charge	ALL	–	42	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF450, IRF451	–	–	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF452, IRF453	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF450, IRF451	–	–	52	A	
		IRF452, IRF453	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	IRF450, IRF451	–	–	1.4	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
		IRF452, IRF453	–	–	1.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1300	–	ns	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.4	–	μC	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF450, IRF451, IRF452, IRF453

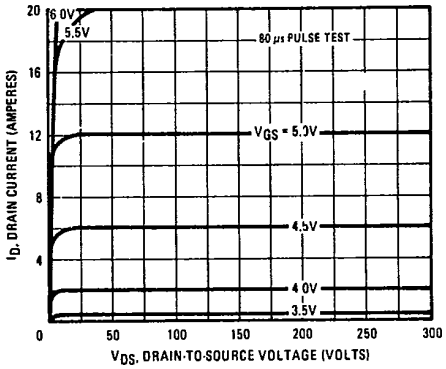


Fig. 1 – Typical Output Characteristics

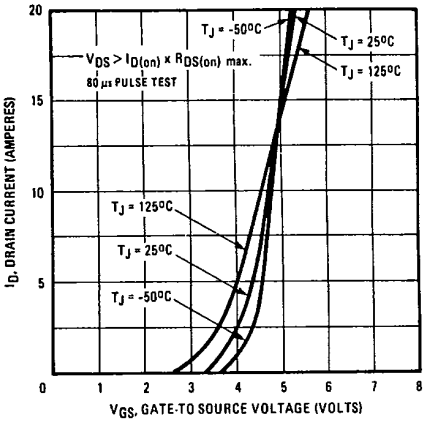


Fig. 2 – Typical Transfer Characteristics

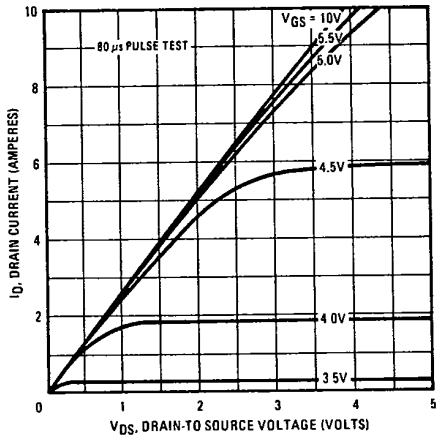


Fig. 3 – Typical Saturation Characteristics

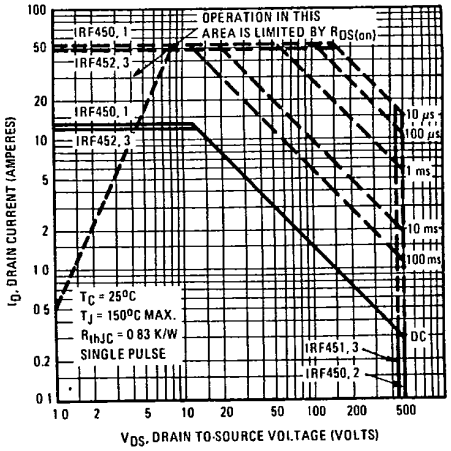


Fig. 4 – Maximum Safe Operating Area

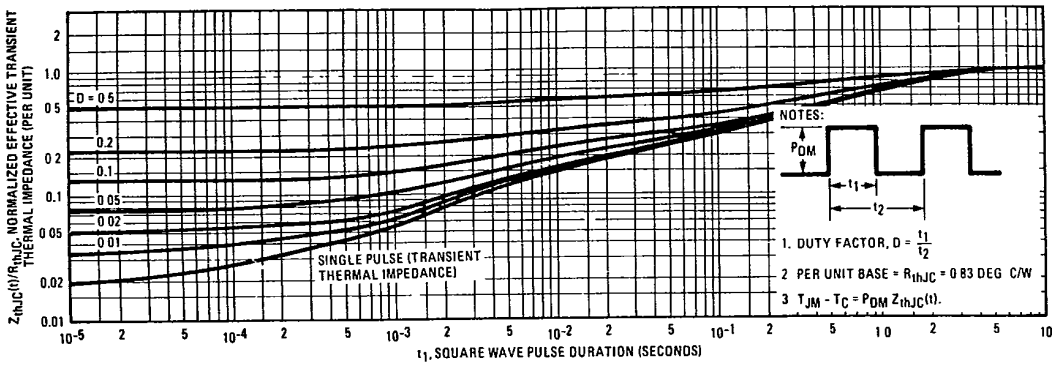


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF450, IRF451, IRF452, IRF453

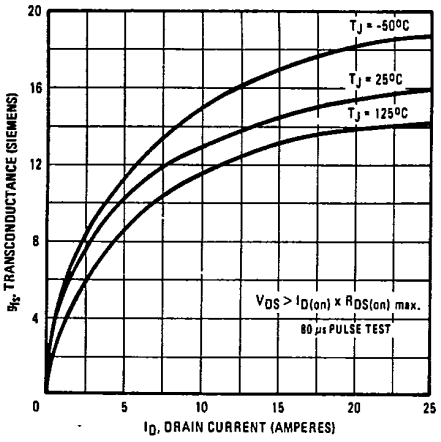


Fig. 6 — Typical Transconductance Vs. Drain Current

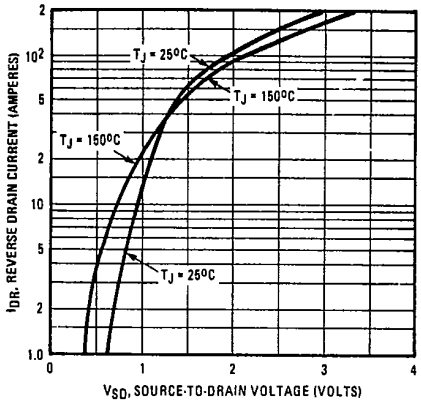


Fig. 7 — Typical Source-Drain Diode Forward Voltage

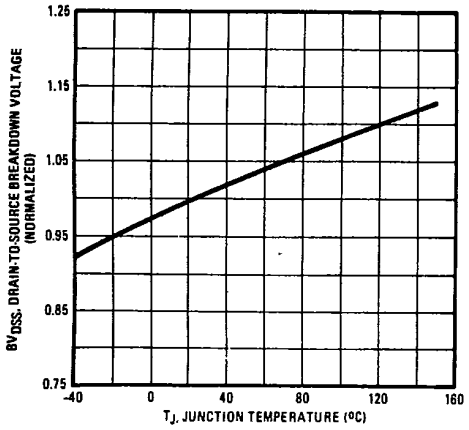


Fig. 8 — Breakdown Voltage Vs. Temperature

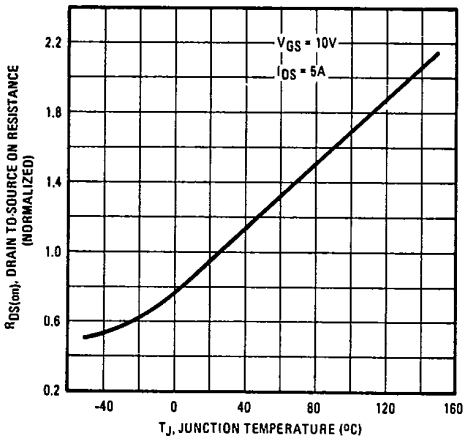


Fig. 9 — Normalized On-Resistance Vs. Temperature

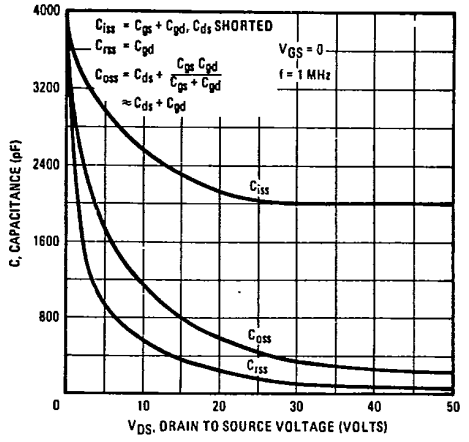


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

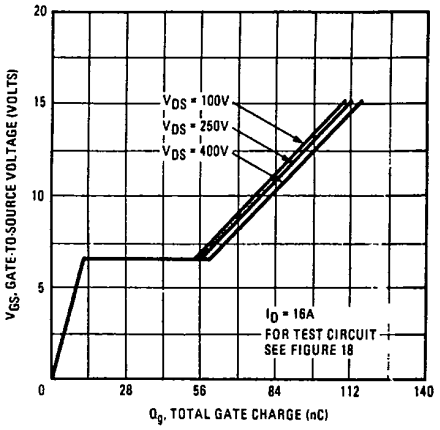


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

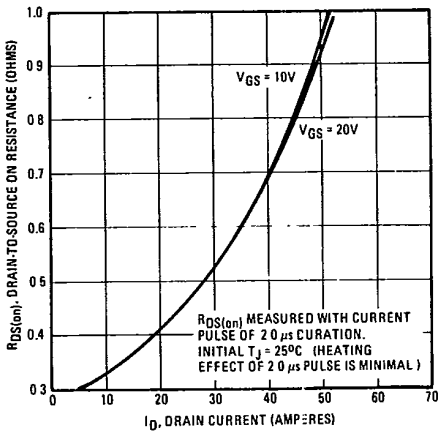


Fig. 12 – Typical On-Resistance Vs. Drain Current

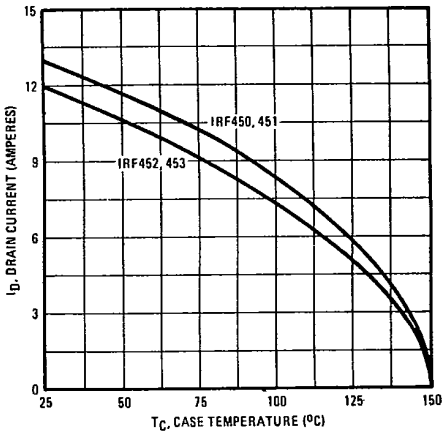


Fig. 13 – Maximum Drain Current Vs. Case Temperature

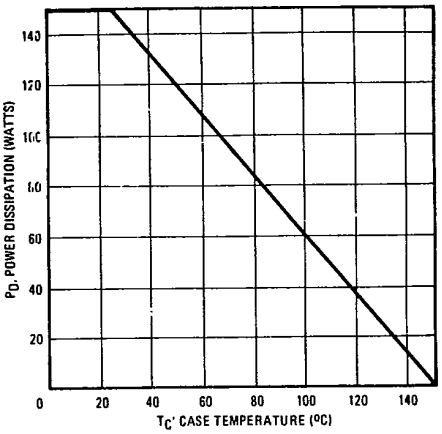


Fig. 14 – Power Vs. Temperature Derating Curve

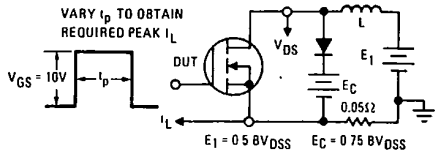


Fig. 15 – Clamped Inductive Test Circuit

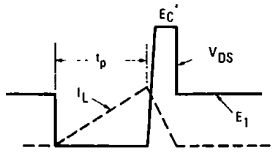


Fig. 16 – Clamped Inductive Waveforms

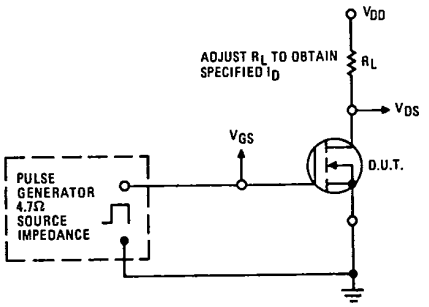


Fig. 17 – Switching Time Test Circuit

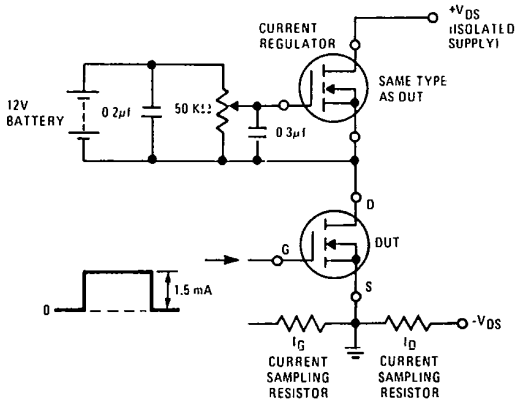


Fig. 18 – Gate Charge Test Circuit