

FEATURES

- designed to drive class D integrated receivers
- MPO range externally adjustable
- 150 μ A typical current drain
- 46 dB of adjustable gain
- low external parts count

STANDARD PACKAGING

- 8 Pin MICROpac
- 8 Pin PLID[®]
- 8 Pin SLT
- Chip (56 x 56 mils)
 Au Bump

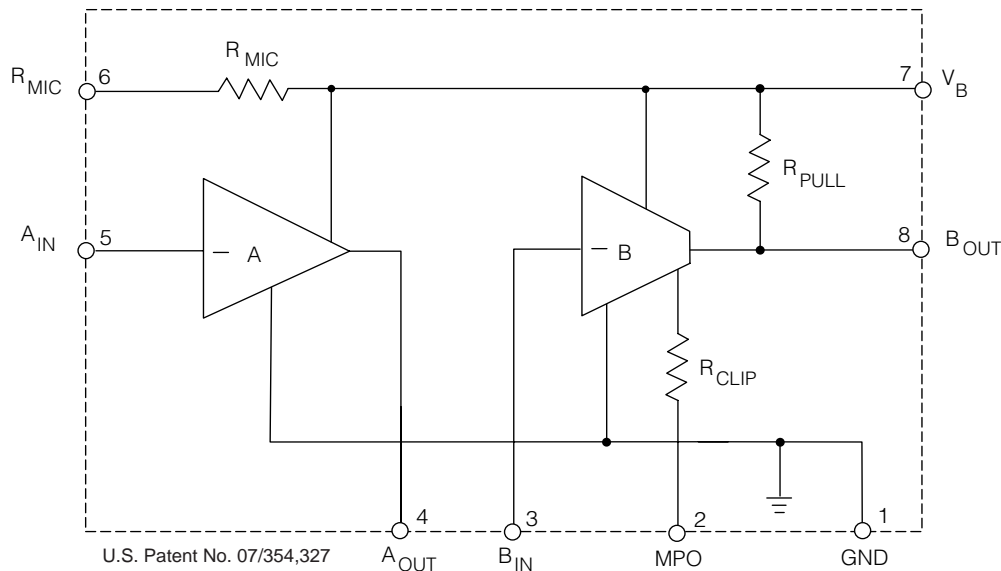
DESCRIPTION

The GL504 is a low current preamplifier designed to drive the class D series of integrated receivers. This preamp has a built-in symmetrical peak clipping output limiter, 46 dB of adjustable gain, and requires few external components.

Composed of two stages, an inverting preamp with gain of 28 dB, and a transconductance block with gain of 18 dB, the GL504 is easily configured for mid-supply reference as required by the class D receivers.

The two stages of the GL504 must be AC coupled in order to maintain the DC bias conditions of each stage. Also, a 48 k Ω resistor, between the output and ground, is used to keep the receivers at mid-supply reference. The minimal total parts count, excluding an MPO variable resistor, requires 3 capacitors, a 100 k Ω volume control and the 48 k Ω bias resistor at the output.

The GL504 is capable of providing a flat frequency response with very little distortion.



BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

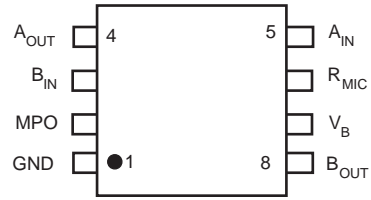
PARAMETER	VALUE / UNITS
Supply Voltage	5 V
Operating Temperature	-10°C to +40°C
Storage Temperature	-20°C to +70°C

CAUTION

Class 1 ESD Sensitivity

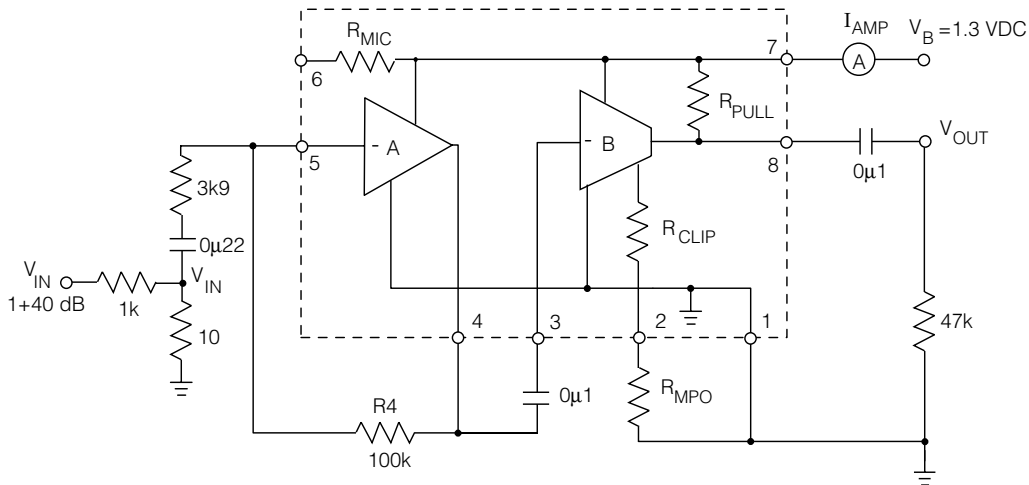


PIN CONNECTION



ELECTRICAL CHARACTERISTICS (refer to test circuit) Supply Voltage = 1.3 V, Test Frequency 1kHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier Current	I_{AMP}	$R_{MPO} = 0$	75	150	225	μA
Microphone Resistance	R_{MIC}		3.0	4.0	5.3	$k\Omega$
Input Referred Noise	IRN	NFB 0.2 to 10kHz at 12 dB/oct	-	2	-	μV_{RMS}
Gain	A_V	$V_{IN} = -80$ dBV	44.5	46.5	48.5	dB
MPO Level	MPO	$V_{IN} = -50$ dBV $R_{MPO} = 0$	-16	-14	-12	dBV
Change in MPO	ΔMPO	$V_{IN} = -50$ dBV $R_{MPO} = 10$ $k\Omega$	10	12	14	dB
Preamp A input Bias Current	$I_{BIAS A}$		-25	0	+25	nA
Pull-up Resistance	R_{PULL}		40	48	58	$k\Omega$
Gain Loss	$\Delta GAIN$	$R_4 = 10$ k, $V_{IN} = -70$ dBV, $R_{MPO} = 50$ k	-	0	2.5	dB



All resistors in ohms, all capacitors in μF , unless otherwise stated.

Fig. 1 Test Circuit

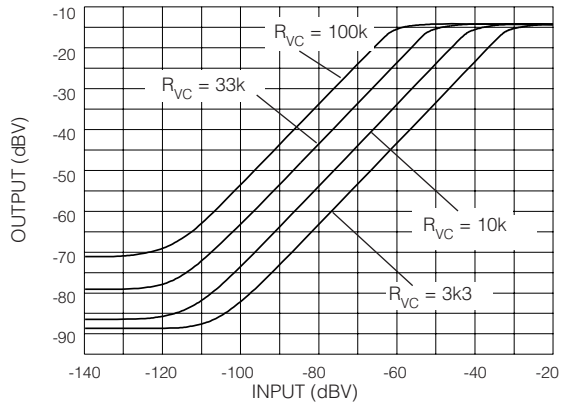


Fig. 4 I/O Curves at Various R_{VC} Settings

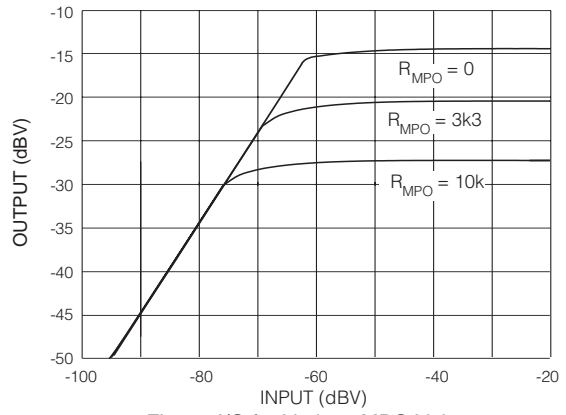


Fig. 5 I/O for Various MPO Values

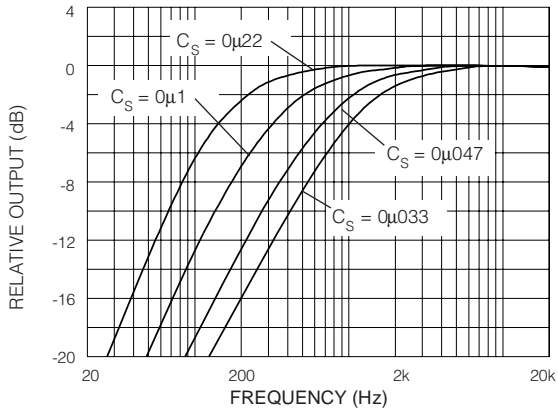


Fig. 6 Frequency Response for Various C_S Values

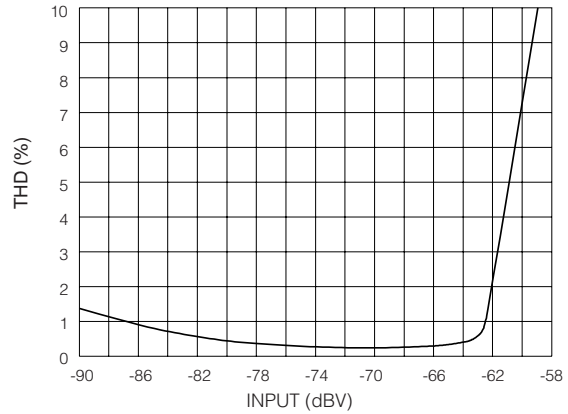


Fig. 7 Distortion vs Input Level ($R_{VC} = 100k\Omega$)

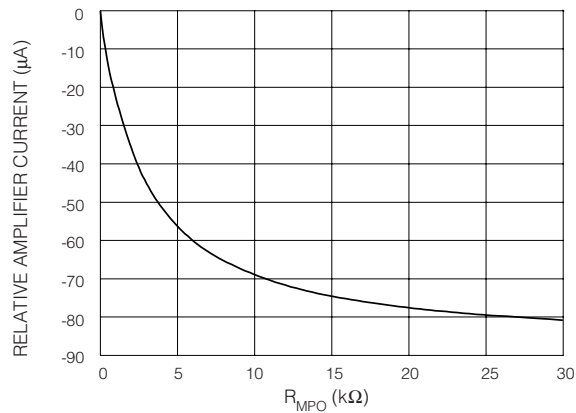


Fig. 8 Quiescent Current vs MPO Resistance

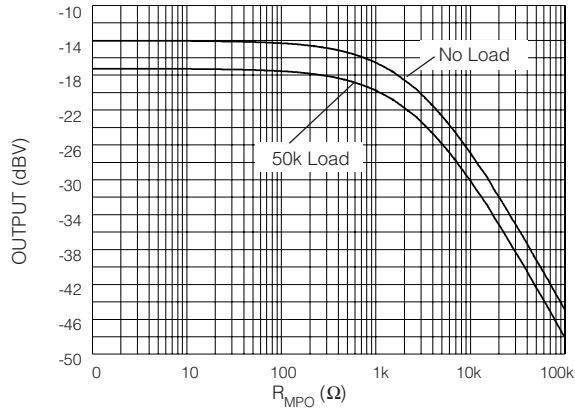


Fig. 9 Output vs MPO Resistance

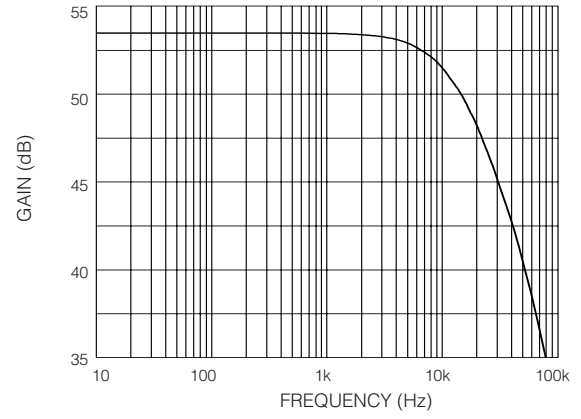


Fig. 10 Preamp A Open Loop Voltage Gain

DOCUMENT IDENTIFICATION: DATA SHEET
 The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:
 Updated to Data sheet