

FEATURES

- Full Four-Quadrant Multiplying
- Low Feedthrough: 1/2 LSB @ 200 kHz
- Fast Settling: 100 ns (typ.)
- Low Power Dissipation
- Low Cost
- 5 V/15 V Operation
- Buffered Version: MP7524/XRD7524

APPLICATIONS

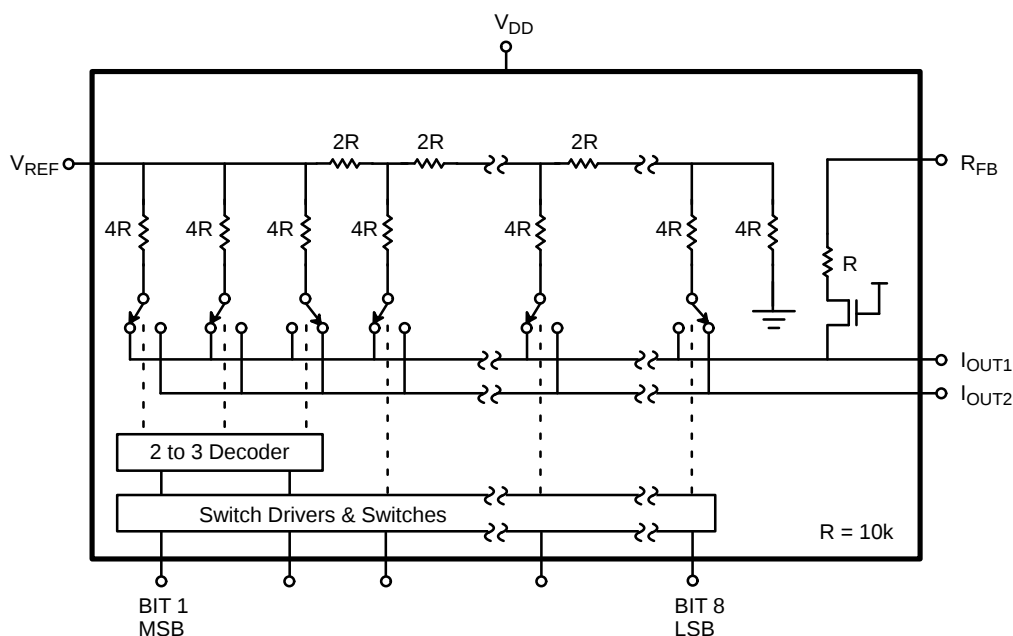
- Battery Operated Equipment
- Low Power, Ratiometric A/D Converters
- Digitally Controlled Gain Circuits
- Digitally Controlled Attenuators
- CRT Character Generation
- Low Noise Audio Gain Control

GENERAL DESCRIPTION

The MP7523/XRD7523 is a low cost multiplying Digital-to-Analog Converter. The device uses an advanced thin-film-on-CMOS technology to provide 8-bit resolution with accuracy to 10-bits and very low power dissipation.

The MP7523/XRD7523's excellent multiplying characteristics and low cost allow it to be used in a wide ranging field of applications such as: low noise audio gain control, CRT character generation, motor speed control, digitally controlled attenuators, etc.

SIMPLIFIED BLOCK DIAGRAM

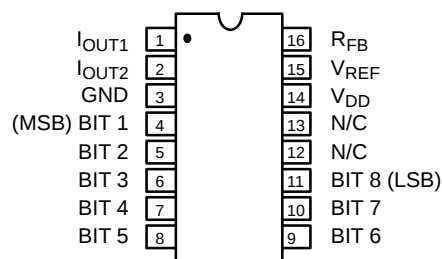


3 Segment D/A Converter with Termination to DGND
Logical "1" at Digital Input Steers Current to I_{OUT1}

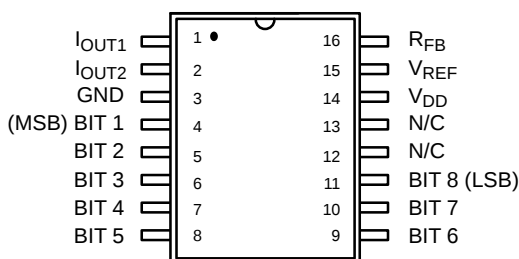
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	-40 to +85°C	MP7523JN	$\pm 1/2$	± 1	± 1.8
Plastic Dip	-40 to +85°C	MP7523KN	$\pm 1/4$	± 1	± 1.8
SOIC (Jedec, 0.300")	-40 to +85°C	MP7523JS	$\pm 1/2$	± 1	± 1.8
SOIC (Jedec, 0.300")	-40 to +85°C	MP7523KS	$\pm 1/4$	± 1	± 1.8
SOIC (Jedec, 0.150")	-40 to +85°C	XRD7523AID-J	$\pm 1/2$	± 1	± 1.8
SOIC (Jedec, 0.150")	-40 to +85°C	XRD7523AID-K	$\pm 1/4$	± 1	± 1.8
SOP (EIAJ)	-40 to +85°C	XRD7523AIK-J	$\pm 1/2$	± 1	± 1.8
SOP (EIAJ)	-40 to +85°C	XRD7523AIK-K	$\pm 1/4$	± 1	± 1.8

PIN CONFIGURATIONS



16 Pin PDIP (0.300")



16 pin SOIC (Jedec, 0.300")
16 pin SOIC (Jedec, 0.150")
16 pin SOP (EIAJ, 5.5 mm)

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I _{OUT1}	Current Output 1
2	I _{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Bit 1 (MSB)
5	BIT 2	Bit 2
6	BIT 3	Bit 3
7	BIT 4	Bit 4
8	BIT 5	Bit 5

PIN NO.	NAME	DESCRIPTION
9	BIT 6	Bit 6
10	BIT 7	Bit 7
11	BIT 8	Bit 8
12	N/C	No Connection
13	N/C	No Connection
14	V _{DD}	Positive Power Supply
15	V _{REF}	Reference Input Voltage
16	R _{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS

($V_{DD} = +15\text{ V}$, $V_{REF} = +10\text{ V}$ unless otherwise noted)

Parameter	Symbol	Min	25°C Typ	Max	Tmin to Tmax Min	Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE¹								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line (Max INL – Min INL) / 2
J				$\pm 1/2$		$\pm 1/2$		
K				$\pm 1/4$		$\pm 1/4$		
Monotonicity								Guaranteed over temp
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J				± 1		± 1		
K				± 1		± 1		
Gain Error	GE			± 1.5		± 1.8	%	Using Internal R_{FB} Digital Inputs = V_{INH}
J								
K								
Power Supply Rejection Ratio	PSRR			± 200		± 300	ppm/%	$ \Delta \text{Gain}/\Delta V_{DD} \Delta V_{DD} = \pm 5\%$ Digital Inputs = V_{INH}
J								
K								
Output Leakage Current (Pin 1)	I_{OUT1}			$\pm 50\text{nA}$		$\pm 200\text{nA}$	nA	Digital Inputs = V_{INL}
J								
K								
Output Leakage Current (Pin 2)	I_{OUT2}			$\pm 50\text{nA}$		$\pm 200\text{nA}$	nA	Digital Inputs = V_{INH}
J								
K								
REFERENCE INPUT								
Input Resistance	R_{IN}	5		20	5	20	k Ω	$V_{OUT1} = V_{OUT2} = 0\text{ V}$
DIGITAL INPUTS								
Logical “1” Voltage	V_{IH}	14.5			14.5		V	
Logical “0” Voltage	V_{IL}			0.5		0.5	V	
Input Leakage Current	I_{LKG}			± 1		± 1	μA	
ANALOG OUTPUTS								
Output Capacitance ²								
	C_{OUT1}			100		100	pF	DAC Inputs all 1's
	C_{OUT1}			30		30	pF	DAC Inputs all 0's
	C_{OUT2}			30		30	pF	DAC Inputs all 1's
	C_{OUT2}			100		100	pF	DAC Inputs all 0's

ELECTRICAL CHARACTERISTICS (CON'T)

Parameter	Symbol	Min	25°C Typ	Max	Tmin to Tmax Min Max	Units	Test Conditions/Comments
POWER SUPPLY							
Functional Voltage Range ²	V _{DD}	5		16	5 16	V	All digital inputs = 0 V or all = 15 V
Supply Current	I _{DD}			1.6		mA	

NOTES:

- ¹ Full Scale Range (FSR) is 10V.
- ² Guaranteed but not production tested.
- ³ Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- ⁴ Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2}

V _{DD} to GND	 +17 V	Storage Temperature	 -65°C to +150°C
Digital Input Voltage to GND	GND -0.5 to V _{DD} +0.5 V	Lead Temperature (Soldering, 10 seconds)	. +300°C
I _{OUT1} , I _{OUT2} to GND	 -0.5 to 6.5 V	Package Power Dissipation Rating to 75°C	
V _{REF} to GND	 ±25 V	CDIP, PDIP, SOIC	 800mW
V _{RFB} to GND	 ±25 V	Derates above 75°C	 11mW/°C

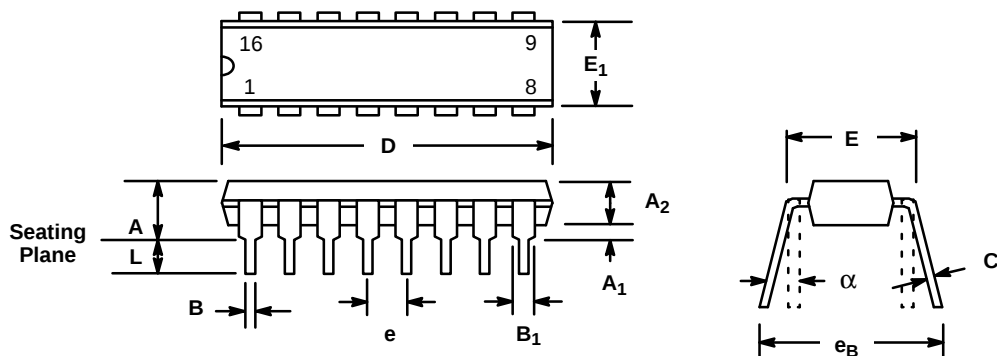
NOTES:

- ¹ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- ² Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES

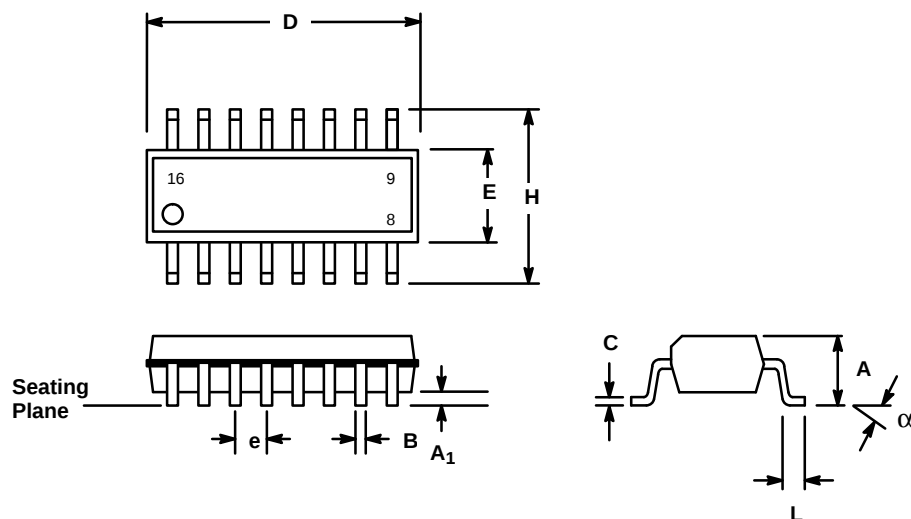
Refer to Section 8 in the 1995 Data Acquisition Products databook for Applications Information

**16 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)**



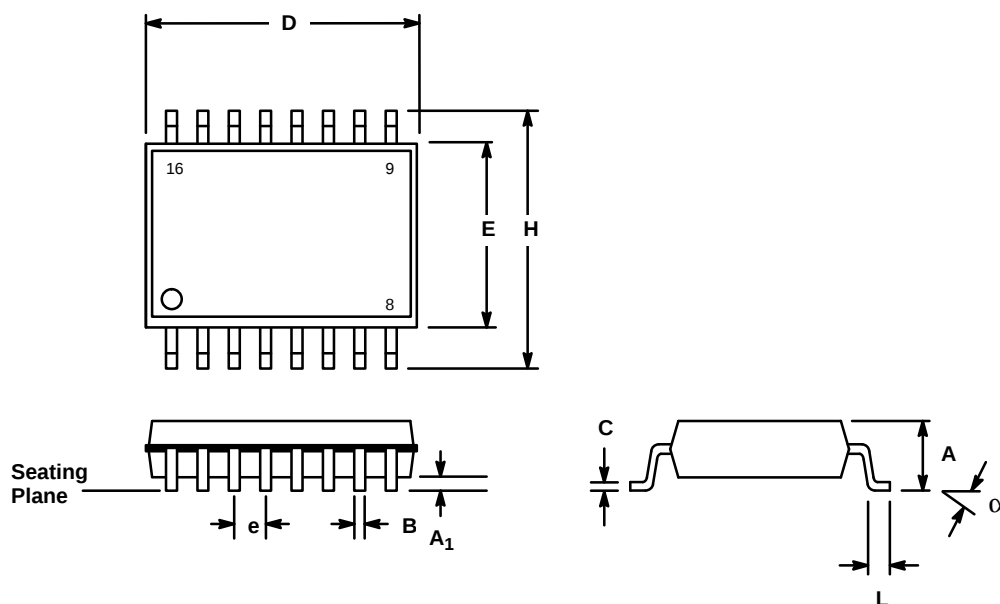
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A ₁	0.015	0.070	0.38	1.78
A ₂	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B ₁	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E ₁	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e _B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

16 LEAD SMALL OUTLINE (150 MIL JEDEC SOIC)



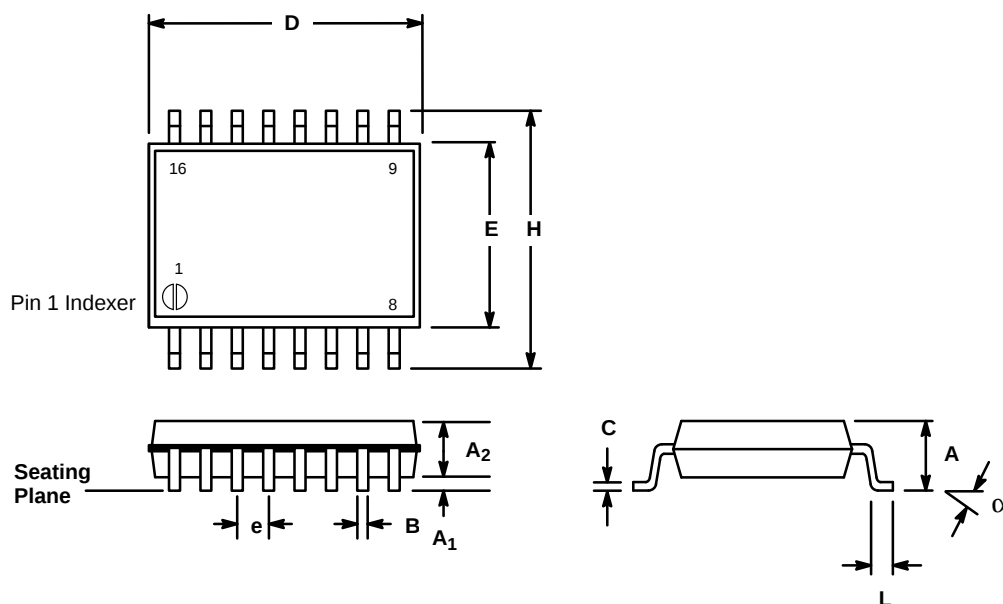
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A ₁	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

**16 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)**



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A ₁	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

16 LEAD EIAJ SMALL OUTLINE (5.5 mm EIAJ SOP)



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.80	2.40	0.071	0.095
A ₁	0.02	0.20	0.001	0.008
A ₂	1.80	2.20	0.079	0.087
B	0.30	0.50	0.012	0.020
C	0.13	0.20	0.005	0.008
D	9.9	10.5	0.390	0.414
E	5.30	5.70	0.209	0.224
e	1.27 BSC		0.050 BSC	
H	7.80	8.20	0.307	0.323
L	0.30	0.90	0.012	0.035
α	0°	15°	0°	15°

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