

FDP7042L / FDB7042L

N-Channel Logic Level PowerTrench® MOSFET

General Description

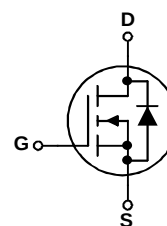
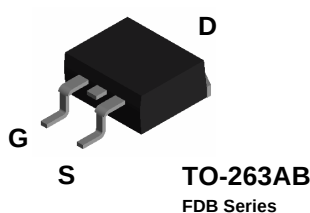
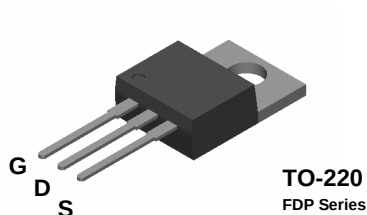
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for "low side" synchronous rectifier operation, providing an extremely low $R_{DS(ON)}$.

Applications

- Synchronous rectifier
- DC/DC converter

Features

- 50 A, 30 V. $R_{DS(ON)} = 9 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
 $R_{DS(ON)} = 7.5 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
- Critical DC electrical parameters specified at elevated temperature
- High performance trench technology for extremely low $R_{DS(ON)}$
- 175°C maximum junction temperature rating



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous (Note 1)	50	A
	– Pulsed (Note 1)	150	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	83	W
	Derate above 25°C	0.48	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-65 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDB7042L	FDB7042L	13"	24mm	800 units
FDP7042L	FDP7042L	Tube	n/a	45

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		24		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 12 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = −12 V V _{DS} = 0 V			−100	nA
On Characteristics (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.8	1.2	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		−4.1		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 4.5 V, I _D = 25A V _{GS} = 10 V, I _D = 25A V _{GS} = 4.5 V, I _D =25A, T _J =125°C		6.2 5.5 9.6	9 7.5 16	mΩ
I _{D(on)}	On–State Drain Current	V _{GS} = 4.5 V, V _{DS} = 10 V	60			A
g _{FS}	Forward Transconductance	V _{DS} = 5V, I _D = 25 A		117		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz		2418		pF
C _{oss}	Output Capacitance			549		pF
C _{rss}	Reverse Transfer Capacitance			243		pF
Switching Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	V _{DD} = 15 V, I _D = 1 A, V _{GS} = 4.5 V, R _{GEN} = 6 Ω		21	34	ns
t _r	Turn–On Rise Time			20	32	ns
t _{d(off)}	Turn–Off Delay Time			60	96	ns
t _f	Turn–Off Fall Time			30	48	ns
Q _g	Total Gate Charge	V _{DS} = 15 V, I _D = 50 A, V _{GS} = 4.5 V		32	51	nC
Q _{gs}	Gate–Source Charge			10		nC
Q _{gd}	Gate–Drain Charge			9		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain–Source Diode Forward Current				50	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 25 A (Note 2)		0.8	1.3	V

Notes:

- Maximum continuous current is limited by the package.
- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

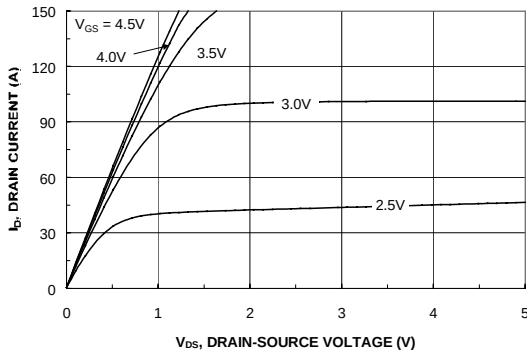


Figure 1. On-Region Characteristics.

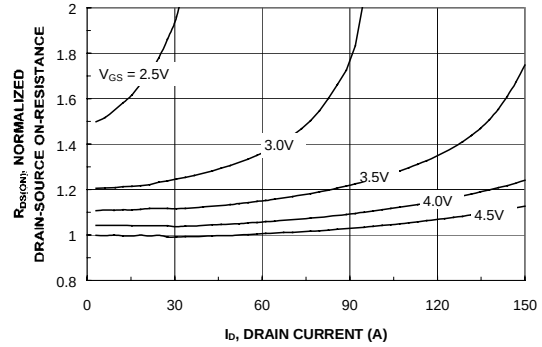


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

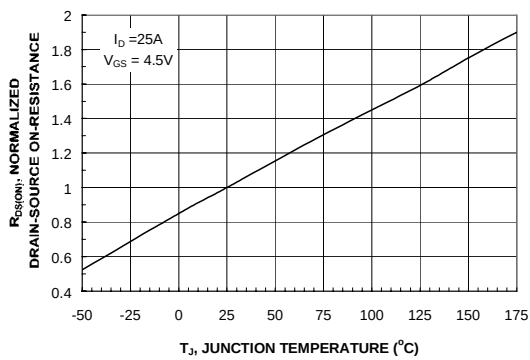


Figure 3. On-Resistance Variation with Temperature.

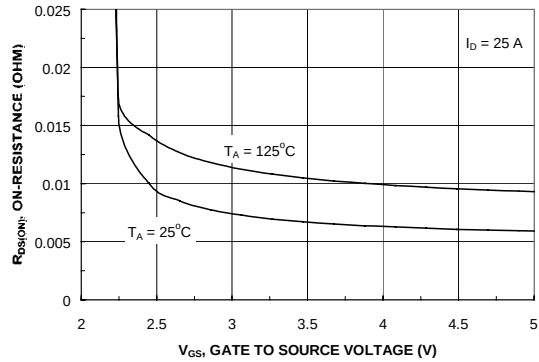


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

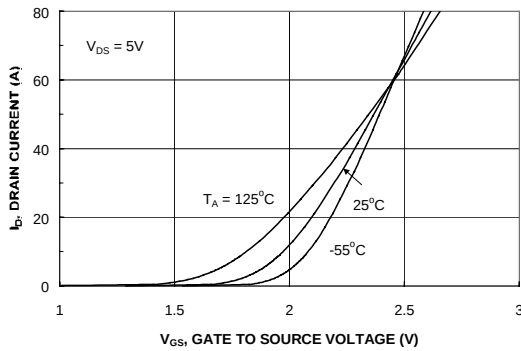


Figure 5. Transfer Characteristics.

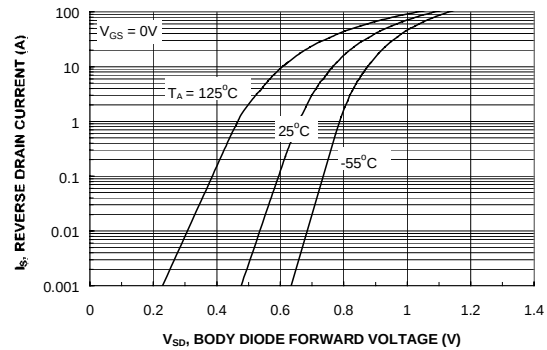


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

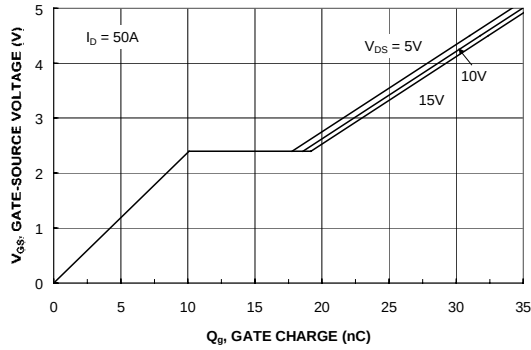


Figure 7. Gate Charge Characteristics.

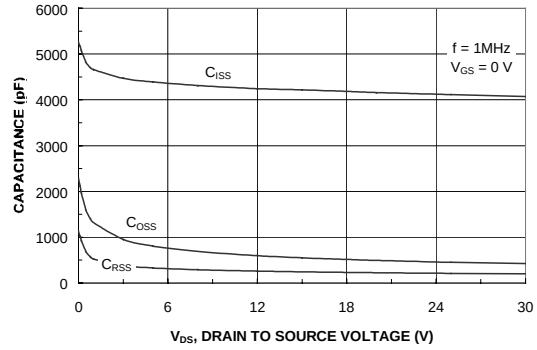


Figure 8. Capacitance Characteristics.

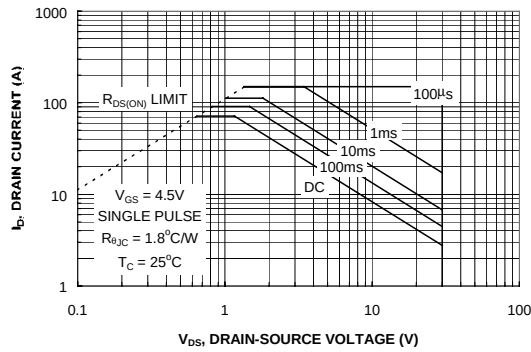


Figure 9. Maximum Safe Operating Area.

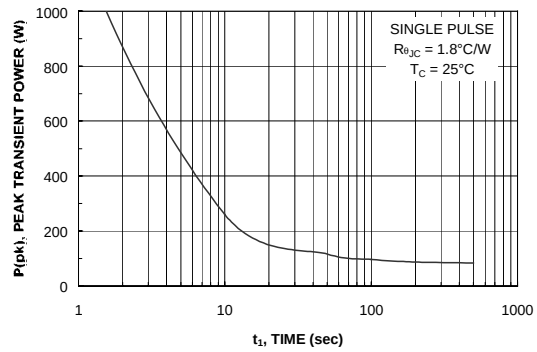


Figure 10. Single Pulse Maximum Power Dissipation.

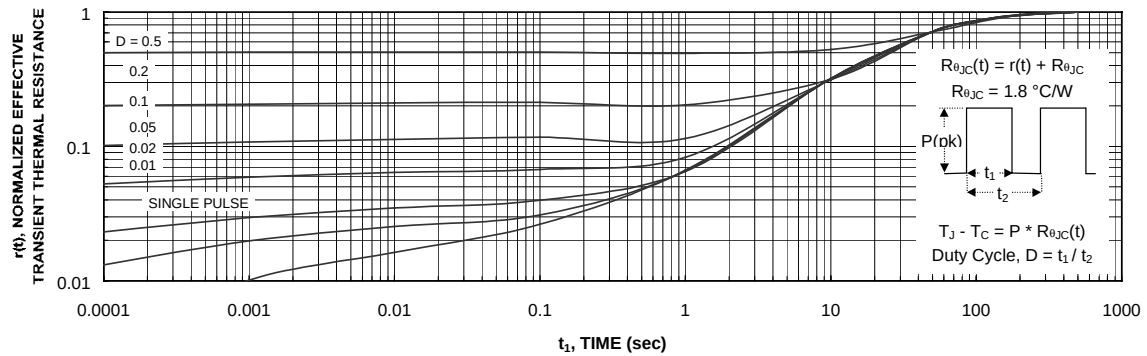


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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