

FDP8896

N-Channel PowerTrench® MOSFET 30V, 92A, 5.9mΩ

General Description

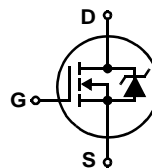
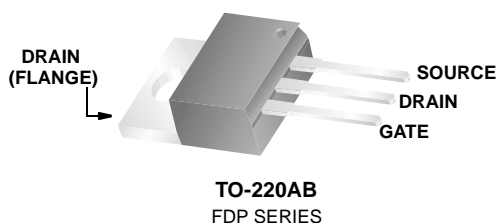
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(ON)}$ and fast switching speed.

Features

- $r_{DS(ON)} = 5.9m\Omega$, $V_{GS} = 10V$, $I_D = 35A$
- $r_{DS(ON)} = 7.0m\Omega$, $V_{GS} = 4.5V$, $I_D = 35A$
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability

Applications

- DC/DC converters



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|----------------|--|------------|---------------|
| V_{DSS} | Drain to Source Voltage | 30 | V |
| V_{GS} | Gate to Source Voltage | ± 20 | V |
| I_D | Drain Current | | |
| | Continuous ($T_C = 25^\circ C$, $V_{GS} = 10V$) (Note 1) | 92 | A |
| | Continuous ($T_C = 25^\circ C$, $V_{GS} = 4.5V$) (Note 1) | 85 | A |
| | Continuous ($T_{amb} = 25^\circ C$, $V_{GS} = 10V$, with $R_{\theta JA} = 62^\circ C/W$) | 16 | A |
| | Pulsed | Figure 4 | A |
| E_{AS} | Single Pulse Avalanche Energy (Note 2) | 74 | mJ |
| P_D | Power dissipation | 80 | W |
| | Derate above $25^\circ C$ | 0.53 | W/ $^\circ C$ |
| T_J, T_{STG} | Operating and Storage Temperature | -55 to 175 | $^\circ C$ |

Thermal Characteristics

| | | | |
|-----------------|---|------|--------------|
| $R_{\theta JC}$ | Thermal Resistance Junction to Case TO-220 | 1.88 | $^\circ C/W$ |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient TO-220 (Note 3) | 62 | $^\circ C/W$ |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|---------------------|----------|-----------|------------|----------|
| FDP8896 | FDP8896 | TO-220AB | Tube | N/A | 50 units |
| FDP8896 | FDP8896_NL (Note 4) | TO-220AB | Tube | N/A | 50 units |

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|------------|-----------------------------------|---|----|---|-----------|---------------|
| B_{VDSS} | Drain to Source Breakdown Voltage | $I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ | 30 | - | - | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$ | - | - | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 20\text{V}$ | - | - | ± 100 | nA |

On Characteristics

| | | | | | | |
|--------------|----------------------------------|---|-----|--------|--------|----------|
| $V_{GS(TH)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ | 1.2 | - | 2.5 | V |
| $r_{DS(ON)}$ | Drain to Source On Resistance | $I_D = 35\text{A}$, $V_{GS} = 10\text{V}$ | - | 0.0050 | 0.0059 | Ω |
| | | $I_D = 35\text{A}$, $V_{GS} = 4.5\text{V}$ | - | 0.0060 | 0.0070 | |
| | | $I_D = 35\text{A}$, $V_{GS} = 10\text{V}$, $T_J = 175^\circ\text{C}$ | - | 0.0078 | 0.0094 | |

Dynamic Characteristics

| | | | | | | | |
|--------------|----------------------------------|---|---|------|-----|----------|----|
| C_{ISS} | Input Capacitance | $V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ | - | 2525 | - | pF | |
| C_{OSS} | Output Capacitance | | - | 490 | - | pF | |
| C_{RSS} | Reverse Transfer Capacitance | | - | 300 | - | pF | |
| R_G | Gate Resistance | $V_{GS} = 0.5\text{V}$, $f = 1\text{MHz}$ | - | 2.3 | - | Ω | |
| $Q_{g(TOT)}$ | Total Gate Charge at 10V | $V_{GS} = 0\text{V}$ to 10V | $V_{DD} = 15\text{V}$ $I_D = 35\text{A}$ $I_g = 1.0\text{mA}$ | - | 48 | 67 | nC |
| $Q_{g(5)}$ | Total Gate Charge at 5V | $V_{GS} = 0\text{V}$ to 5V | | - | 25 | 36 | nC |
| $Q_{g(TH)}$ | Threshold Gate Charge | $V_{GS} = 0\text{V}$ to 1V | | - | 2.3 | 3.0 | nC |
| Q_{gs} | Gate to Source Gate Charge | | | - | 8 | - | nC |
| Q_{gs2} | Gate Charge Threshold to Plateau | | | - | 5.7 | - | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | | - | 9.5 | - | nC |

Switching Characteristics ($V_{GS} = 10\text{V}$)

| | | | | | | |
|--------------|---------------------|---|---|-----|-----|----|
| t_{ON} | Turn-On Time | $V_{DD} = 15\text{V}$, $I_D = 35\text{A}$ $V_{GS} = 4.5\text{V}$, $R_{GS} = 6.2\Omega$ | - | - | 168 | ns |
| $t_{d(ON)}$ | Turn-On Delay Time | | - | 9 | - | ns |
| t_r | Rise Time | | - | 103 | - | ns |
| $t_{d(OFF)}$ | Turn-Off Delay Time | | - | 56 | - | ns |
| t_f | Fall Time | | - | 44 | - | ns |
| t_{OFF} | Turn-Off Time | | - | - | 150 | ns |

Drain-Source Diode Characteristics

| | | | | | | |
|----------|-------------------------------|--|---|---|------|----|
| V_{SD} | Source to Drain Diode Voltage | $I_{SD} = 35\text{A}$ | - | - | 1.25 | V |
| | | $I_{SD} = 20\text{A}$ | - | - | 1.0 | V |
| t_{rr} | Reverse Recovery Time | $I_{SD} = 35\text{A}$, $di_{SD}/dt = 100\text{A}/\mu\text{s}$ | - | - | 27 | ns |
| Q_{RR} | Reverse Recovered Charge | $I_{SD} = 35\text{A}$, $di_{SD}/dt = 100\text{A}/\mu\text{s}$ | - | - | 12 | nC |

Notes:

- 1: Package current limitation is 80A.
- 2: Starting $T_J = 25^\circ\text{C}$, $L = 36\mu\text{H}$, $I_{AS} = 64\text{A}$, $V_{DD} = 27\text{V}$, $V_{GS} = 10\text{V}$.
- 3: Pulse width = 100s.
- 4: FDP8896_NL is lead free product. FDP8896_NL marking will appear on the reel label.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

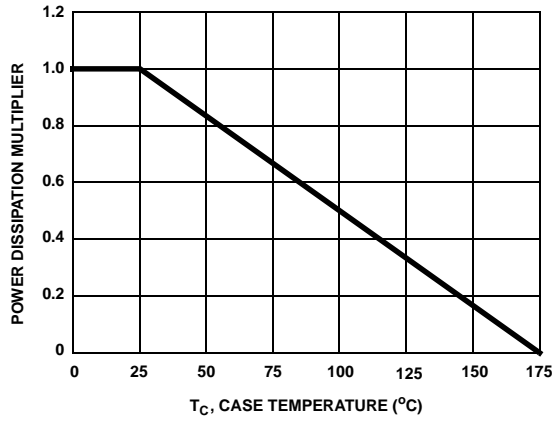


Figure 1. Normalized Power Dissipation vs Case Temperature

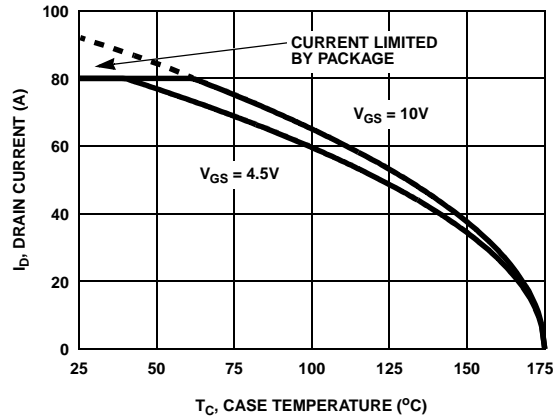


Figure 2. Maximum Continuous Drain Current vs Case Temperature

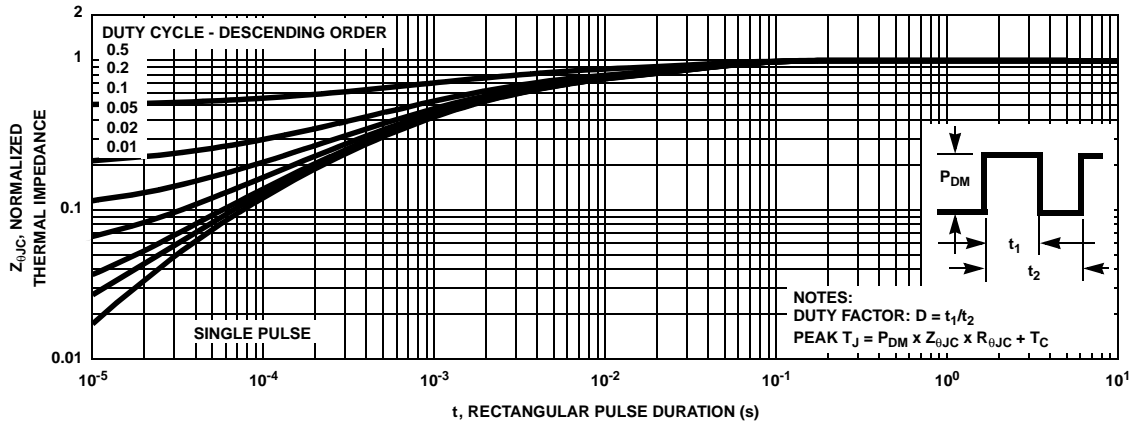


Figure 3. Normalized Maximum Transient Thermal Impedance

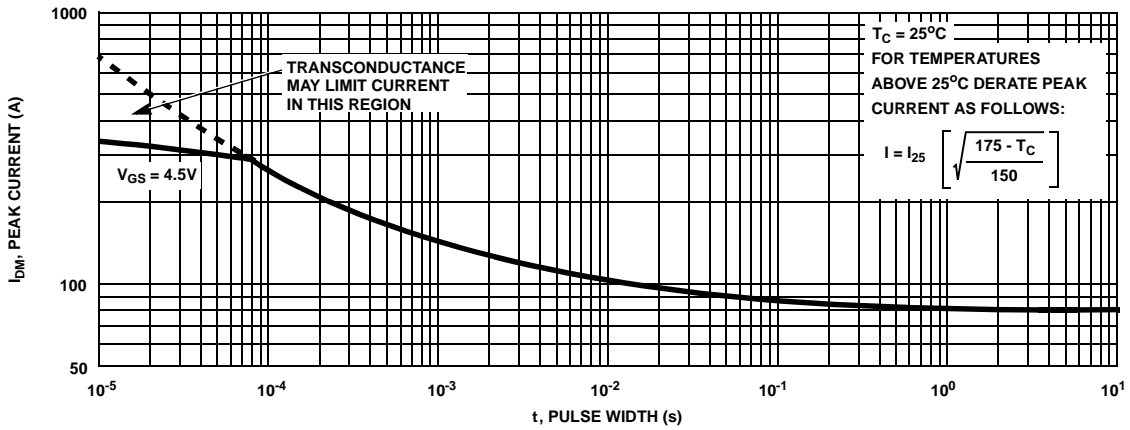


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

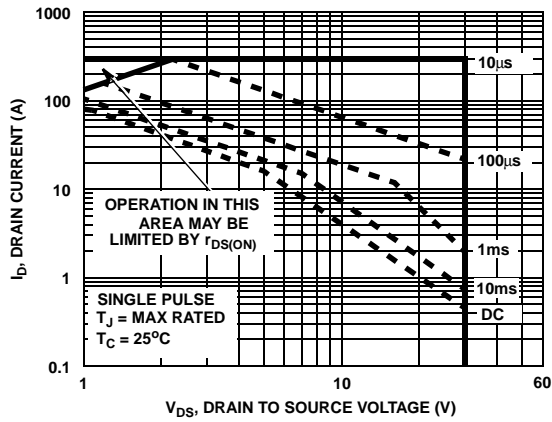


Figure 5. Forward Bias Safe Operating Area

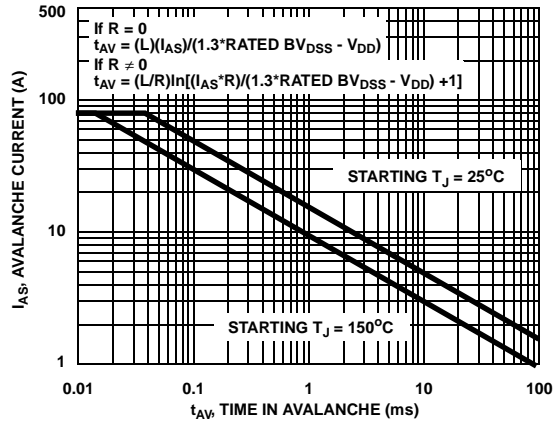


Figure 6. Unclamped Inductive Switching Capability
 NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

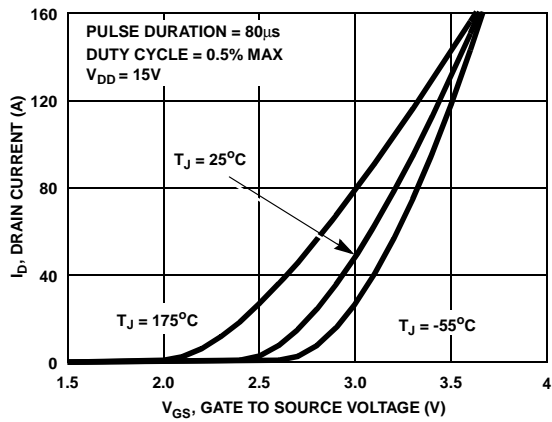


Figure 7. Transfer Characteristics

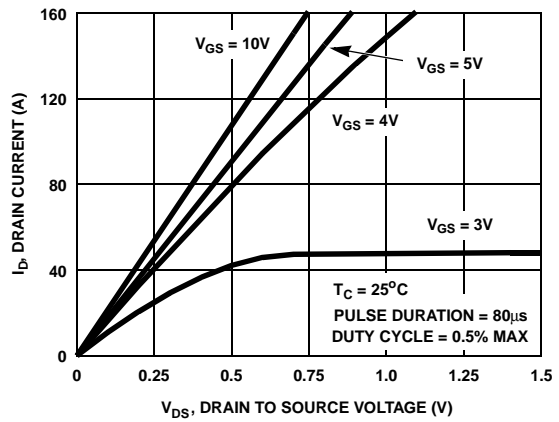


Figure 8. Saturation Characteristics

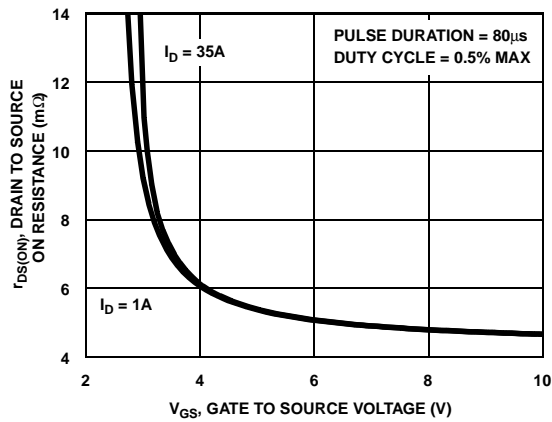


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

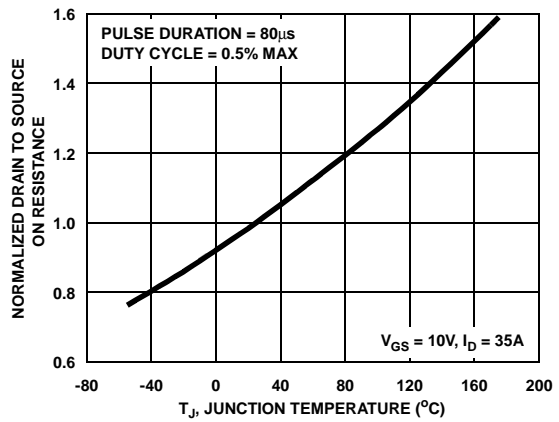


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

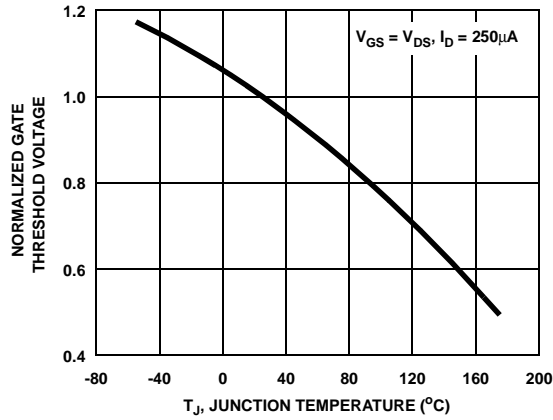


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

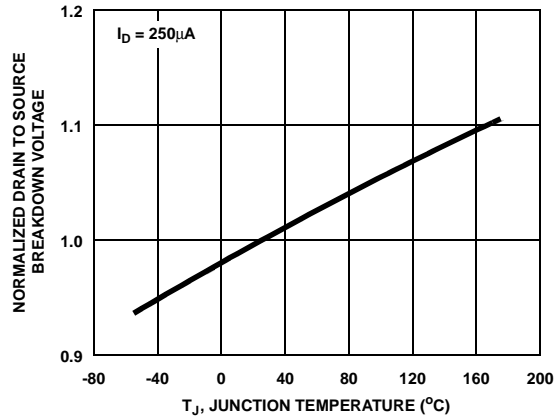


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

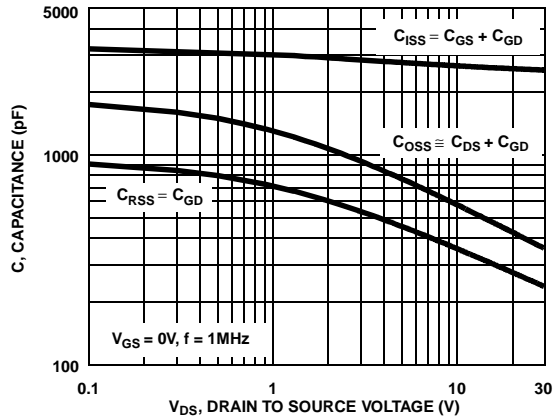


Figure 13. Capacitance vs Drain to Source Voltage

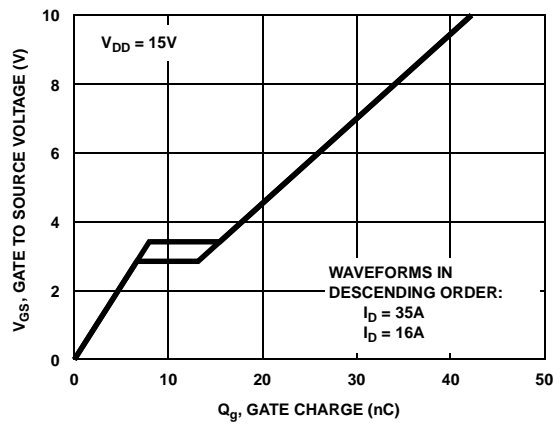


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

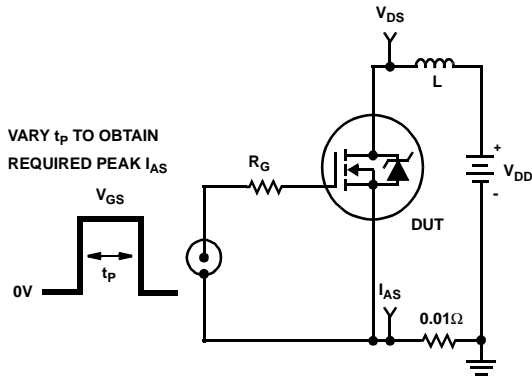


Figure 15. Unclamped Energy Test Circuit

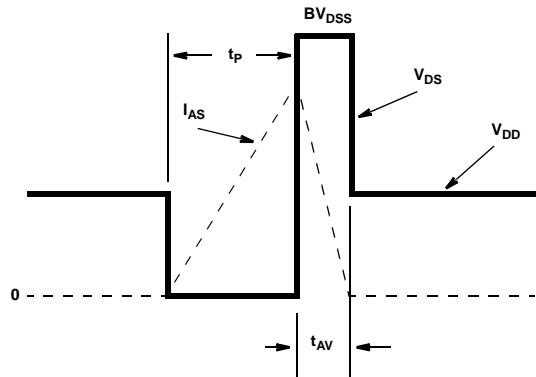


Figure 16. Unclamped Energy Waveforms

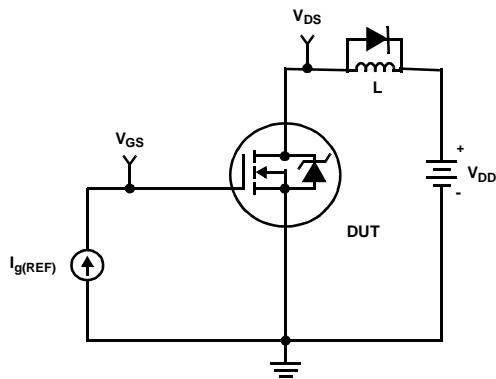


Figure 17. Gate Charge Test Circuit

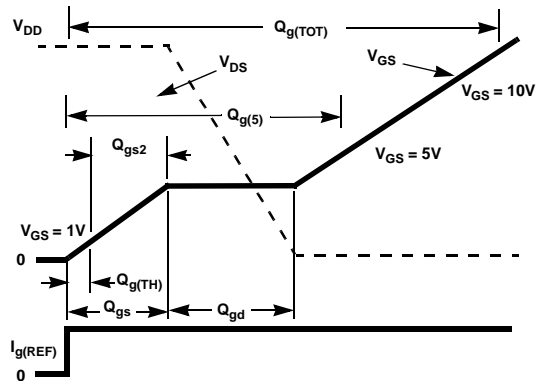


Figure 18. Gate Charge Waveforms

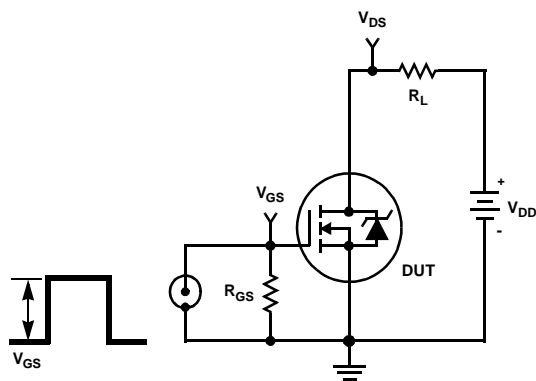


Figure 19. Switching Time Test Circuit

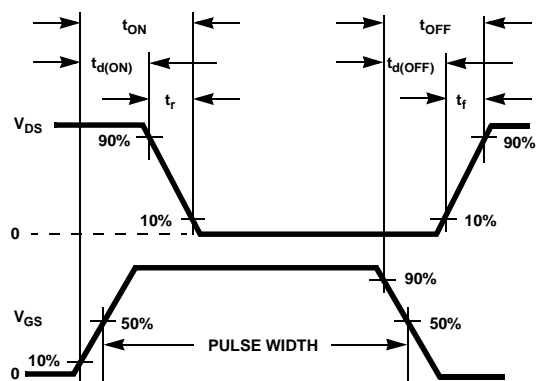


Figure 20. Switching Time Waveforms

PSPICE Electrical Model

.SUBCKT FDP8896 2 1 3 ; rev November 2003

Ca 12 8 2.3e-9
 Cb 15 14 2.3e-9
 Cin 6 8 2.3e-9

Dbody 7 5 DbodyMOD
 Dbreak 5 11 DbreakMOD
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 33
 Eds 14 8 5 8 1
 Egs 13 8 6 8 1
 Esg 6 10 6 8 1
 Evthres 6 21 19 8 1
 Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.5e-9
 Ldrain 2 5 1.0e-9
 Lsource 3 7 2.7e-9

RLgate 1 9 55
 RLdrain 2 5 10
 RLsource 3 7 27

Mmed 16 6 8 8 MmedMOD
 Mstro 16 6 8 8 MstroMOD
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
 Rdrain 50 16 RdrainMOD 2.3e-3
 Rgate 9 20 2.3
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 Rsource 8 7 RsourceMOD 2e-3
 Rvthres 22 8 RvthresMOD 1
 Rvtemp 18 19 RvtempMOD 1
 S1a 6 12 13 8 S1AMOD
 S1b 13 12 13 8 S1BMOD
 S2a 6 15 14 13 S2AMOD
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51))/(1e-6*500),10))}}

.MODEL DbodyMOD D (IS=4E-12 IKF=10 N=1.01 RS=2.6e-3 TRS1=8e-4 TRS2=2e-7
 + CJO=8.8e-10 M=0.57 TT=1e-16 XT1=2.2)

.MODEL DbreakMOD D (RS=8e-2 TRS1=1e-3 TRS2=-8.9e-6)

.MODEL DplcapMOD D (CJO=9.4e-10 IS=1e-30 N=10 M=0.4)

.MODEL MmedMOD NMOS (VTO=1.98 KP=10 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.3 T_ABS=25)

.MODEL MstroMOD NMOS (VTO=2.4 KP=350 IS=1e-30 N=10 TOX=1 L=1u W=1u T_ABS=25)

.MODEL MweakMOD NMOS (VTO=1.68 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=23 RS=0.1 T_ABS=25)

.MODEL RbreakMOD RES (TC1=8.3e-4 TC2=-4e-7)

.MODEL RdrainMOD RES (TC1=1e-3 TC2=8e-6)

.MODEL RSLCMOD RES (TC1=9e-4 TC2=1e-6)

.MODEL RsourceMOD RES (TC1=7.5e-3 TC2=1e-6)

.MODEL RvthresMOD RES (TC1=-2.4e-3 TC2=-8.8e-6)

.MODEL RvtempMOD RES (TC1=-2.6e-3 TC2=2e-7)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3)

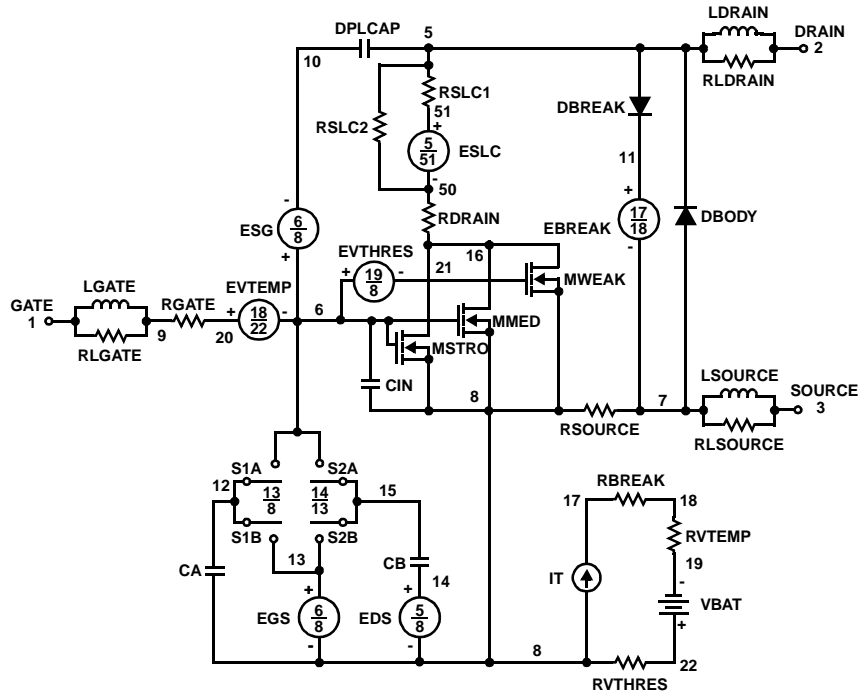
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3 VOFF=-4)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-0.5)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-2)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

rev November 2003

template FDP8896 n2,n1,n3 =m_temp

electrical n2,n1,n3

number m_temp=25

{

var i iscl

dp..model dbodymod = (isl=4e-12,ikf=10,nl=1.01,rs=2.6e-3,trs1=8e-4,trs2=2e-7,cjo=8.8e-10,m=0.57,tt=1e-16,xti=2.2)

dp..model dbreakmod = (rs=8e-2,trs1=1e-3,trs2=-8.9e-6)

dp..model dplcapmod = (cjo=9.4e-10,isl=10e-30,nl=10,m=0.4)

m..model mmedmod = (type=_n,vto=1.98,kp=10,is=1e-30,tox=1)

m..model mstrongmod = (type=_n,vto=2.4,kp=350,is=1e-30,tox=1)

m..model mweakmod = (type=_n,vto=1.68,kp=0.05,is=1e-30,tox=1,rs=0.1)

sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-3,voff=-3)

sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3,voff=-4)

sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2,voff=-0.5)

sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2)

c.ca n12 n8 = 2.3e-9

c.cb n15 n14 = 2.3e-9

c.cin n6 n8 = 2.3e-9

dp.dbody n7 n5 = model=dbodymod

dp.dbreak n5 n11 = model=dbreakmod

dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 33

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evthres n6 n21 n19 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5.5e-9

l.ldrain n2 n5 = 1.0e-9

l.lsource n3 n7 = 2.7e-9

res.rlgate n1 n9 = 55

res.rldrain n2 n5 = 10

res.rlsource n3 n7 = 27

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u, temp=m_temp

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u, temp=m_temp

m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u, temp=m_temp

res.rbreak n17 n18 = 1, tc1=8.3e-4,tc2=-4e-7

res.rdrain n50 n16 = 2.3e-3, tc1=1e-3,tc2=8e-6

res.rgate n9 n20 = 2.3

res.rslc1 n5 n51 = 1e-6, tc1=9e-4,tc2=1e-6

res.rslc2 n5 n50 = 1e3

res.rsource n8 n7 = 2e-3, tc1=7.5e-3,tc2=1e-6

res.rvthres n22 n8 = 1, tc1=-2.4e-3,tc2=-8.8e-6

res.rvtemp n18 n19 = 1, tc1=-2.6e-3,tc2=2e-7

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

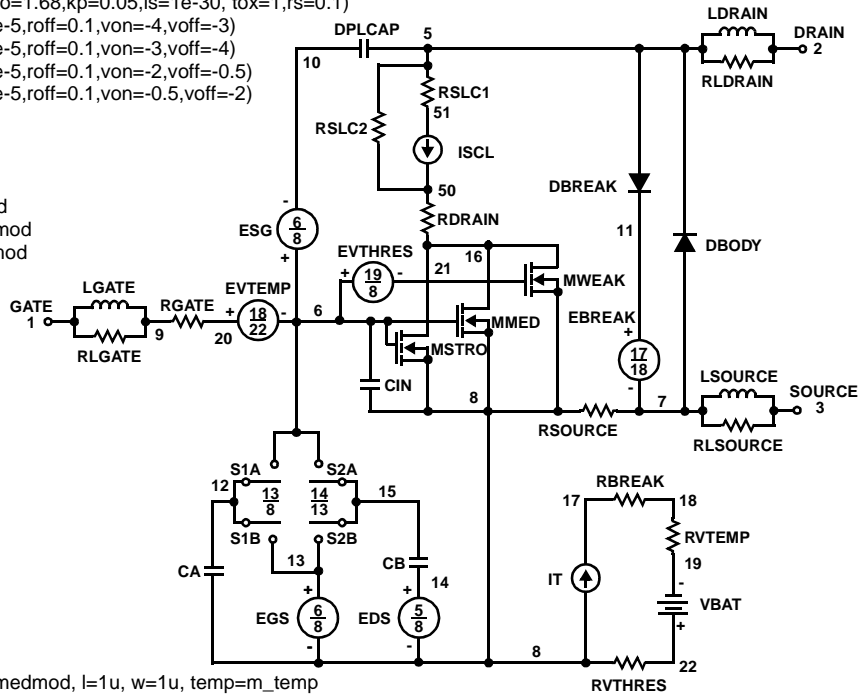
equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/500)** 10))

}

}



PSPICE Thermal Model

REV 23 November 2003

FDP8896T

CTHERM1 TH 6 9e-4
 CHERM2 6 5 1e-3
 CHERM3 5 4 2e-3
 CHERM4 4 3 3e-3
 CHERM5 3 2 7e-3
 CHERM6 2 TL 8e-2

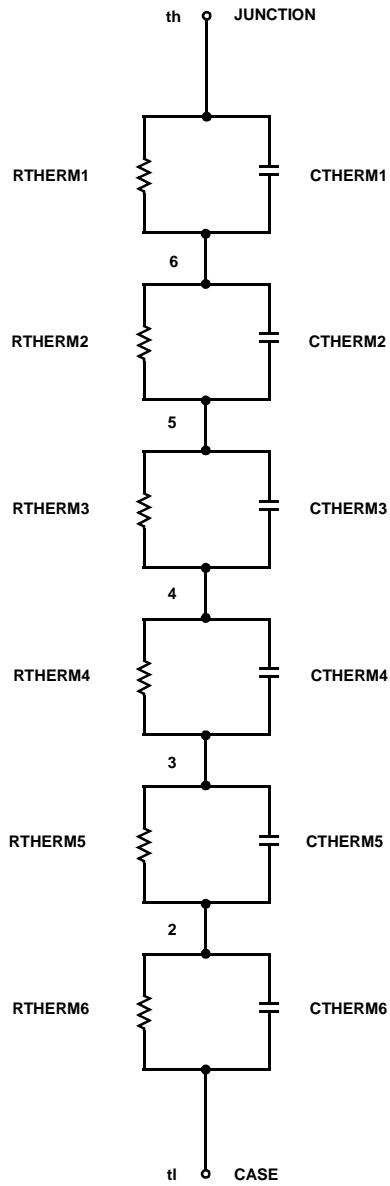
RATHERM1 TH 6 3.0e-2
 RATHERM2 6 5 1.0e-1
 RATHERM3 5 4 1.8e-1
 RATHERM4 4 3 2.8e-1
 RATHERM5 3 2 4.5e-1
 RATHERM6 2 TL 4.6e-1

SABER Thermal Model

SABER thermal model FDP8896T
 template thermal_model th tl
 thermal_c th, tl

```
{
ctherm.ctherm1 th 6 =9e-4
ctherm.ctherm2 6 5 =1e-3
ctherm.ctherm3 5 4 =2e-3
ctherm.ctherm4 4 3 =3e-3
ctherm.ctherm5 3 2 =7e-3
ctherm.ctherm6 2 tl =8e-2
```

```
rtherm.rtherm1 th 6 =3.0e-2
rtherm.rtherm2 6 5 =1.0e-1
rtherm.rtherm3 5 4 =1.8e-1
rtherm.rtherm4 4 3 =2.8e-1
rtherm.rtherm5 3 2 =4.5e-1
rtherm.rtherm6 2 tl =4.6e-1
}
```



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| ActiveArray™ | FASTr™ | LittleFET™ | PowerEdge™ | SuperFET™ |
| Bottomless™ | FPST™ | MICROCOUPLER™ | PowerSaver™ | SuperSOT™-3 |
| CoolFET™ | FRFET™ | MicroFET™ | PowerTrench® | SuperSOT™-6 |
| CROSSVOLT™ | GlobalOptoisolator™ | MicroPak™ | QFET® | SuperSOT™-8 |
| DOMET™ | GTO™ | MICROWIRE™ | QS™ | SyncFET™ |
| EcoSPARK™ | HiSeC™ | MSX™ | QT Optoelectronics™ | TinyLogic® |
| E ² CMOS™ | ꝑC™ | MSXPro™ | Quiet Series™ | TINYOPTO™ |
| EnSigna™ | i-Lo™ | OCX™ | RapidConfigure™ | TruTranslation™ |
| FACT™ | ImpliedDisconnect™ | OCXPro™ | RapidConnect™ | UHC™ |
| FACT Quiet Series™ | | OPTOLOGIC® | µSerDes™ | UltraFET® |
| Across the board. Around the world.™ | | OPTOPLANAR™ | SILENT SWITCHER® | UniFET™ |
| The Power Franchise® | | PACMAN™ | SMART START™ | VCX™ |
| Programmable Active Droop™ | | POP™ | SPM™ | |

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

| Datasheet Identification | Product Status | Definition |
|--------------------------|------------------------|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
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