

FDS6982

Dual N-Channel, Notebook Power Supply MOSFET

General Description

This part is designed to replace two single SO-8 MOSFETs in synchronous DC:DC power supplies that provide the various peripheral voltage rails required in notebook computers and other battery powered electronic devices. FDS6982 contains two unique 30V, N-channel, logic level, PowerTrench® MOSFETs designed to maximize power conversion efficiency.

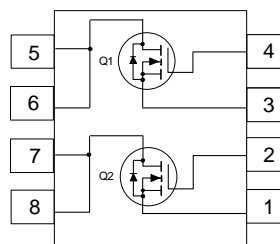
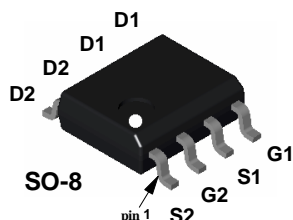
The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized for low conduction losses (less than 20mΩ at $V_{GS} = 4.5V$).

Applications

- Battery powered synchronous DC:DC converters.
- Embedded DC:DC conversion.

Features

- Q2: 8.6A, 30V. $R_{DS(on)} = 0.015 \Omega @ V_{GS} = 10V$
 $R_{DS(on)} = 0.020 \Omega @ V_{GS} = 4.5V$
- Q1: 6.3A, 30V. $R_{DS(on)} = 0.028 \Omega @ V_{GS} = 10V$
 $R_{DS(on)} = 0.035 \Omega @ V_{GS} = 4.5V$
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(on)}$.



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Q2	Q1	Units
V_{DSS}	Drain-Source Voltage	30	30	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Note 1a)	8.6	6.3	A
	- Pulsed	30	20	
P_D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ C$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS6982	FDS6982	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	Q2 Q1	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	Q2 Q1		27 26		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	All			1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	Q2 Q1	1 1	2.2 1.6	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	Q2 Q1		-5 -4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8.6\text{ A}$	Q2		0.012	0.015	Ω
		$V_{GS} = 10\text{ V}, I_D = 8.6\text{ A}, T_J = 125^\circ\text{C}$			0.018	0.024	
		$V_{GS} = 4.5\text{ V}, I_D = 7.5\text{ A}$			0.016	0.020	
		$V_{GS} = 10\text{ V}, I_D = 6.3\text{ A}$	Q1		0.021	0.028	Ω
		$V_{GS} = 10\text{ V}, I_D = 6.3\text{ A}, T_J = 125^\circ\text{C}$			0.038	0.047	
		$V_{GS} = 4.5\text{ V}, I_D = 5.6\text{ A}$			0.028	0.035	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	Q2 Q1	30 20			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 8.6\text{ A}$	Q2		50		S
		$V_{DS} = 5\text{ V}, I_D = 6.3\text{ A}$	Q1		40		

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	Q2 Q1		2085 760		pF
C_{oss}	Output Capacitance		Q2 Q1		420 160		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		160 70		pF

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Switching Characteristics (Note 2)

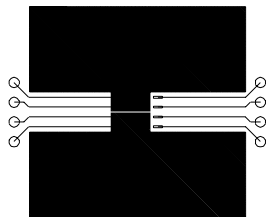
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	Q2		15	27	ns
t_r	Turn-On Rise Time		Q1		10	18	ns
			Q2		11	20	
$t_{d(off)}$	Turn-Off Delay Time		Q1		14	25	ns
		Q2		36	58		
t_f	Turn-Off Fall Time	Q1		21	34	ns	
		Q2		18	29		
Q_g	Total Gate Charge	Q2 $V_{DS} = 15\text{ V}, I_D = 8.6\text{ A}, V_{GS} = 5\text{ V}$	Q2		18.5	26	nC
			Q1		8.5	12	
Q_{gs}	Gate-Source Charge	Q1 $V_{DS} = 15\text{ V}, I_D = 6.3\text{ A}, V_{GS} = 5\text{ V}$	Q2		7.3		nC
			Q1		2.4		
Q_{gd}	Gate-Drain Charge		Q2		6.2		nC
			Q1		3.1		

Drain-Source Diode Characteristics and Maximum Ratings

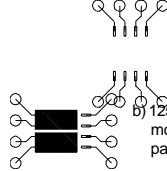
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2			1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	Q2		0.72	1.2	V
			Q1		0.74	1.2	

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. Thermal rating based on independent single device operation.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz. copper.



b) 125°C/W when mounted on a 0.02 in^2 pad of 2 oz. copper.

c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics: Q2

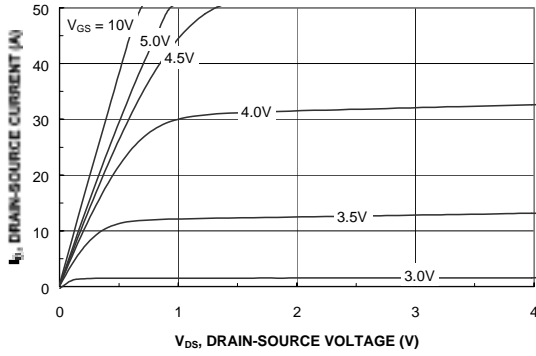


Figure 1. On-Region Characteristics.

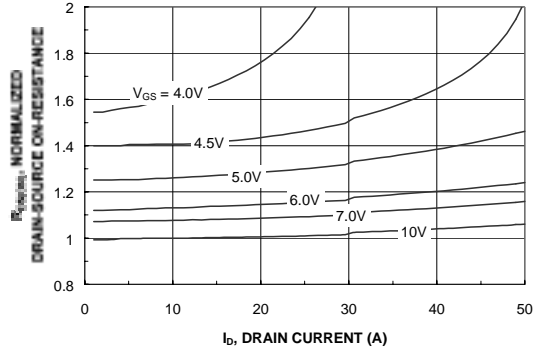


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

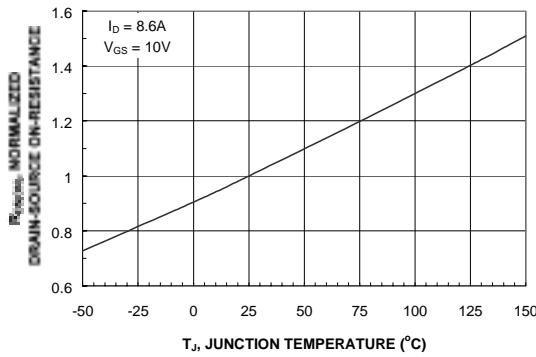


Figure 3. On-Resistance Variation with Temperature.

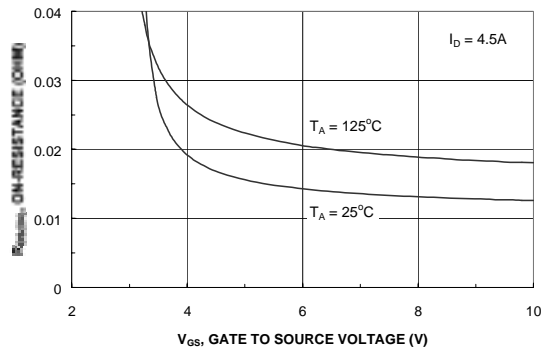


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

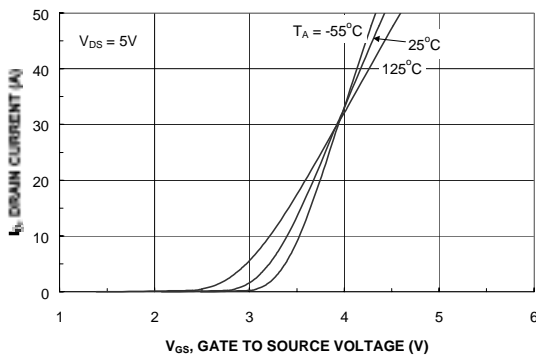


Figure 5. Transfer Characteristics.

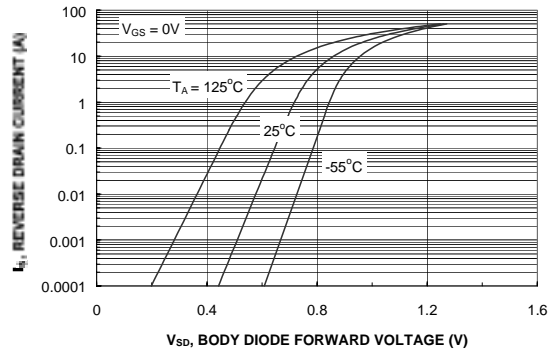


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2 (continued)

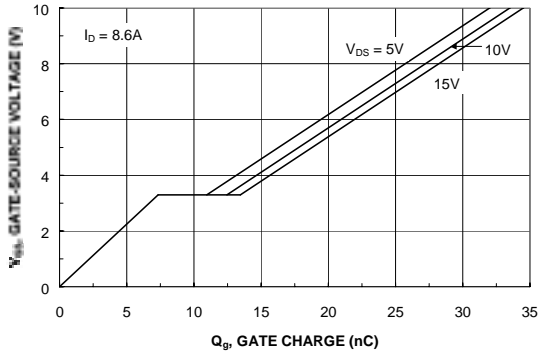


Figure 7. Gate-Charge Characteristics.

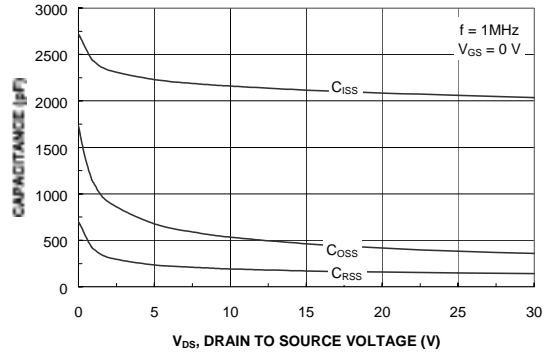


Figure 8. Capacitance Characteristics.

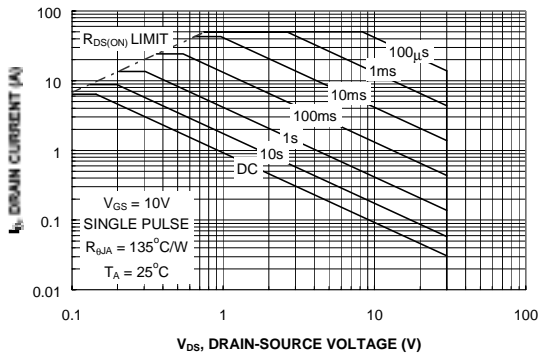


Figure 9. Maximum Safe Operating Area.

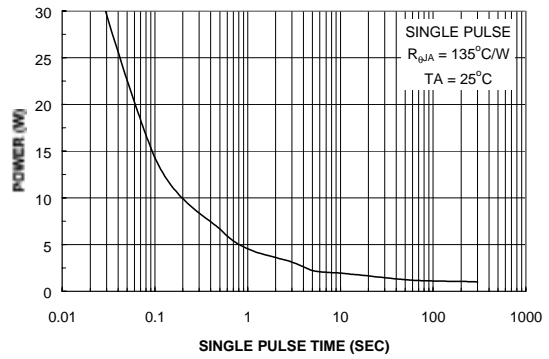


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1

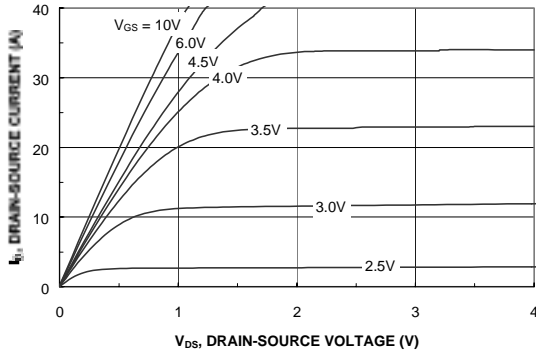


Figure 11. On-Region Characteristics.

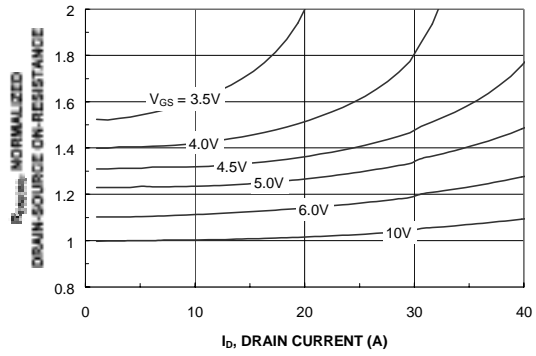


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

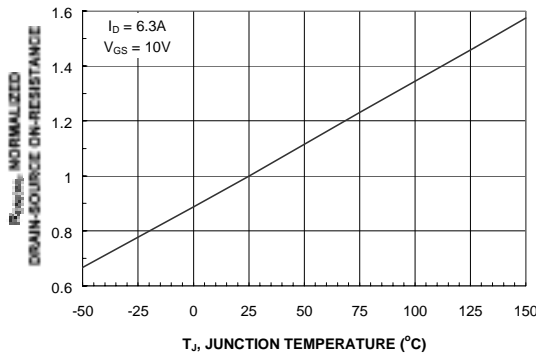


Figure 13. On-Resistance Variation with Temperature.

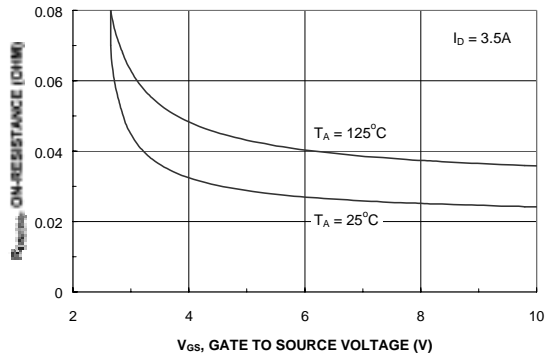


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

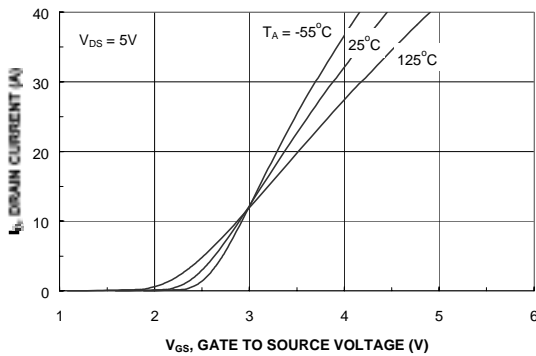


Figure 15. Transfer Characteristics.

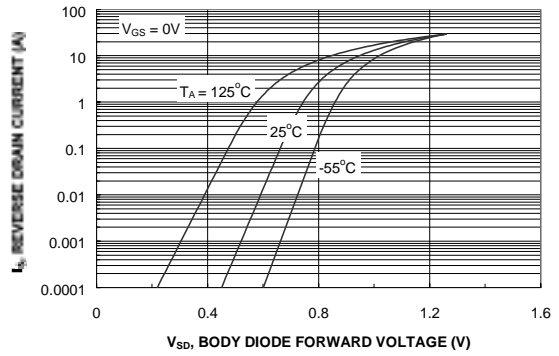


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1 (continued)

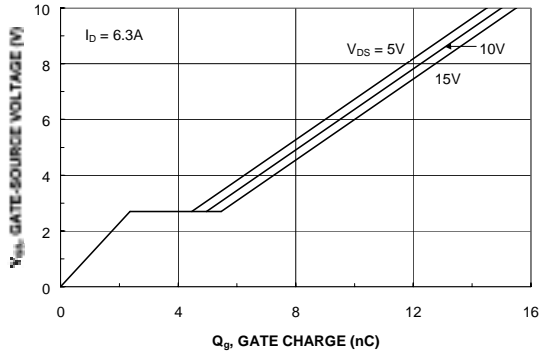


Figure 17. Gate-Charge Characteristics.

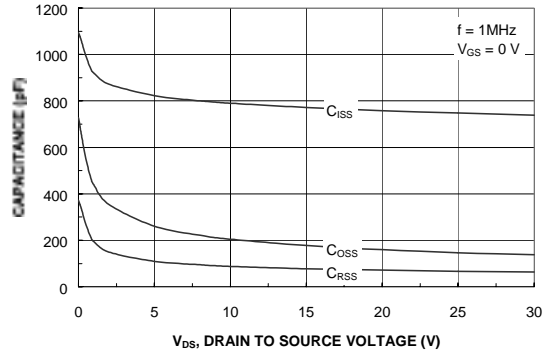


Figure 18. Capacitance Characteristics.

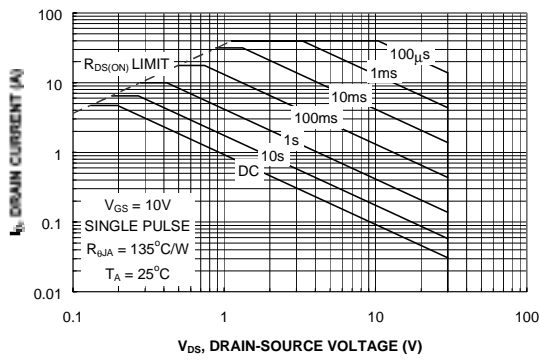


Figure 19. Maximum Safe Operating Area.

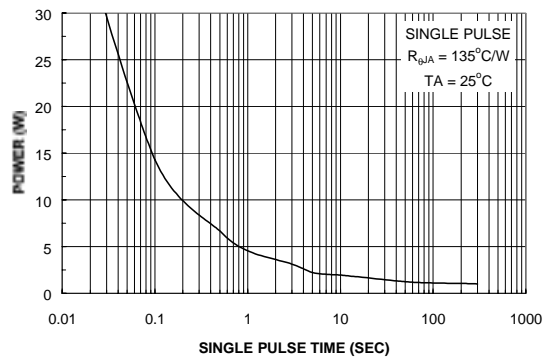


Figure 20. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1 & Q2 (continued)

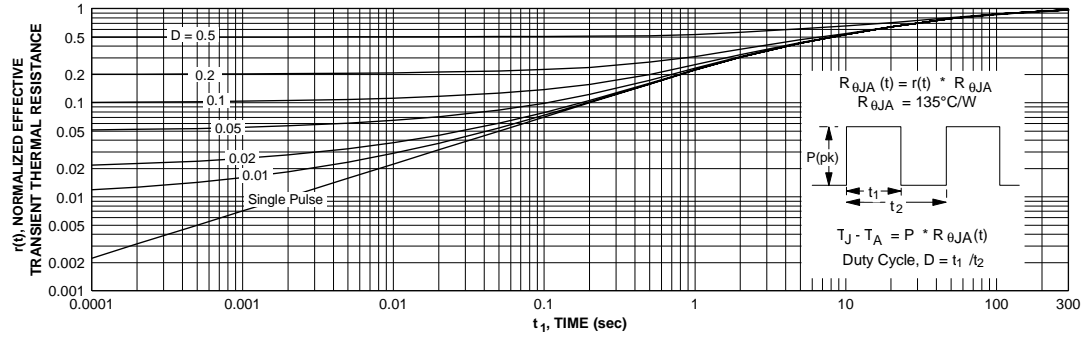


Figure 21. Transient Thermal Response Curve.

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