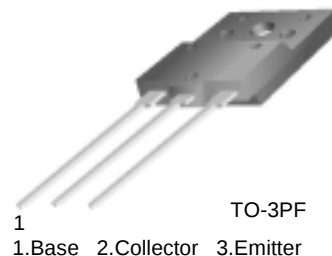


FJAF6815

FJAF6815

High Voltage Color Display Horizontal Deflection Output

- High Collector-Base Breakdown Voltage : $BV_{CBO} = 1500V$
- Low Saturation Voltage : $V_{CE(sat)} = 3V$ (Max.)
- For Color Monitor



NPN Triple Diffused Planar Silicon Transistor

Absolute Maximum Ratings $T_C=25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Rating	Units
V_{CBO}	Collector-Base Voltage	1500	V
V_{CEO}	Collector-Emitter Voltage	750	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector Current (DC)	15	A
I_{CP}^*	Collector Current (Pulse)	25	A
P_C	Collector Dissipation	60	W
T_J	Junction Temperature	150	$^{\circ}C$
T_{STG}	Storage Temperature	-55 ~ 150	$^{\circ}C$

* Pulse Test: $PW=300\mu s$, duty Cycle=2% Pulsed

Electrical Characteristics $T_C=25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CES}	Collector Cut-off Current	$V_{CB}=1400V, R_{BE}=0$			1	mA
I_{CBO}	Collector Cut-off Current	$V_{CB}=800V, I_E=0$			10	μA
I_{EBO}	Emitter Cut-off Current	$V_{EB}=4V, I_C=0$			1	mA
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C=500\mu A, I_E=0$	1500			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C=5mA, I_B=0$	750			V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E=500\mu A, I_C=0$	6			V
h_{FE1} h_{FE2}	DC Current Gain	$V_{CE}=5V, I_C=1A$ $V_{CE}=5V, I_C=10A$	10 5		8	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C=10A, I_B=2.5A$			3	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C=10A, I_B=2.5A$			1.5	V
t_{STG}^*	Storage Time	$V_{CC}=200V, I_C=8A, R_L=25\Omega$			3	μs
t_F^*	Fall Time	$I_{B1}=1.6A, I_{B2}=-3.2A$			0.2	μs

* Pulse Test: $PW=20\mu s$, duty Cycle=1% Pulsed

Thermal Characteristics $T_C=25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.08	$^{\circ}C/W$

Typical Characteristics

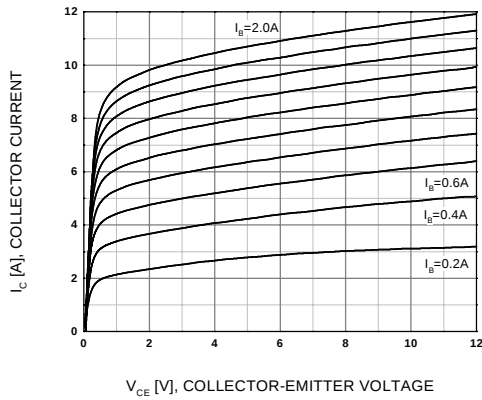


Figure 1. Static Characteristics

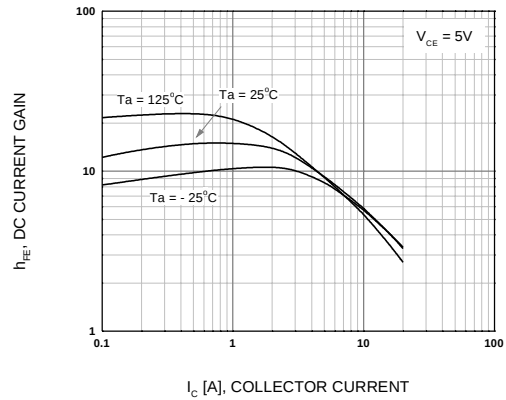


Figure 2. DC Current Gain

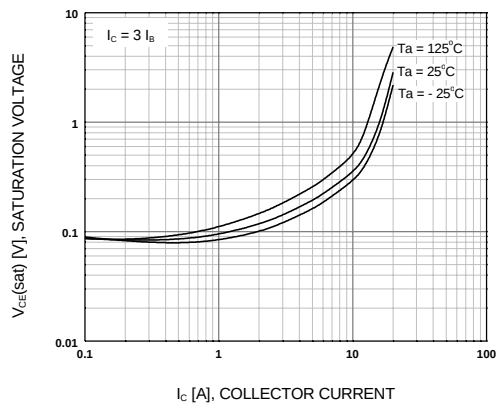


Figure 3. Collector-Emitter Saturation Voltage

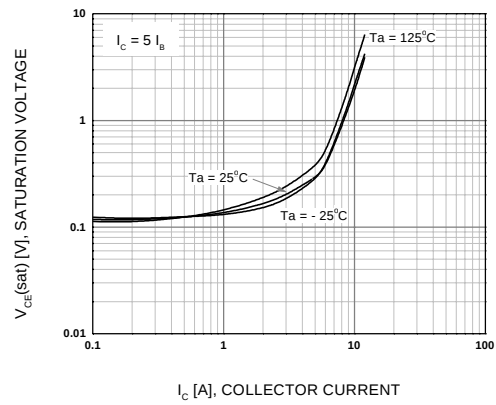


Figure 4. Collector-Emitter Saturation Voltage

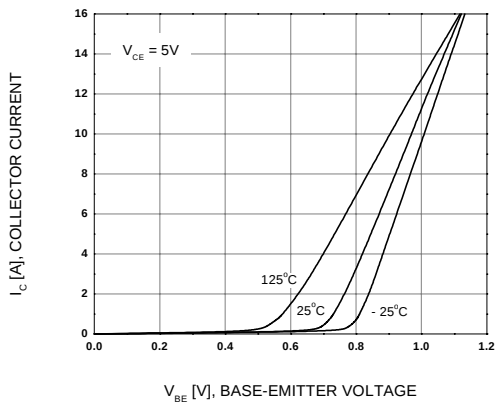


Figure 5. Base-Emitter On Voltage

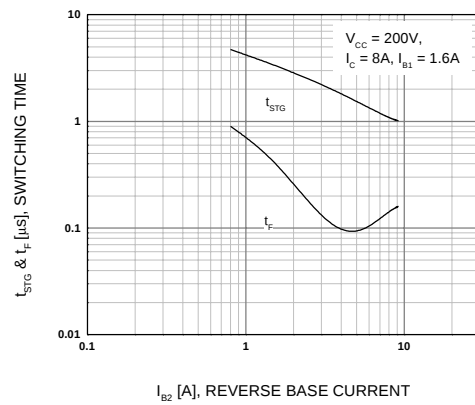


Figure 6. Resistive Load Switching Time

Typical Characteristics (Continued)

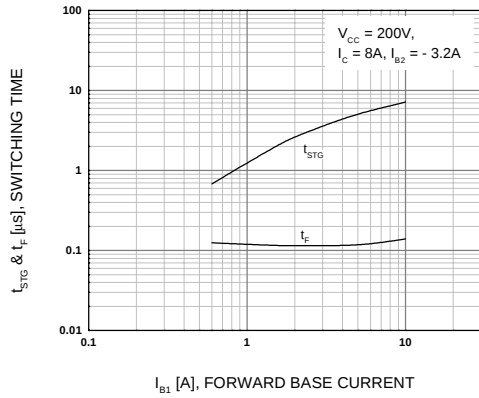


Figure 7. Resistive Load Switching Time

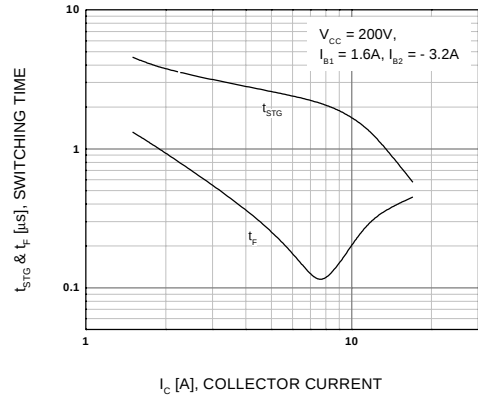


Figure 8. Resistive Load Switching Time

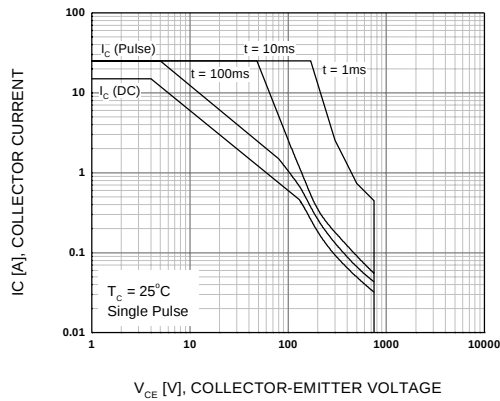


Figure 9. Forward Bias Safe Operating Area

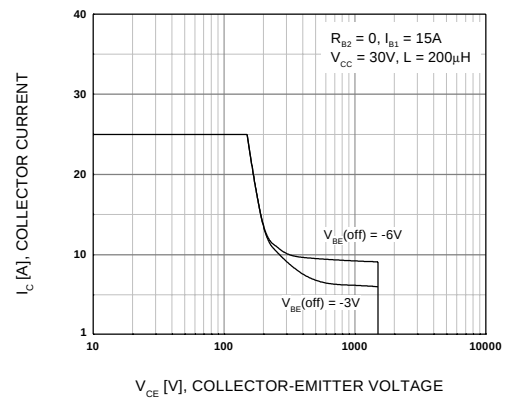


Figure 10. Reverse Bias Safe Operating Area

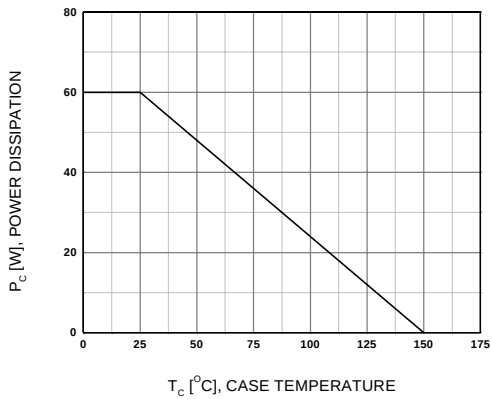


Figure 11. Power Derating

Rev. A, May 2001

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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