#### INTEGRATED CIRCUITS

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# **74HC/HCT245**Octal bus transceiver; 3-state

Product specification
File under Integrated Circuits, IC06

September 1993





74HC/HCT245

#### **FEATURES**

- · Octal bidirectional bus interface
- · Non-inverting 3-state outputs
- · Output capability: bus driver
- I<sub>CC</sub> category: MSI

#### **GENERAL DESCRIPTIONS**

The 74HC/HCT245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The "245" features an output enable  $(\overline{OE})$  input for easy cascading and a send/receive (DIR) for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated. The "245" is similar to the "640" but has true (non-inverting) outputs.

#### **QUICK REFERENCE DATA**

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$ 

SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT		
STWIBOL	PARAMETER	CONDITIONS	нс	нст	ONII	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	7	10	ns	
Cı	input capacitance		3.5	3.5	pF	
C <sub>I</sub> / <sub>O</sub>	input/output capacitance		10	10	pF	
C <sub>PD</sub>	power dissipation capacitance per transceiver	notes 1 and 2	30	30	pF	

#### **Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$ 

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is  $V_1 = GND$  to  $V_{CC}$ 

For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 V$ 

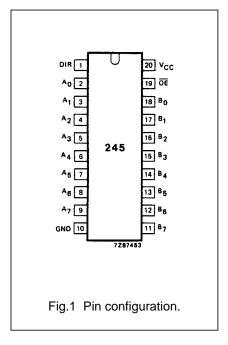
#### **ORDERING INFORMATION**

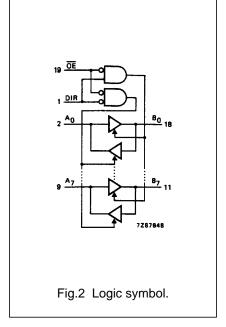
See "74HC/HCT/HCU/HCMOS Logic Package Information".

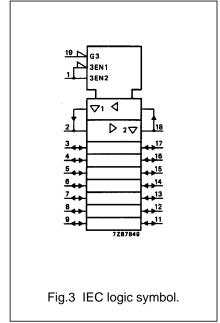
# 74HC/HCT245

#### **PIN DESCRIPTION**

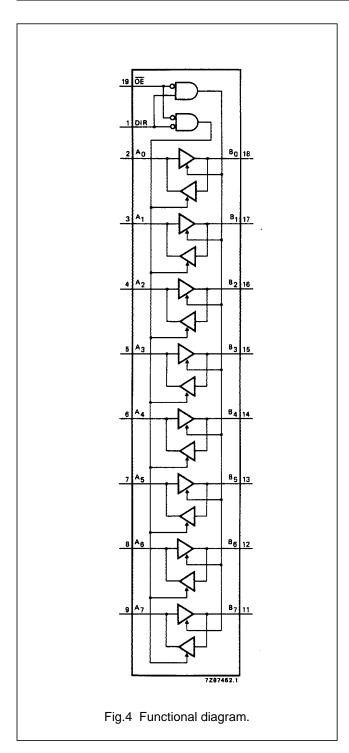
PIN NO.	SYMBOL	NAME AND FUNCTION					
1	DIR	direction control					
2, 3, 4, 5, 6, 7, 8, 9 A <sub>0</sub> to A <sub>7</sub>		data inputs/outputs					
10	GND	ground (0 V)					
18, 17, 16, 15, 14, 13, 12, 11 B <sub>0</sub> to B <sub>7</sub>		data inputs/outputs					
19	ŌĒ	output enable input (active LOW)					
20	V <sub>CC</sub>	positive supply voltage					







# 74HC/HCT245



#### **FUNCTION TABLE**

INP	UTS	INPUTS/OUTPUTS					
ŌĒ	DIR	A <sub>n</sub>	B <sub>n</sub>				
L	L	A = B	inputs B = A				
L	Н	inputs	B = A				
Н	X	Z	Z				

#### **Notes**

- 1. H = HIGH voltage level
  - L = LOW voltage level
  - X = don't care
  - Z = high impedance OFF-state

Philips Semiconductors Product specification

# Octal bus transceiver; 3-state

74HC/HCT245

#### DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

#### **AC CHARACTERISTICS FOR 74HC**

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS	
SYMBOL		74HC									WAVEFORMS
STWIBOL		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	VVAVEI OKIIIS
		min.	typ.	max.	min.	max.	min.	max.		( ' '	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay  A <sub>n</sub> to B <sub>n;</sub> B <sub>n</sub> to A <sub>n</sub>		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time  OE to A <sub>n;</sub> OE to B <sub>n</sub> signalname DIR		30 11 9	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time  OE to A <sub>n;</sub> OE to B <sub>n</sub> signalname DIR		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5

74HC/HCT245

#### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

#### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT						
An	0.40						
B <sub>n</sub>	0.40						
OE	1.50						
DIR	0.90						

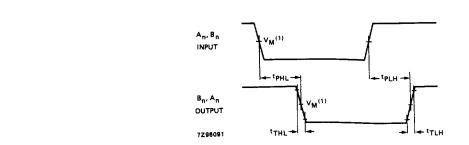
#### **AC CHARACTERISTICS FOR 74HCT**

 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$ 

	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS	
SYMBOL		74HCT									WAVEFORMS
		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	VVAVEI OKIIIS
		min.	typ.	max.	min.	max.	min.	max.		(-)	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay  A <sub>n</sub> to B <sub>n</sub> ;  B <sub>n</sub> to A <sub>n</sub>		12	22		28		33	ns	4.5	Fig.5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time  OE to A <sub>n;</sub> OE to B <sub>n</sub> signalname DIR		16	30		38		45	ns	4.5	Fig.6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time  OE to A <sub>n;</sub> OE to B <sub>n</sub> signalname DIR		16	30		38		45	ns	4.5	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.5

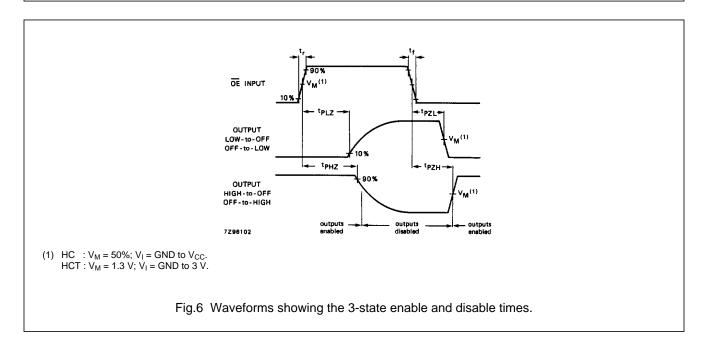
74HC/HCT245

#### **AC WAVEFORMS**



 $\begin{array}{ll} \text{(1)} & \text{HC} & : V_M = 50\%; \ V_I = \text{GND to } V_{CC}. \\ & \text{HCT} : V_M = 1.3 \ V; \ V_I = \text{GND to 3 } V. \end{array}$ 

Fig.5 Waveforms showing the input  $(A_n, B_n)$  to output  $(B_n, A_n)$  propagation delays and the output transition times.



#### **PACKAGE OUTLINES**

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".