

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT194**

4-bit bidirectional universal shift register

Product specification  
File under Integrated Circuits, IC06

December 1990

## 4-bit bidirectional universal shift register

## 74HC/HCT194

## FEATURES

- Shift-left and shift-right capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous master reset
- Hold ("do nothing") mode
- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT194 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The functional characteristics of the 74HC/HCT194 4-bit bidirectional universal shift registers are indicated in the logic diagram and function table. The registers are fully synchronous.

The "194" design has special features which increase the range of application. The synchronous operation of the device is determined by the mode select inputs ( $S_0$ ,  $S_1$ ). As shown in the mode select table, data can be entered

and shifted from left to right ( $Q_0 \rightarrow Q_1 \rightarrow Q_2$ , etc.) or, right to left ( $Q_3 \rightarrow Q_2 \rightarrow Q_1$ , etc.) or parallel data can be entered, loading all 4 bits of the register simultaneously. When both  $S_0$  and  $S_1$  are LOW, existing data is retained in a hold ("do nothing") mode. The first and last stages provide D-type serial data inputs ( $D_{SR}$ ,  $D_{SL}$ ) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode select and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The four parallel data inputs ( $D_0$  to  $D_3$ ) are D-type inputs. Data appearing on the  $D_0$  to  $D_3$  inputs, when  $S_0$  and  $S_1$  are HIGH, is transferred to the  $Q_0$  to  $Q_3$  outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset ( $\overline{MR}$ ) overrides all other input conditions and forces the Q outputs LOW.

The "194" is similar in operation to the "195" universal shift register, with added features of shift-left without external connections and hold ("do nothing") modes of operation.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL              | PARAMETER                                 | CONDITIONS                                   | TYPICAL |     | UNIT |
|---------------------|-------------------------------------------|----------------------------------------------|---------|-----|------|
|                     |                                           |                                              | HC      | HCT |      |
| $t_{PHL} / t_{PLH}$ | propagation delay<br>CP to $Q_n$          | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 14      | 15  | ns   |
| $t_{PHL}$           | $\overline{MR}$ to $Q_n$                  |                                              | 11      | 15  | ns   |
| $f_{max}$           | maximum clock frequency                   |                                              | 102     | 77  | MHz  |
| $C_I$               | input capacitance                         |                                              | 3.5     | 3.5 | pF   |
| $C_{PD}$            | power dissipation capacitance per package | notes 1 and 2                                | 40      | 40  | pF   |

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum = (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_i = \text{GND to } V_{CC}$ ; for HCT the condition is  $V_i = \text{GND to } V_{CC} - 1.5\text{ V}$

4-bit bidirectional universal shift register

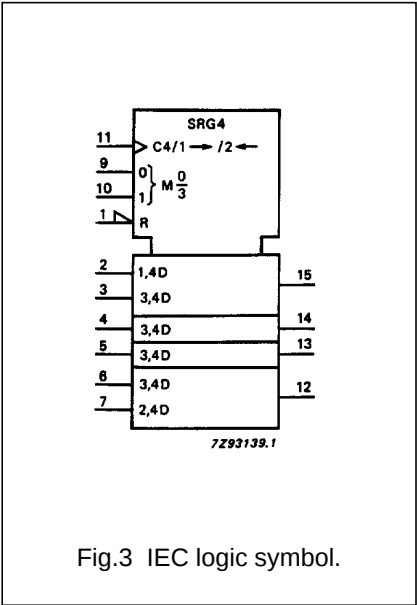
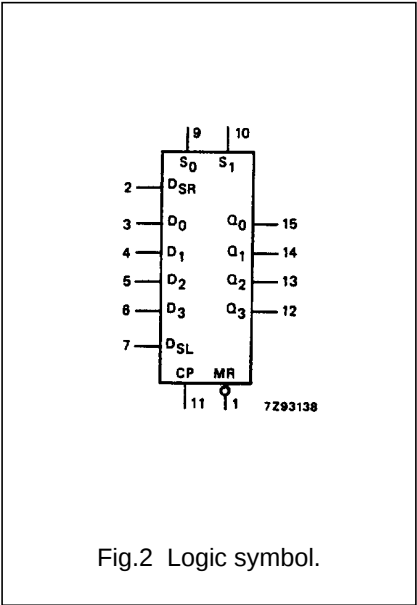
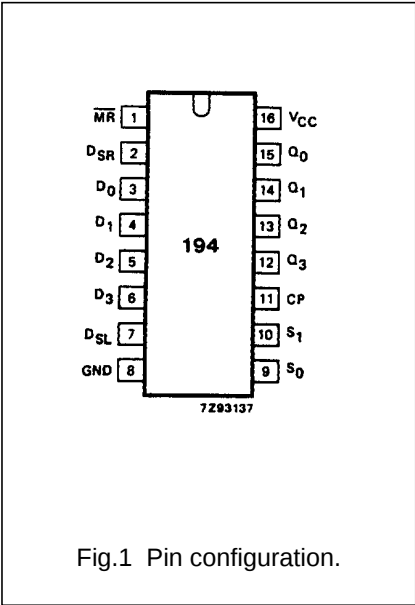
74HC/HCT194

ORDERING INFORMATION

See “74HC/HCT/HCU/HCMOS Logic Package Information”.

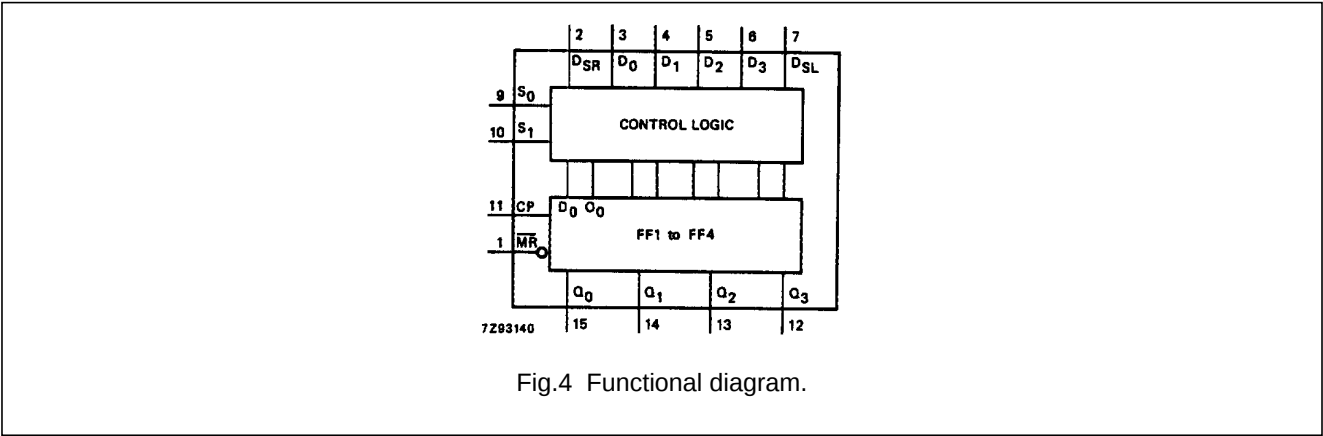
PIN DESCRIPTION

| PIN NO.        | SYMBOL                       | NAME AND FUNCTION                            |
|----------------|------------------------------|----------------------------------------------|
| 1              | $\overline{\text{MR}}$       | asynchronous master reset input (active LOW) |
| 2              | $\text{D}_{\text{SR}}$       | serial data input (shift right)              |
| 3, 4, 5, 6     | $\text{D}_0$ to $\text{D}_3$ | parallel data inputs                         |
| 7              | $\text{D}_{\text{SL}}$       | serial data input (shift left)               |
| 8              | GND                          | ground (0 V)                                 |
| 9, 10          | $\text{S}_0$ , $\text{S}_1$  | mode control inputs                          |
| 11             | CP                           | clock input (LOW-to-HIGH edge-triggered)     |
| 15, 14, 13, 12 | $\text{Q}_0$ to $\text{Q}_3$ | parallel outputs                             |
| 16             | $\text{V}_{\text{CC}}$       | positive supply voltage                      |



4-bit bidirectional universal shift register

74HC/HCT194



FUNCTION TABLE

| OPERATING MODES     | INPUTS |                        |                |                |                 |                 |                | OUTPUTS        |                |                |                |
|---------------------|--------|------------------------|----------------|----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|
|                     | CP     | $\overline{\text{MR}}$ | S <sub>1</sub> | S <sub>0</sub> | D <sub>SR</sub> | D <sub>SL</sub> | D <sub>n</sub> | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| reset (clear)       | X      | L                      | X              | X              | X               | X               | X              | L              | L              | L              | L              |
| hold ("do nothing") | X      | H                      | l              | l              | X               | X               | X              | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> | q <sub>3</sub> |
| shift left          | ↑      | H                      | h              | l              | X               | l               | X              | q <sub>1</sub> | q <sub>2</sub> | q <sub>3</sub> | L              |
|                     | ↑      | H                      | h              | l              | X               | h               | X              | q <sub>1</sub> | q <sub>2</sub> | q <sub>3</sub> | H              |
| shift right         | ↑      | H                      | l              | h              | l               | X               | X              | L              | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> |
|                     | ↑      | H                      | l              | h              | h               | X               | X              | H              | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> |
| parallel load       | ↑      | H                      | h              | h              | X               | X               | d <sub>n</sub> | d <sub>0</sub> | d <sub>1</sub> | d <sub>2</sub> | d <sub>3</sub> |

- Notes
- H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
q,d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition  
X = don't care  
↑ = LOW-to-HIGH CP transition

## 4-bit bidirectional universal shift register

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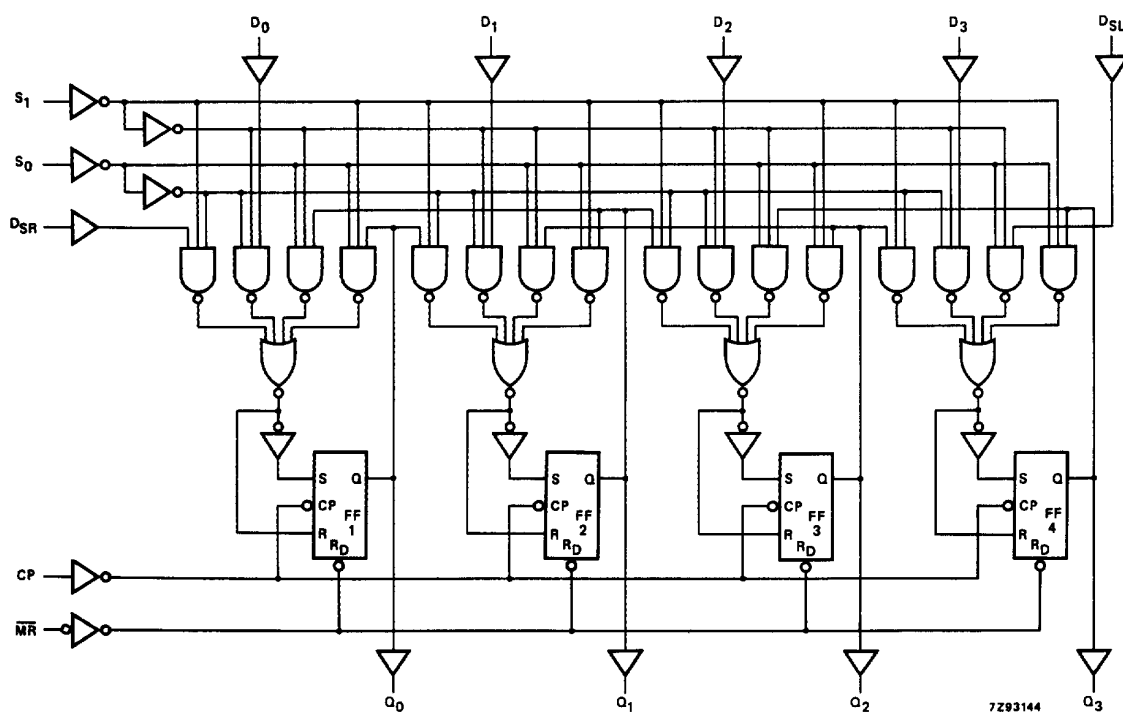


Fig.5 Logic diagram.

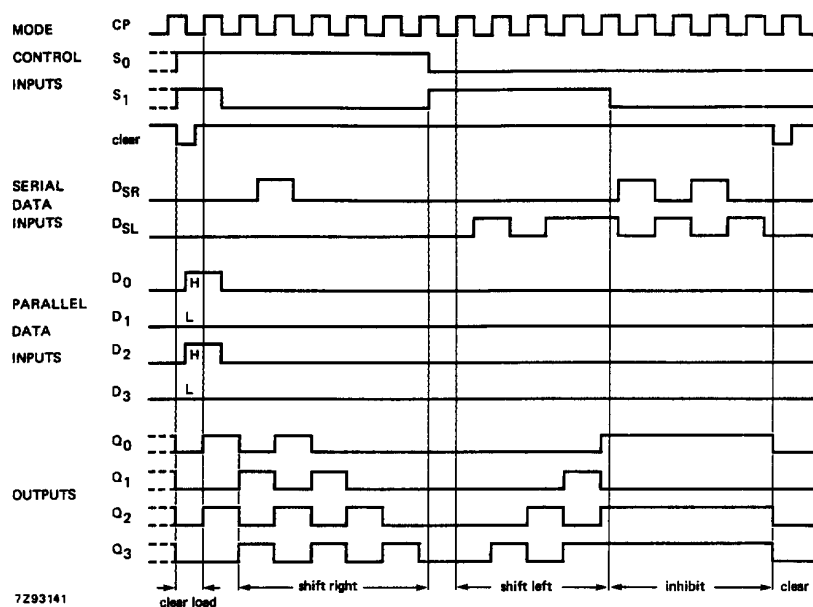


Fig.6 Typical clear, clear-load, shift-right, shift-left, inhibit and clear timing sequences.

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4-bit bidirectional universal shift register74HC/HCT194

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## 4-bit bidirectional universal shift register

## 74HC/HCT194

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                              | PARAMETER                                              | T <sub>amb</sub> (°C) |                 |                 |                 |                 |                 |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|--------------------------------------------------------|-----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
|                                     |                                                        | 74HC                  |                 |                 |                 |                 |                 |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                        | +25                   |                 |                 | −40 to +85      |                 | −40 to +125     |                 |      |                        |           |
|                                     |                                                        | min.                  | typ.            | max.            | min.            | max.            | min.            | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP to Q <sub>n</sub>              |                       | 47<br>17<br>14  | 145<br>29<br>25 |                 | 180<br>36<br>31 |                 | 220<br>44<br>38 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>PHL</sub>                    | propagation delay<br>MR to Q <sub>n</sub>              |                       | 39<br>14<br>11  | 140<br>28<br>24 |                 | 175<br>35<br>30 |                 | 210<br>42<br>36 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                 |                       | 19<br>7<br>6    | 75<br>15<br>13  |                 | 95<br>19<br>16  |                 | 110<br>22<br>19 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>W</sub>                      | clock pulse width<br>HIGH or LOW                       | 80<br>16<br>14        | 17<br>6<br>5    |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>W</sub>                      | master reset pulse<br>width; LOW                       | 80<br>16<br>14        | 17<br>6<br>5    |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>rem</sub>                    | removal time<br>MR to CP                               | 60<br>12<br>10        | 17<br>6<br>5    |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to CP                    | 70<br>14<br>12        | 17<br>6<br>5    |                 | 90<br>18<br>15  |                 | 105<br>21<br>18 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |
| t <sub>su</sub>                     | set-up time<br>S <sub>0</sub> , S <sub>1</sub> to CP   | 80<br>16<br>12        | 22<br>8<br>6    |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.10    |
| t <sub>su</sub>                     | set-up time<br>D <sub>SR</sub> , D <sub>SL</sub> to CP | 70<br>14<br>12        | 19<br>7<br>6    |                 | 90<br>18<br>15  |                 | 105<br>21<br>18 |                 | ns   | 2.0<br>4.5<br>6.0      |           |
| t <sub>h</sub>                      | hold time<br>D <sub>n</sub> to CP                      | 0<br>0<br>0           | −14<br>−5<br>−4 |                 | 0<br>0<br>0     |                 | 0<br>0<br>0     |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |
| t <sub>h</sub>                      | hold time<br>S <sub>0</sub> , S <sub>1</sub> to CP     | 0<br>0<br>0           | −11<br>−4<br>−3 |                 | 0<br>0<br>0     |                 | 0<br>0<br>0     |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.10    |
| t <sub>h</sub>                      | hold time<br>D <sub>SR</sub> , D <sub>SL</sub> to CP   | 0<br>0<br>0           | −17<br>−6<br>−5 |                 | 0<br>0<br>0     |                 | 0<br>0<br>0     |                 | ns   | 2.0<br>4.5<br>6.0      |           |
| f <sub>max</sub>                    | maximum clock pulse<br>frequency                       | 6.0<br>30<br>35       | 31<br>93<br>111 |                 | 4.8<br>24<br>28 |                 | 4.0<br>20<br>24 |                 | MHz  | 2.0<br>4.5<br>6.0      | Fig.7     |

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4-bit bidirectional universal shift register74HC/HCT194

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT                             | UNIT LOAD COEFFICIENT |
|-----------------------------------|-----------------------|
| D <sub>n</sub>                    | 0.15                  |
| D <sub>SR</sub> , D <sub>SL</sub> | 0.15                  |
| CP                                | 0.50                  |
| $\overline{MR}$                   | 0.45                  |
| S <sub>n</sub>                    | 0.90                  |

## 4-bit bidirectional universal shift register

## 74HC/HCT194

## AC CHARACTERISTICS FOR 74HCT

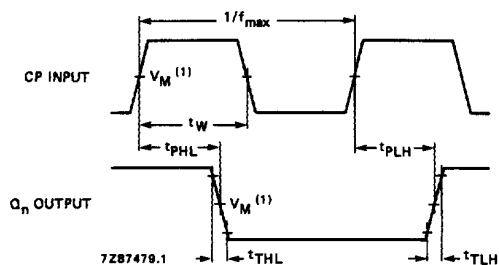
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                              | PARAMETER                                              | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|--------------------------------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
|                                     |                                                        | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                        | +25                   |      |      | −40 to +85 |      | −40 to +125 |      |      |                        |           |
|                                     |                                                        | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP to Q <sub>n</sub>              |                       | 18   | 32   |            | 40   |             | 48   | ns   | 4.5                    | Fig.7     |
| t <sub>PHL</sub>                    | propagation delay<br>MR to Q <sub>n</sub>              |                       | 18   | 32   |            | 40   |             | 48   | ns   | 4.5                    | Fig.8     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                 |                       | 7    | 15   |            | 19   |             | 22   | ns   | 4.5                    | Fig.7     |
| t <sub>W</sub>                      | clock pulse width<br>HIGH or LOW                       | 16                    | 7    |      | 20         |      | 24          |      | ns   | 4.5                    | Fig.7     |
| t <sub>W</sub>                      | master reset pulse<br>width; LOW                       | 16                    | 7    |      | 20         |      | 24          |      | ns   | 4.5                    | Fig.8     |
| t <sub>rem</sub>                    | removal time<br>MR to CP                               | 12                    | 6    |      | 15         |      | 18          |      | ns   | 4.5                    | Fig.8     |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to CP                    | 14                    | 7    |      | 18         |      | 21          |      | ns   | 4.5                    | Fig.9     |
| t <sub>su</sub>                     | set-up time<br>S <sub>0</sub> , S <sub>1</sub> to CP   | 20                    | 10   |      | 25         |      | 30          |      | ns   | 4.5                    | Fig.10    |
| t <sub>su</sub>                     | set-up time<br>D <sub>SR</sub> , D <sub>SL</sub> to CP | 14                    |      |      | 18         |      | 21          |      | ns   | 4.5                    | Fig.9     |
| t <sub>h</sub>                      | hold time<br>D <sub>n</sub> to CP                      | 0                     | −7   |      | 0          |      | 0           |      | ns   | 4.5                    | Fig.9     |
| t <sub>h</sub>                      | hold time<br>S <sub>0</sub> , S <sub>1</sub> to CP     | 0                     | −5   |      | 0          |      | 0           |      | ns   | 4.5                    | Fig.10    |
| t <sub>h</sub>                      | hold time<br>D <sub>SR</sub> , D <sub>SL</sub> to CP   | 0                     | −7   |      | 0          |      | 0           |      | ns   | 4.5                    | Fig.9     |
| f <sub>max</sub>                    | maximum clock pulse<br>frequency                       | 30                    | 70   |      | 24         |      | 20          |      | MHz  | 4.5                    | Fig.7     |

## 4-bit bidirectional universal shift register

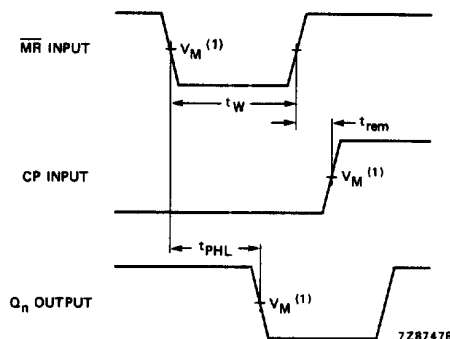
74HC/HCT194

## AC WAVEFORMS



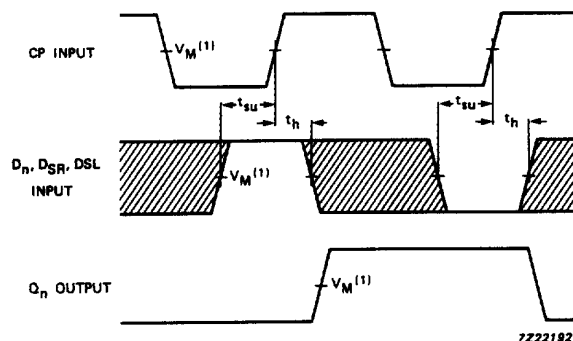
(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

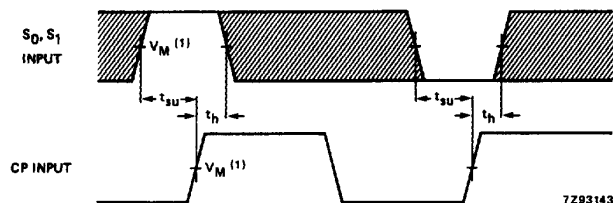
Fig.8 Waveforms showing the master reset ( $\overline{\text{MR}}$ ) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock (CP) removal time.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.9 Waveforms showing the set-up and hold times from the data inputs ( $D_n$ ,  $D_{SR}$  and  $D_{SL}$ ) to the clock (CP).



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.10 Waveforms showing the set-up and hold times from the mode control inputs ( $S_n$ ) to the clock input (CP).

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".