

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT195 4-bit parallel access shift register

Product specification
File under Integrated Circuits, IC06

December 1990

4-bit parallel access shift register

74HC/HCT195

FEATURES

- Asynchronous master reset
- J, $\bar{K}$, (D) inputs to the first stage
- Fully synchronous serial or parallel data transfer
- Shift right and parallel load capability
- Complement output from the last stage
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT195 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT195 performs serial, parallel, serial-to-parallel or parallel-to-serial data transfer at very high speeds. The "195" operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled

by the state of the parallel load enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\bar{K}$ inputs when the $\overline{PE}$ input is HIGH and shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and $\bar{K}$ inputs provide the flexibility of the JK type input for special applications and by tying the pins together, the simple D-type input for general applications. The "195" appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW.

After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0 to D_3) is transferred to the respective Q_0 to Q_3 outputs. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. There is no restriction on the activity of the J, $\bar{K}$, D_n and $\overline{PE}$ inputs for logic operation other than the set-up and hold time requirements. A LOW on the asynchronous master reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	15	15	ns
f_{max}	maximum clock frequency		57	57	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	105	105	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \quad \text{where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

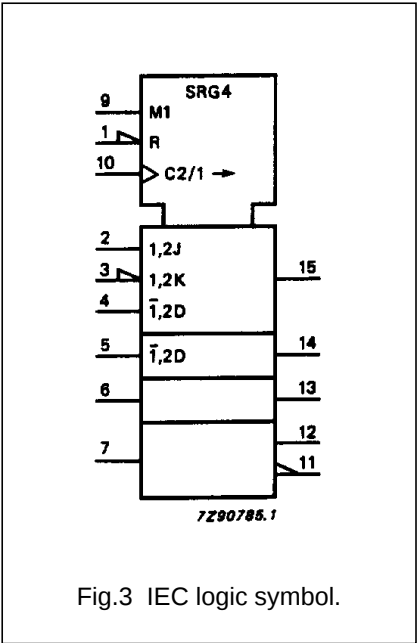
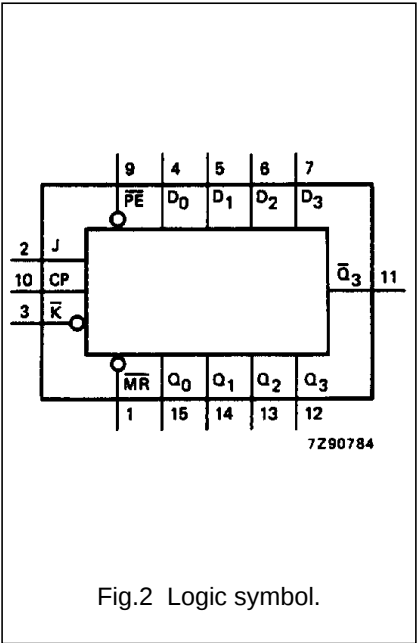
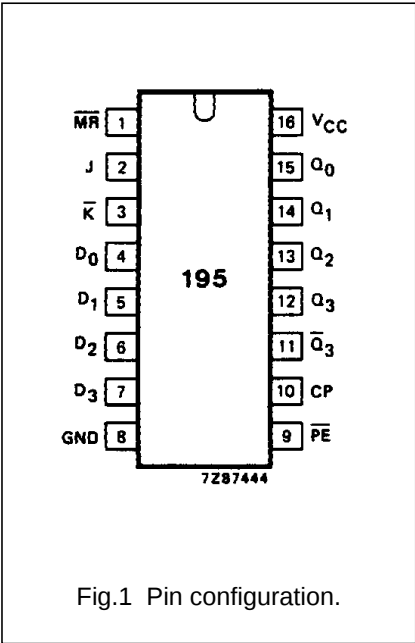
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{MR}}$	master reset input (active LOW)
2	J	first stage J-input (active HIGH)
3	$\overline{\text{K}}$	first stage $\overline{\text{K}}$ -input (active LOW)
4, 5, 6, 7	D ₀ to D ₃	parallel data inputs
8	GND	ground (0 V)
9	$\overline{\text{PE}}$	parallel enable input (active LOW)
10	CP	clock input (LOW-to-HIGH edge-triggered)
11	$\overline{\text{Q}}_3$	inverted output from the last stage
15, 14, 13, 12	Q ₀ to Q ₃	parallel outputs
16	V _{CC}	positive supply voltage



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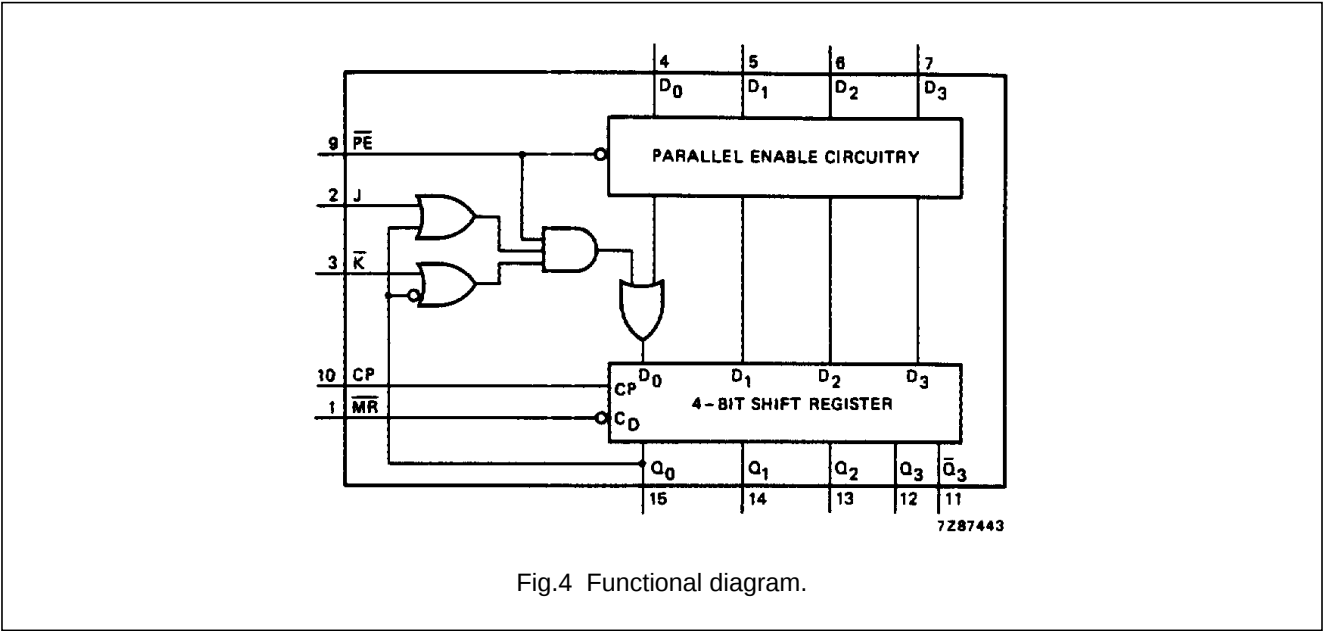


Fig.4 Functional diagram.

APPLICATIONS

- Serial data transfer
- Parallel data transfer
- Serial-to-parallel data transfer
- Parallel-to-serial data transfer

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\bar{K}$	D _n	Q ₀	Q ₁	Q ₂	Q ₃	$\bar{Q}_3$
asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
shift, set first stage	H	↑	h	h	h	X	H	q0	q1	q2	$\bar{q}_2$
shift, reset first stage	H	↑	h	l	l	X	$\bar{L}$	q0	q1	q2	$\bar{q}_2$
shift, toggle first stage	H	↑	h	h	l	X	$\bar{q}_0$	q0	q1	q2	$\bar{q}_2$
shift, retain first stage	H	↑	h	l	h	X	q0	q0	q1	q2	$\bar{q}_2$
parallel load	H	↑	l	X	X	d _n	d ₀	d ₁	d ₂	d ₃	$\bar{d}_3$

Notes

- H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q, d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

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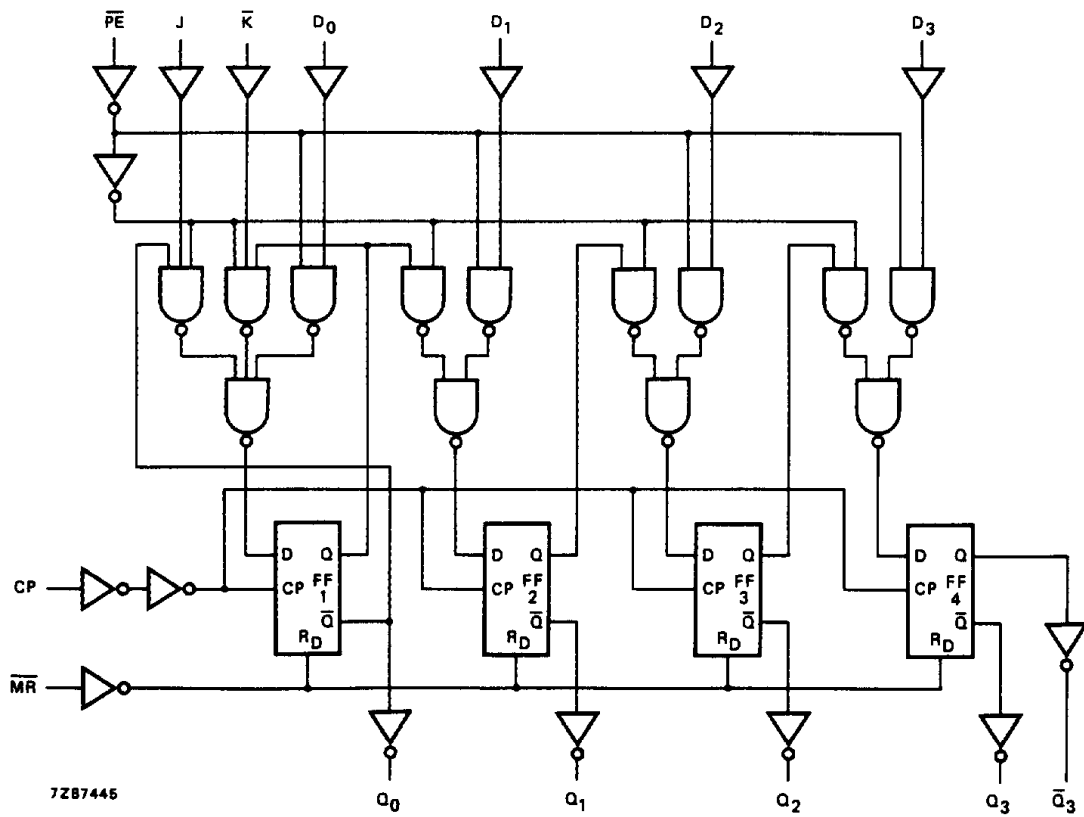


Fig.5 Logic diagram.

4-bit parallel access shift register

74HC/HCT195

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t _{PHL}	propagation delay MR to Q _n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t _w	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t _w	master reset pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t _{rem}	removal time MR to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t _{su}	set-up time J to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Figs 8 and 9
t _{su}	set-up time K, PE, D _n to CP	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 8 and 9
t _h	hold time J, K, PE, D _n to CP	3 3 3	−8 −3 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Figs 8 and 9
f _{max}	maximum clock pulse frequency	6 30 35	17 52 62		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig.6

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DC CHARACTERISTICS FOR HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{PE}$	0.65
all others	0.35

AC CHARACTERISTICS FOR 74HCT

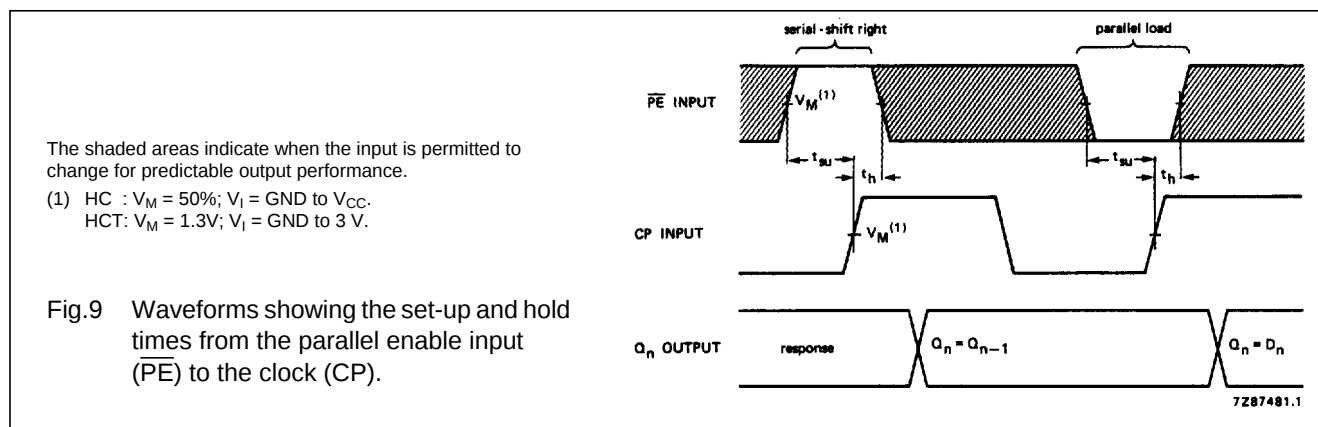
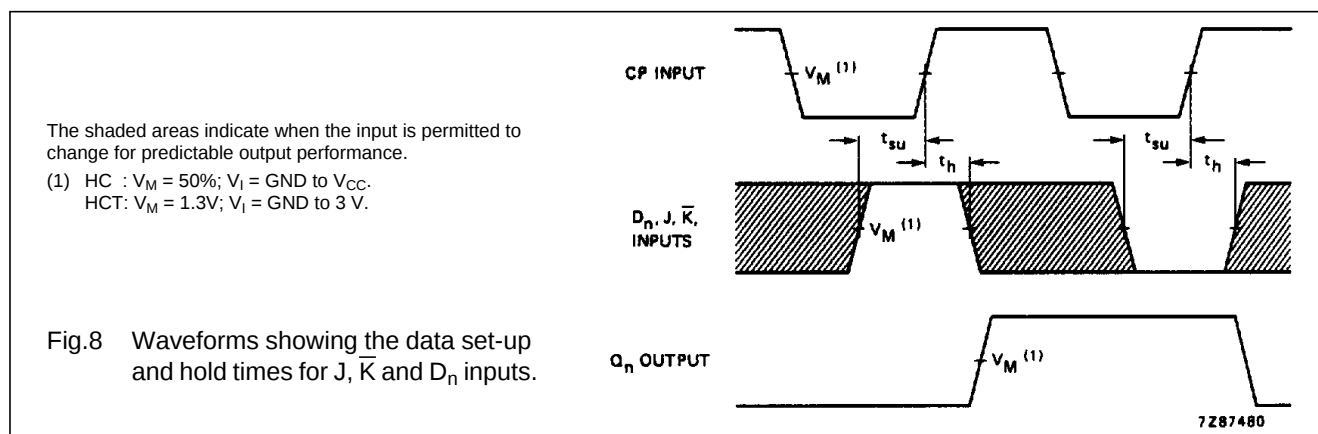
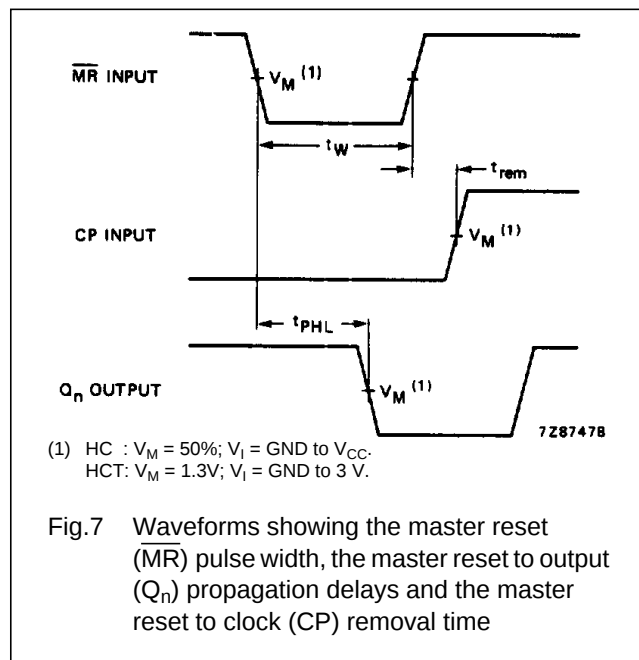
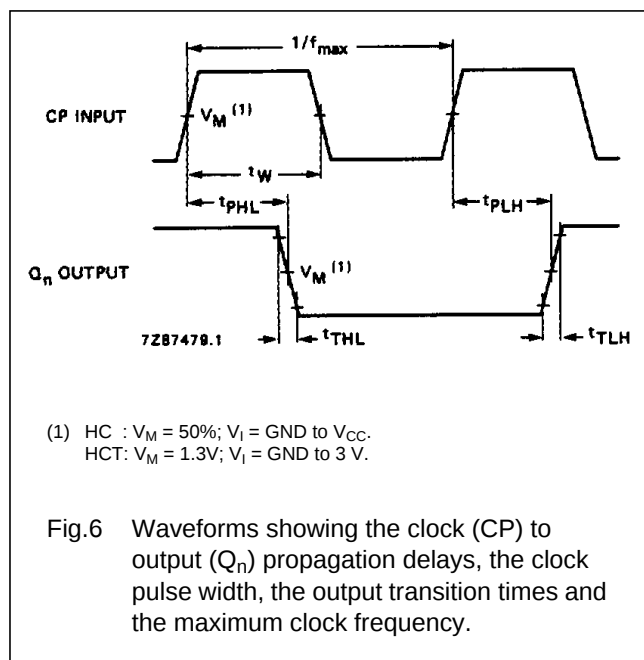
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		18	32		40		48	ns	4.5	Fig.6
t _{PHL}	propagation delay MR to Q _n		17	35		44		53	ns	4.5	Fig.8
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t _W	clock pulse width HIGH or LOW	20	6		25		30		ns	4.5	Fig.6
t _W	master reset pulse width LOW	16	6		20		24		ns	4.5	Fig.8
t _{rem}	removal time $\overline{\text{MR}}$ to CP	16	6		20		24		ns	4.5	Fig.8
t _{su}	set-up time J, K, $\overline{\text{PE}}$ to CP	20	12		25		30		ns	4.5	Figs 8 and 9
t _{su}	set-up time D _n to CP	16	6		20		24		ns	4.5	Figs 8 and 9
t _h	hold time J, K, $\overline{\text{PE}}$, D _n to CP	3	−5		3		3		ns	4.5	Figs 8 and 9
f _{max}	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig.6

4-bit parallel access shift register

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AC WAVEFORMS



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PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.