

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT356

8-input multiplexer/register; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

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74HC/HCT356

FEATURES

- Non-transparent data latches
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT356 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL

(LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT356 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input $\overline{LE}$.

Data on the 8 input lines (D_0 to D_7) is clocked into a edge-triggered data register by a LOW-to-HIGH transition of the clock (CP).

When the output enable input $\overline{OE}_1 = \text{HIGH}$, $\overline{OE}_2 = \text{HIGH}$ or $\overline{OE}_3 = \text{LOW}$, the outputs go to the high impedance OFF-state.

Operation of these output enable inputs does not affect the state of the latches and register.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $S_n, \overline{LE}$ to Y, $\overline{Y}$ CP to Y, $\overline{Y}$	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	24	25	ns
			20	22	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	123	125	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

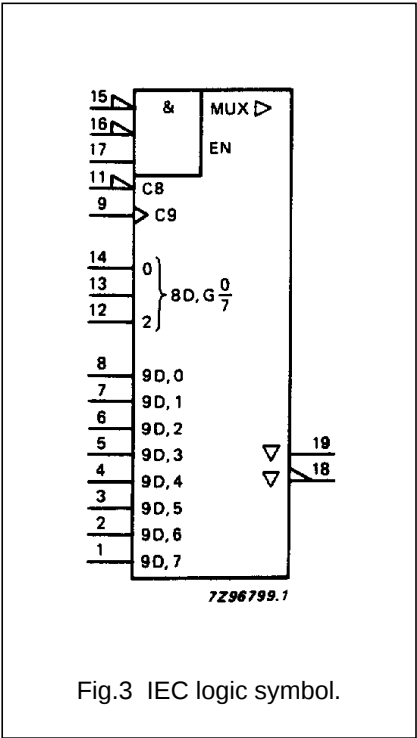
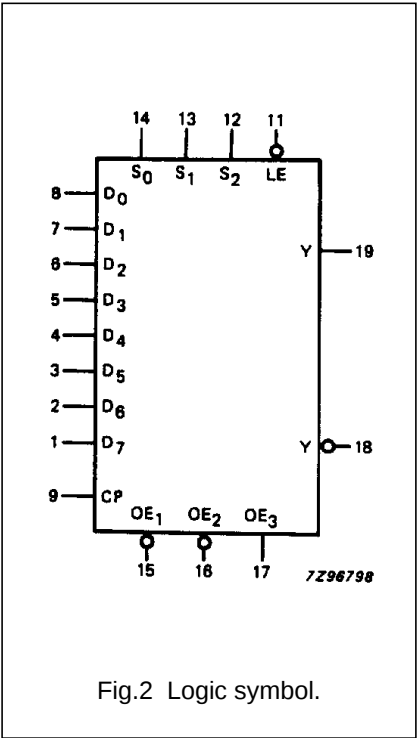
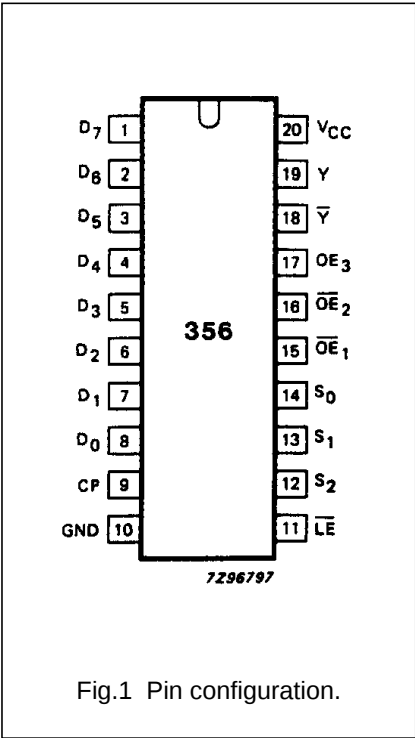
See "74HC/HCT/HCU/HCMOS Logic Package Information".

8-input multiplexer/register; 3-state

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D ₀ to D ₇	data inputs
9	CP	clock input data (LOW-to-HIGH, edge-triggered)
10	GND	ground (0 V)
11	$\overline{\text{LE}}$	address latch enable input (active LOW)
14, 13, 12	S ₀ , S ₁ , S ₂	select inputs
15, 16	$\overline{\text{OE}}_1$, $\overline{\text{OE}}_2$	output enable inputs (active LOW)
17	OE ₃	output enable input (active HIGH)
18	$\overline{\text{Y}}$	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	V _{CC}	positive supply voltage



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FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION
ADDRESS ⁽¹⁾			CP	OUTPUT ENABLE			Y	$\overline{Y}$	
S ₂	S ₁	S ₀		$\overline{OE_1}$	$\overline{OE_2}$	OE ₃			
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	↑	L	L	H	D _{0n}	$\overline{D_{0n}}$	data is clocked into latch
L	L	H	↑	L	L	H	D _{1n}	$\overline{D_{1n}}$	
L	H	L	↑	L	L	H	D _{2n}	$\overline{D_{2n}}$	
L	H	H	↑	L	L	H	D _{3n}	$\overline{D_{3n}}$	
H	L	L	↑	L	L	H	D _{4n}	$\overline{D_{4n}}$	
H	L	H	↑	L	L	H	D _{5n}	$\overline{D_{5n}}$	
H	H	L	↑	L	L	H	D _{6n}	$\overline{D_{6n}}$	
H	H	H	↑	L	L	H	D _{7n}	$\overline{D_{7n}}$	
L	L	L	(2)	L	L	H	D _{0p}	$\overline{D_{0p}}$	outputs do not change states
L	L	H	(2)	L	L	H	D _{1p}	$\overline{D_{1p}}$	
L	H	L	(2)	L	L	H	D _{2p}	$\overline{D_{2p}}$	
L	H	H	(2)	L	L	H	D _{3p}	$\overline{D_{3p}}$	
H	L	L	(2)	L	L	H	D _{4p}	$\overline{D_{4p}}$	
H	L	H	(2)	L	L	H	D _{5p}	$\overline{D_{5p}}$	
H	H	L	(2)	L	L	H	D _{6p}	$\overline{D_{6p}}$	
H	H	H	(2)	L	L	H	D _{7p}	$\overline{D_{7p}}$	

Notes

1. This column shows the input address set-up with $\overline{LE} = \text{LOW}$ (address latch is transparent).
2. CP is HIGH, LOW or ↓.
3. D_{0n} to D_{7n} = data present at inputs D₀ to D₇ when the data latch clock made the transition from LOW-to-HIGH
D_{0p} to D_{7p} = data previously latched into the data latch by the LOW-to-HIGH transition of the data latch clock
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
↓ = HIGH-to-LOW CP transition
Z = high impedance OFF-state

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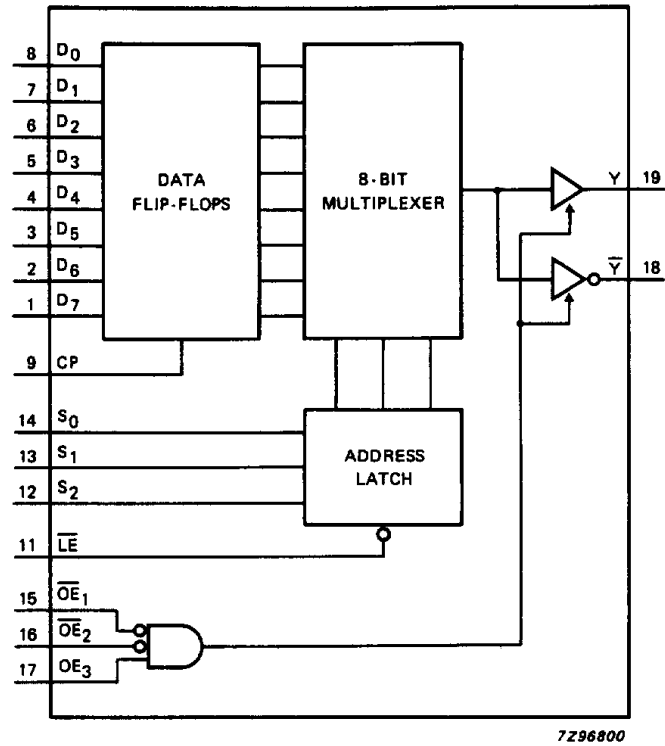


Fig.4 Functional diagram.

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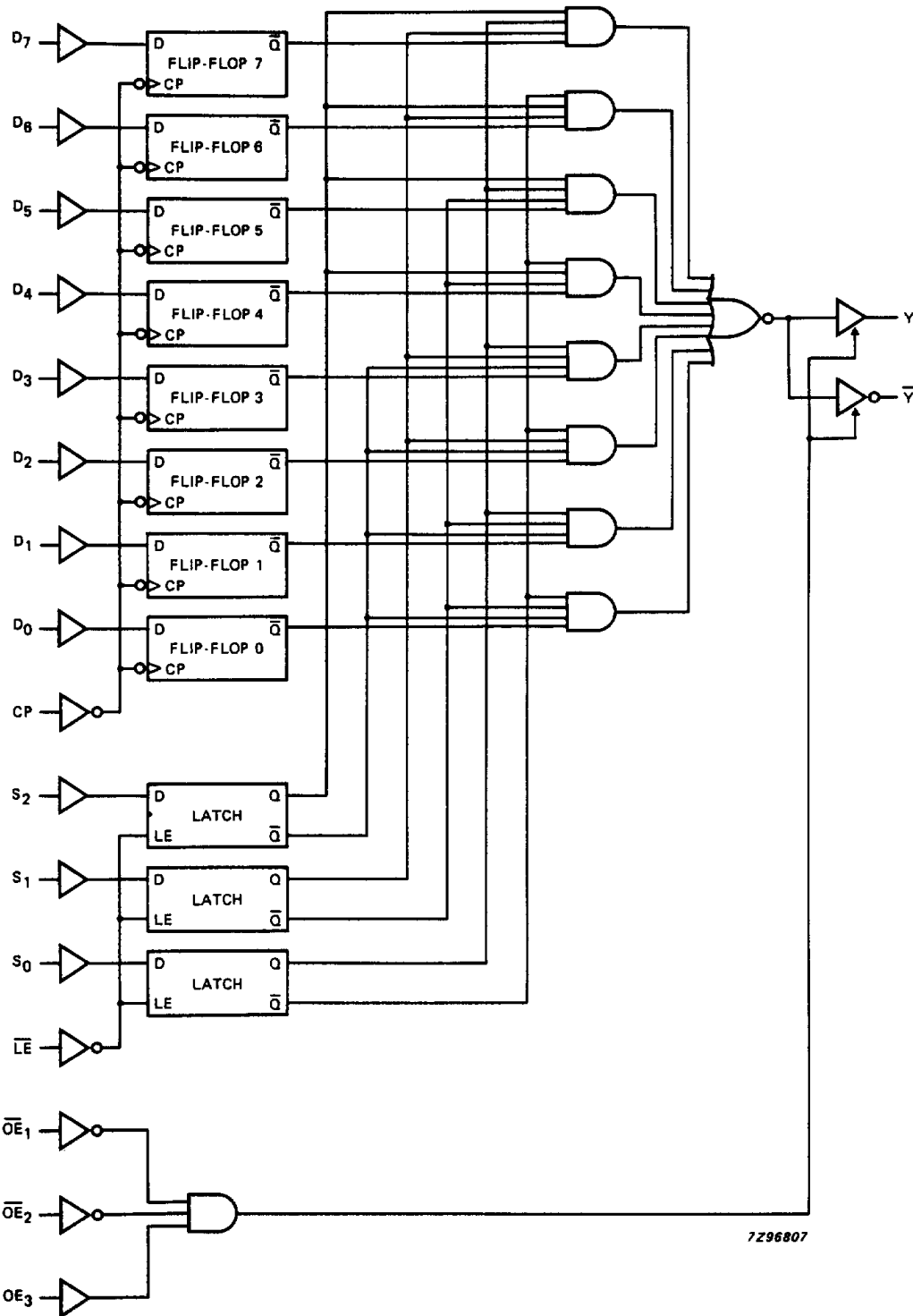


Fig.5 Logic diagram.

8-input multiplexer/register; 3-state

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP to Y, $\overline{Y}$		66 24 19	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay S _n to Y, $\overline{Y}$		77 28 22	260 52 44		325 65 55		390 78 66	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay $\overline{LE}$ to Y, $\overline{Y}$		77 28 22	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	Fig.8
t _{PZH} / t _{PZL}	3-state output enable time $\overline{OE_n}$ to Y, $\overline{Y}$		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.11
t _{PZH} / t _{PZL}	3-state output enable time OE ₃ to Y, $\overline{Y}$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.11
t _{PHZ} / t _{PLZ}	3-state output disable time $\overline{OE_n}$ to Y, $\overline{Y}$		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.11
t _{PHZ} / t _{PLZ}	3-state output disable time OE ₃ to Y, $\overline{Y}$		58 21 17	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.11
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 6, 7 and 8
t _w	clock pulse width CP HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t _w	latch enable pulse width $\overline{LE}$ LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t _{su}	set-up time D _n to CP	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.10

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SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{su}	set-up time S _n to $\overline{\text{LE}}$	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.9	
t _h	hold time D _n to CP	5 5 5	−6 −2 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.10	
t _h	hold time S _n to $\overline{\text{LE}}$	5 5 5	−8 −3 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.9	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n , S _n	0.2
OE ₃	0.25
$\overline{LE}$	0.5
$\overline{OE}_n$, CP	1.0

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AC CHARACTERISTICS FOR 74HCT

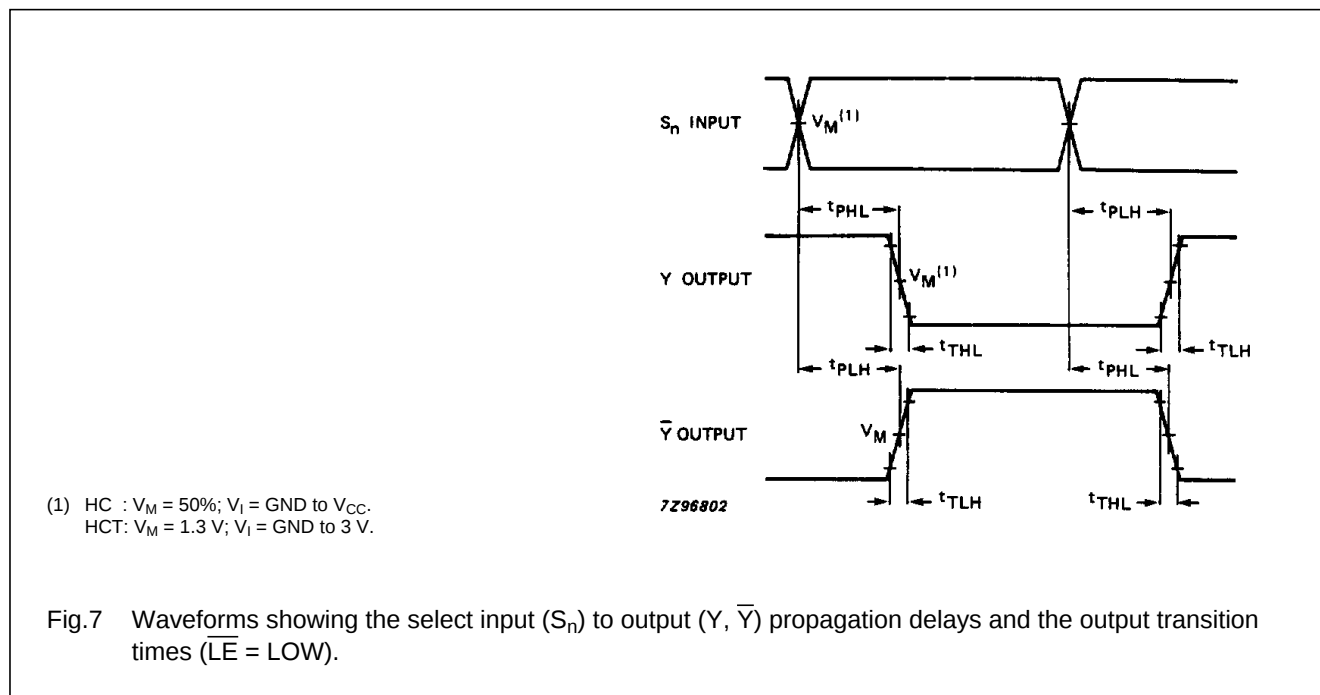
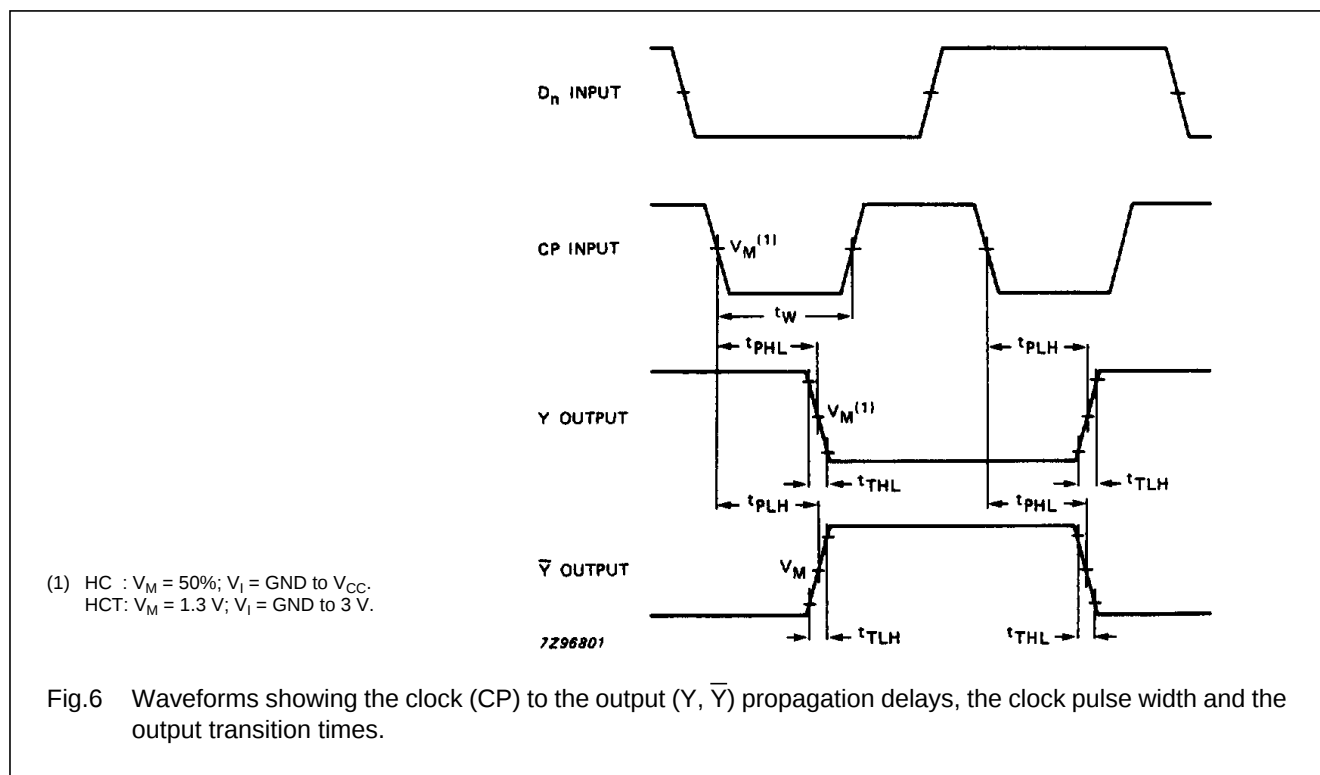
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP to Y, $\overline{Y}$		26	51		64		77	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay S _n to Y, $\overline{Y}$		28	59		74		89	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay $\overline{LE}$ to Y, $\overline{Y}$		29	63		79		95	ns	4.5	Fig.8
t _{PZH} / t _{PZL}	3-state output enable time OE _n to Y, $\overline{Y}$		17	34		43		51	ns	4.5	Fig.11
t _{PZH} / t _{PZL}	3-state output enable time OE ₃ to Y, $\overline{Y}$		18	34		43		51	ns	4.5	Fig.11
t _{PHZ} / t _{PLZ}	3-state output disable time OE _n to Y, $\overline{Y}$		17	33		41		50	ns	4.5	Fig.11
t _{PHZ} / t _{PLZ}	3-state output disable time OE ₃ to Y, $\overline{Y}$		20	33		41		50	ns	4.5	Fig.11
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 6, 7 and 8
t _W	clock pulse width CP HIGH or LOW	16	8		20		24		ns	4.5	Fig.6
t _W	latch enable pulse width $\overline{LE}$ LOW	16	6		20		24		ns	4.5	Fig.8
t _{su}	set-up time D _n to CP	10	4		13		15		ns	4.5	Fig.10
t _{su}	set-up time S _n to $\overline{LE}$	10	5		13		15		ns	4.5	Fig.9
t _h	hold time D _n to CP	5	0		5		5		ns	4.5	Fig.10
t _h	hold time S _n to $\overline{LE}$	5	−2		5		5		ns	4.5	Fig.9

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AC WAVEFORMS



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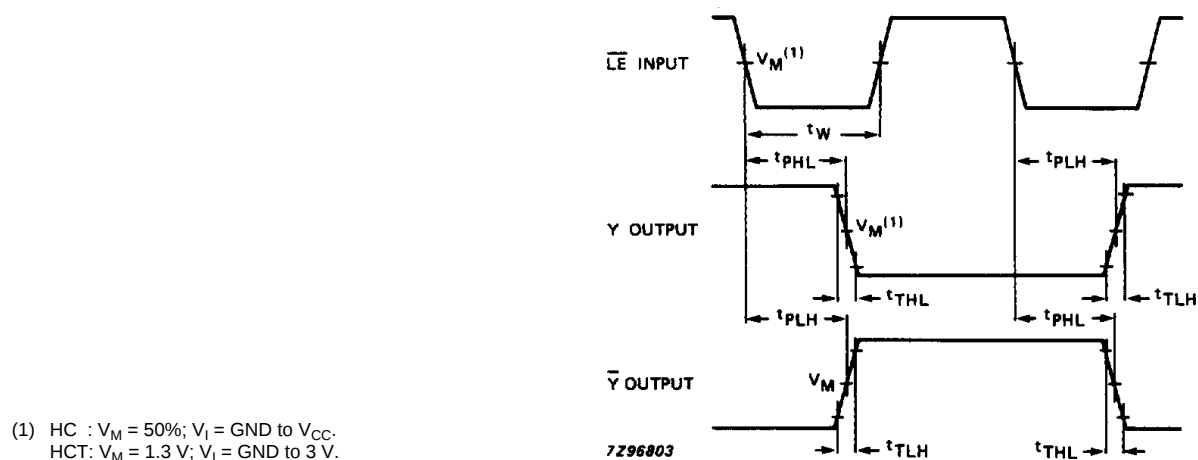


Fig.8 Waveforms showing the address latch enable input ($\overline{\text{LE}}$) pulse width, the latch enable input to output ($Y, \overline{Y}$) propagation delays and the output transition times.

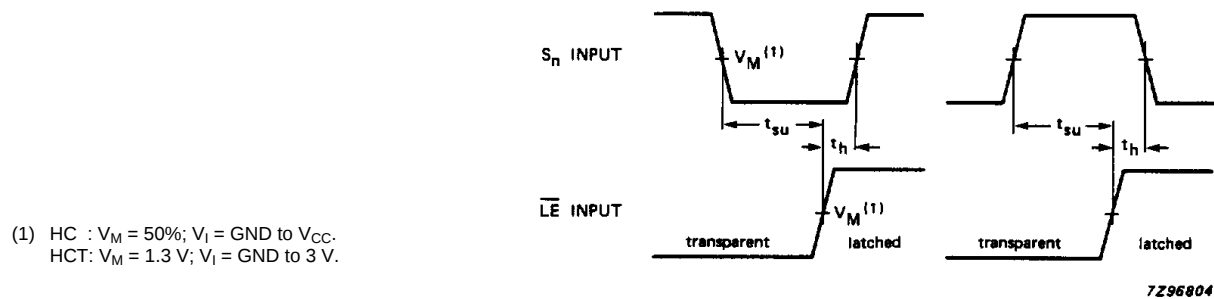


Fig.9 Waveforms showing the set-up and hold times for the select input (S_n) to the address latch enable input ($\overline{\text{LE}}$).

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- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

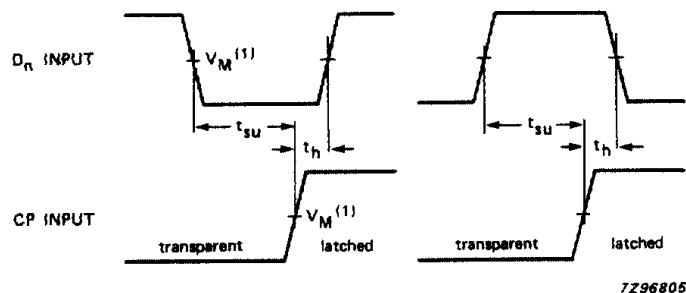


Fig.10 Waveforms showing the set-up and hold times for the data input (D_n) to the clock (CP).

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

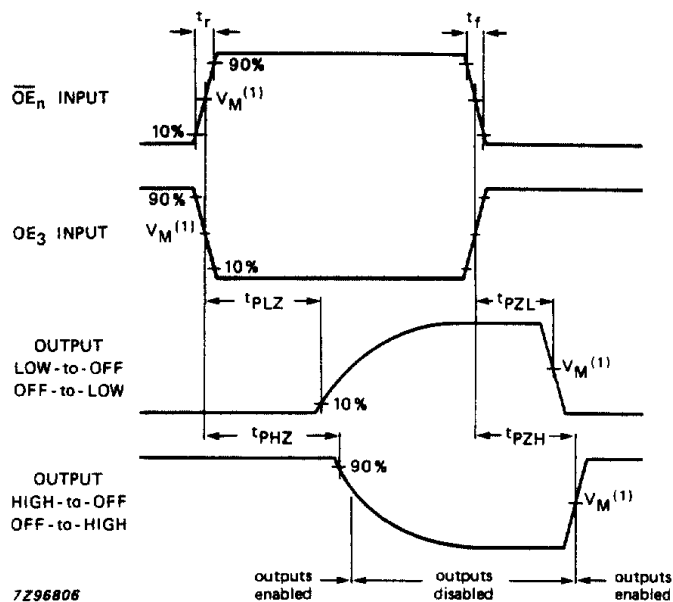


Fig.11 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".